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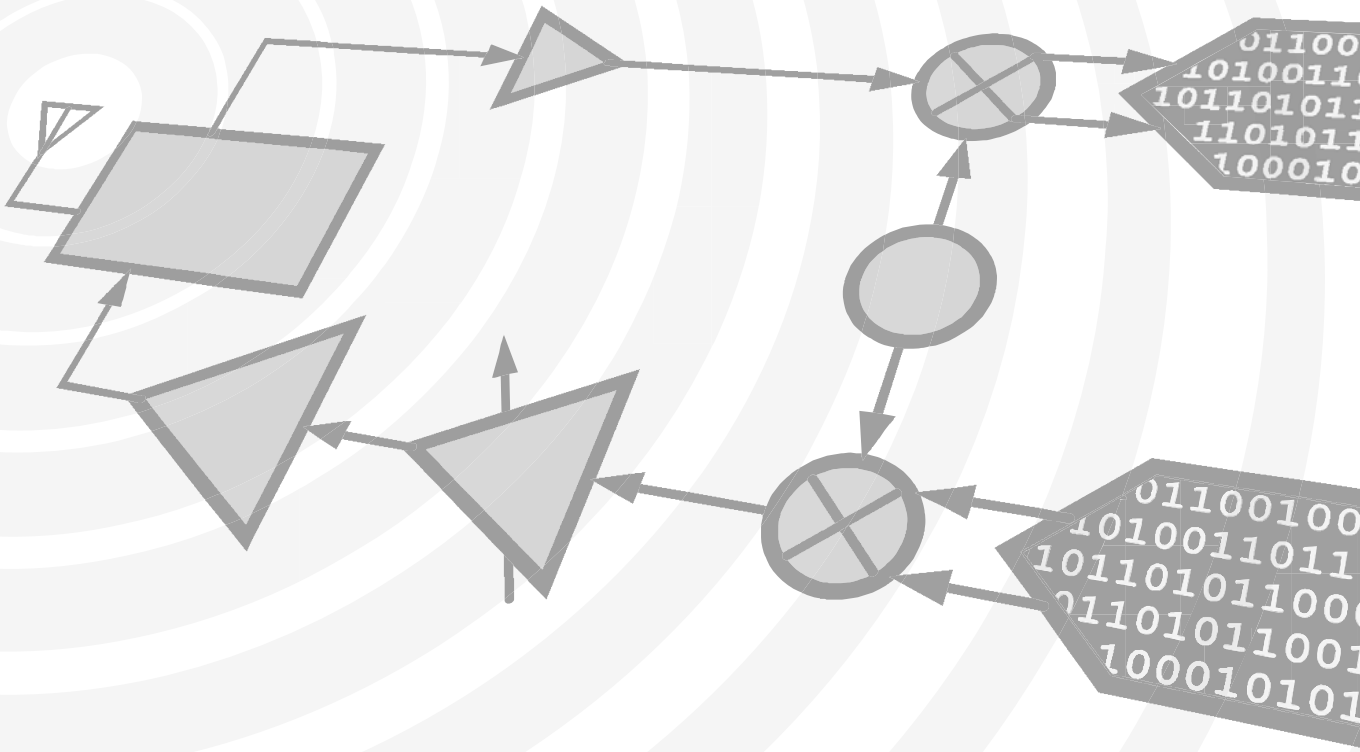

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HMC628* Product Page Quick Links

Last Content Update: 11/01/2016

Comparable Parts

View a parametric search of comparable parts

Evaluation Kits

- HMC628LP4 Evaluation Board

Documentation

Data Sheet

- HMC628 Data Sheet

Reference Materials

Quality Documentation

- Package/Assembly Qualification Test Report: LP4, LP4B, LP4C, LP4K (QTR: 2013-00487 REV: 04)
- Semiconductor Qualification Test Report: BiCMOS-A (QTR: 2013-00235)

Design Resources

- HMC628 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

Discussions

View all HMC628 EngineerZone Discussions

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HMC628LP4 / 628LP4E

v07.0410

BiCMOS MMIC 5-Bit DIGITAL VARIABLE GAIN AMPLIFIER, 50 - 800 MHz

Typical Applications

The HMC628LP4(E) is ideal for:

- Cellular/3G Infrastructure
- WiBro / WiMAX / 4G
- Microwave Radio & VSAT
- Test Equipment and Sensors
- IF & RF Applications

Features

TTL/CMOS compatible serial, parallel or latched parallel control interface

High Output IP3: +35 dBm (At all gain settings)

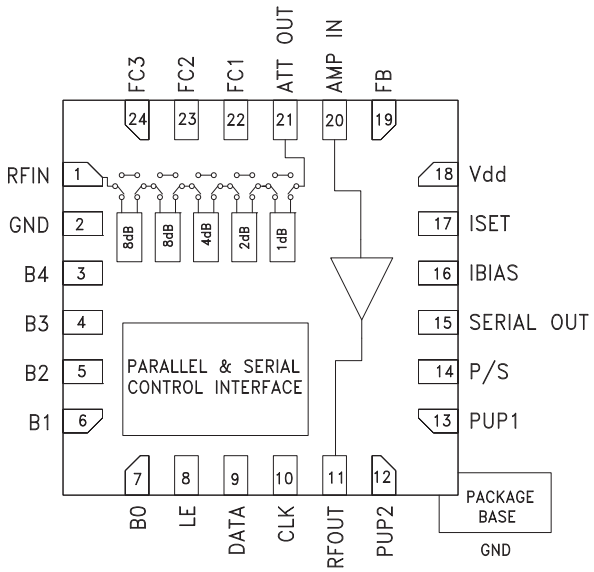
Wide Gain Control Range: 23 dB

Power-up State Selection

24 Lead 4x4 mm SMT Package: 16 mm^2

Excellent State & Step Accuracy (±0.05 dB)

Functional Diagram



General Description

The HMC628LP4(E) is a digitally controlled variable gain amplifier which operates from 50 to 800 MHz, and can be programmed to provide anywhere from 8 dB attenuation, to 15 dB of gain, in 1.0 dB steps. The HMC628LP4(E) delivers noise figure of 5 dB in its maximum gain state, with output IP3 of up to +35 dBm in any state. The dual mode control interface is CMOS/TTL compatible, and accepts either a three wire serial input or a 5 bit parallel word. The HMC628LP4(E) also features a user selectable power up state and a serial output port for cascading other Hittite serial controlled components. The HMC628LP4(E) is housed in a RoHS compliant 4x4 mm QFN leadless package, and is available in three evaluation board configurations, depending on the application frequency.

Electrical Specifications, T_A = +25° C, 50 Ohm System, Vdd= +5V

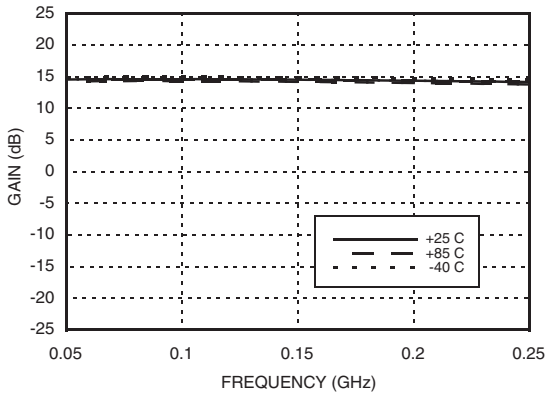
Parameter	50 - 250			250 - 500			500 - 800			MHz
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Gain (Maximum Gain State)	13	15		12.8	14		10.5	13		dB
Gain Control Range		23			23			23		dB
Input Return Loss		12			10			10		dB
Output Return Loss		10			12.5			9		dB
Gain Accuracy: (Referenced to Maximum Gain State)	± (0.1 + 1% of Gain Setting)Max			± (0.4 + 2% of Gain Setting)Max			± (0.4 + 4% of Gain Setting)Max			dB
Output Power for 1dB Compression	19	19.5		16	18		14	18		dBm
Output Third Order Intercept Point		35 [1]			33 [2]			32 [3]		dBm
Output Second Order Intercept Point		46 [1]			54 [2]			55 [3]		dBm
Harmonics 2nd 3rd		46 69			55 75			62 83		dBc dBc
Switching Characteristics tRISE, tFALL (10 / 90% RF) tON, tOFF (Latch Enable to 10 / 90% RF)					11 18					ns ns
Noise Figure		5			6			6.5		dB
Supply Current (Idd)		65	85		65	85		65	85	mA

[1] Two-Tone Output Power @ 5 dBm [2] Two-Tone Output Power @ 2 dBm [3] Two-Tone Output Power @ 0 dBm

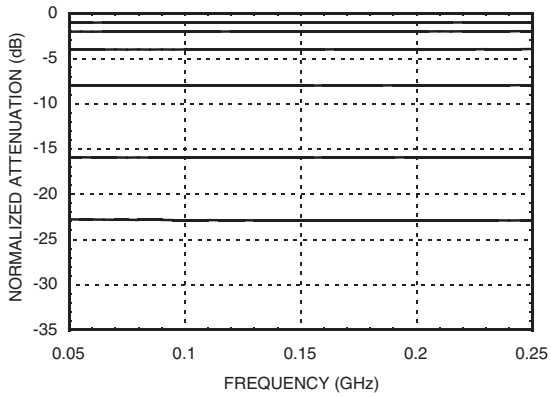
BiCMOS MMIC 5-Bit DIGITAL VARIABLE GAIN AMPLIFIER, 50 - 800 MHz

50 to 250 MHz Tuning

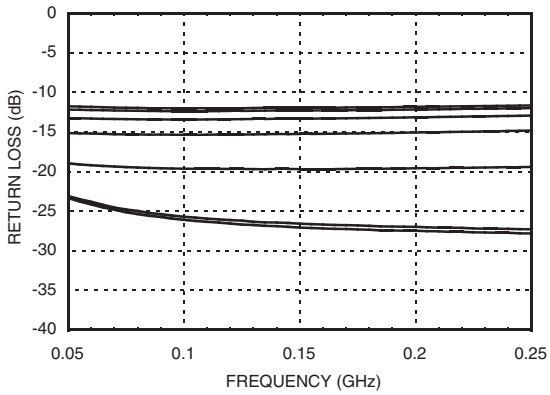
Maximum Gain vs. Frequency



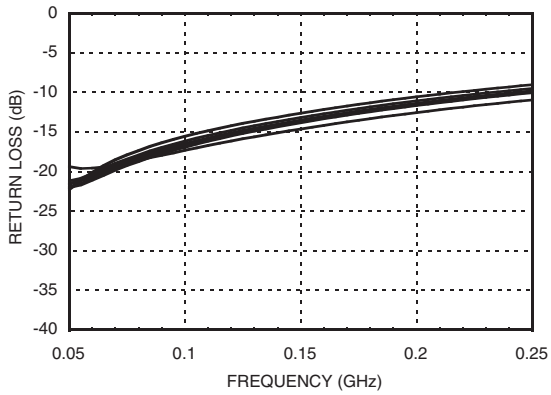
Normalized Attenuation
(Only Major States are Shown)



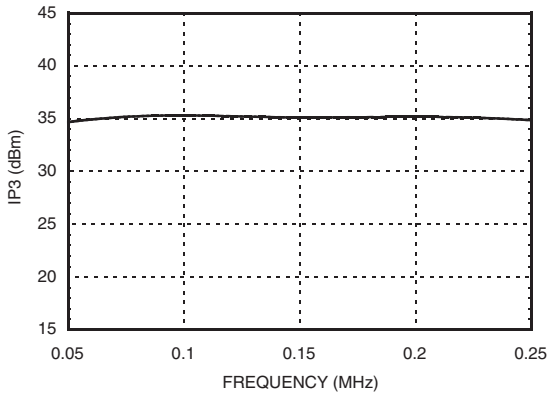
Input Return Loss
(Only Major States are Shown)



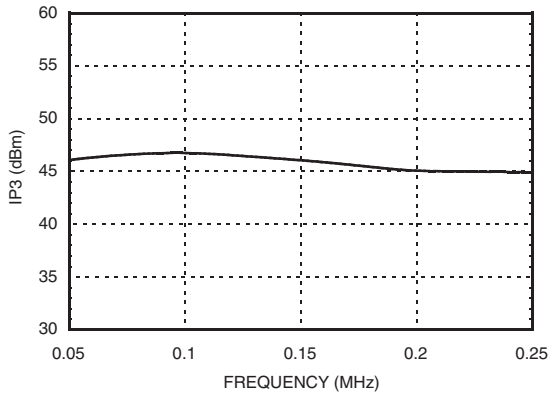
Output Return Loss
(Only Major States are Shown)



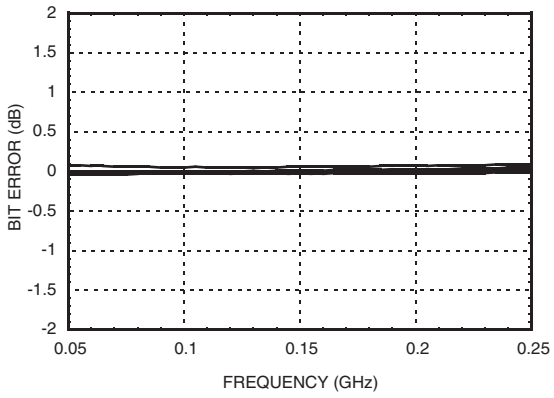
Output IP3 vs. Frequency



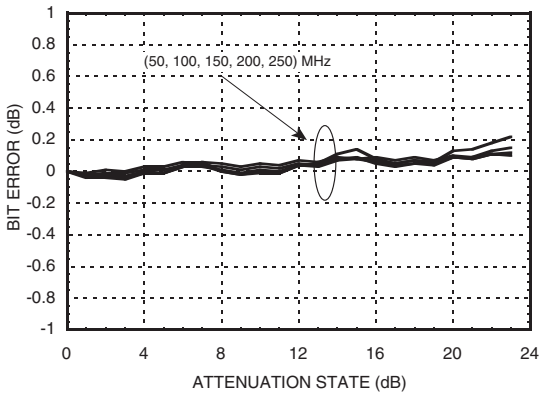
Output IP2 vs. Frequency



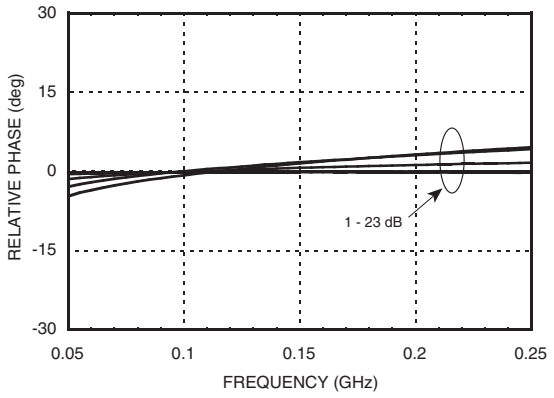
Bit Error vs. Frequency
(Only Major States are Shown)



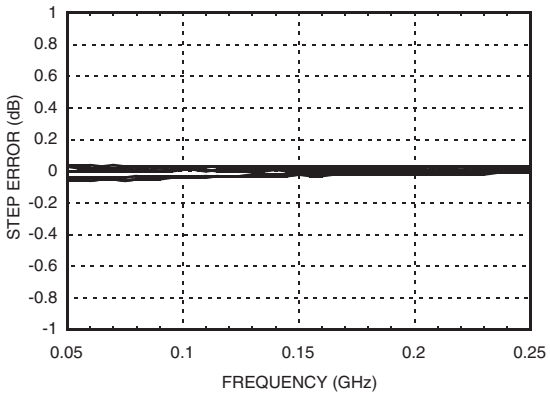
Bit Error vs. Attenuation State



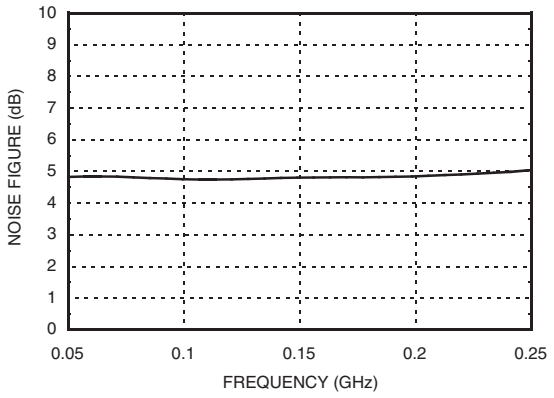
Normal Relative Phase vs. Frequency
(Only Major States are Shown)



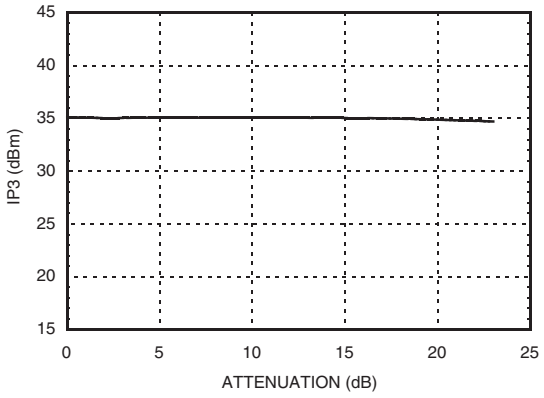
Step Error vs. Frequency
(Only Major States are Shown)



Noise Figure vs. Frequency



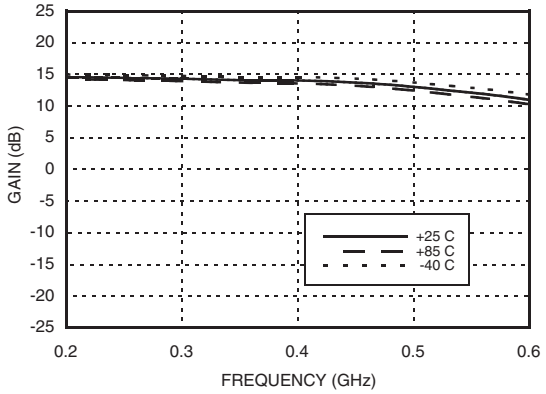
Output IP3 vs. Attenuation @ 150 MHz



BiCMOS MMIC 5-Bit DIGITAL VARIABLE GAIN AMPLIFIER, 50 - 800 MHz

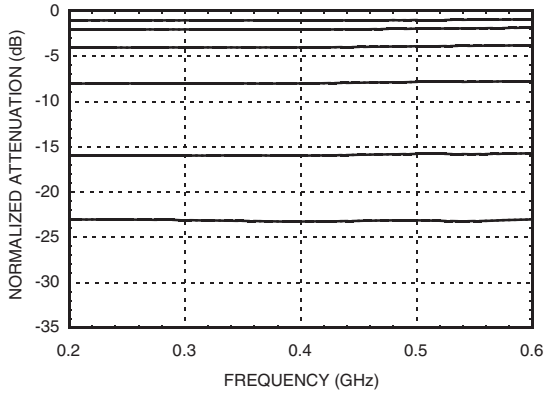
250 to 500 MHz Tuning

Maximum Gain vs. Frequency



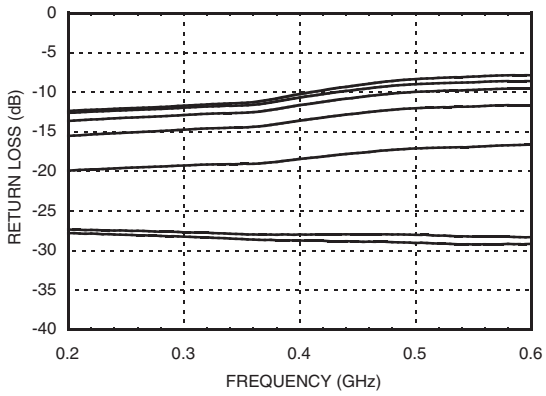
Normalized Attenuation

(Only Major States are Shown)



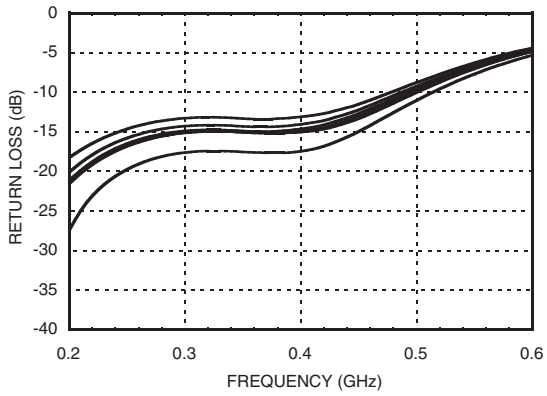
Input Return Loss

(Only Major States are Shown)

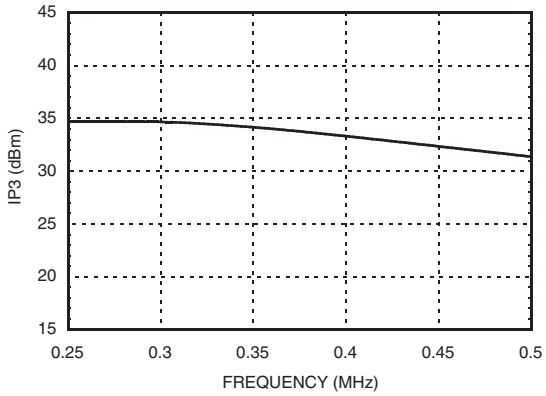


Output Return Loss

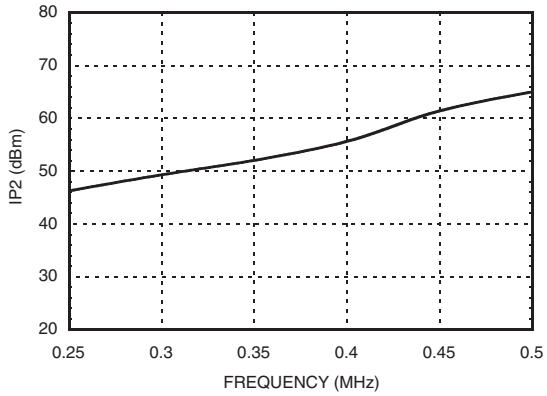
(Only Major States are Shown)



Output IP3 vs. Frequency



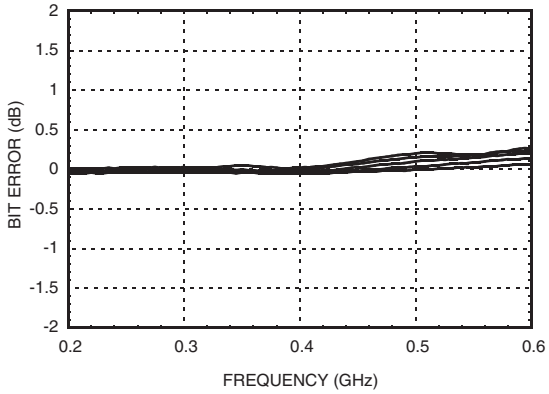
Output IP2 vs. Frequency



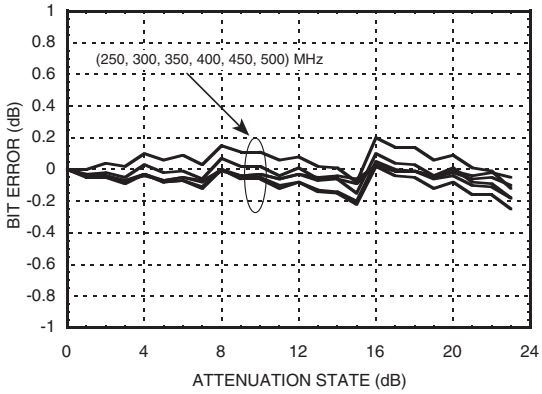
BiCMOS MMIC 5-Bit DIGITAL VARIABLE GAIN AMPLIFIER, 50 - 800 MHz

250 to 500 MHz Tuning

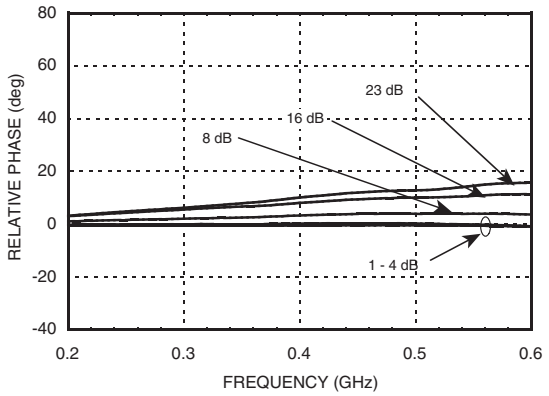
Bit Error vs. Frequency
(Only Major States are Shown)



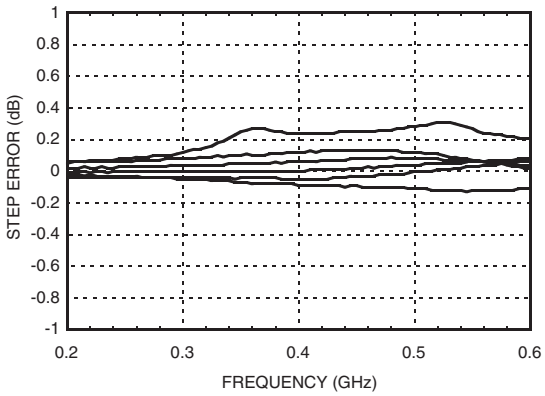
Bit Error vs. Attenuation State



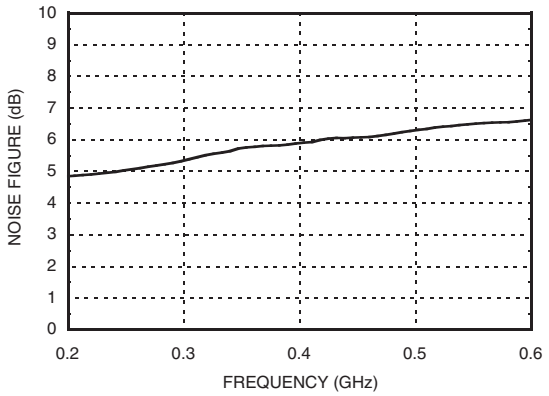
Normal Relative Phase vs. Frequency
(Only Major States are Shown)



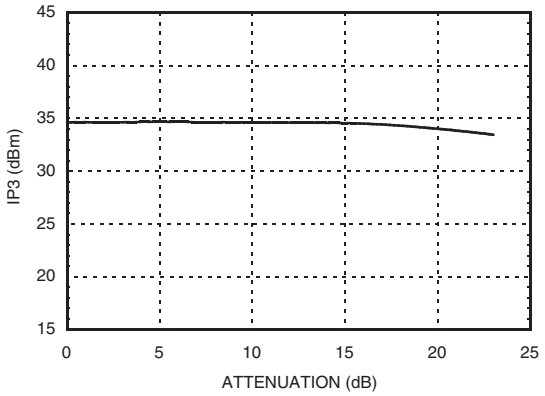
Step Error vs. Frequency
(Only Major States are Shown)



Noise Figure vs. Frequency

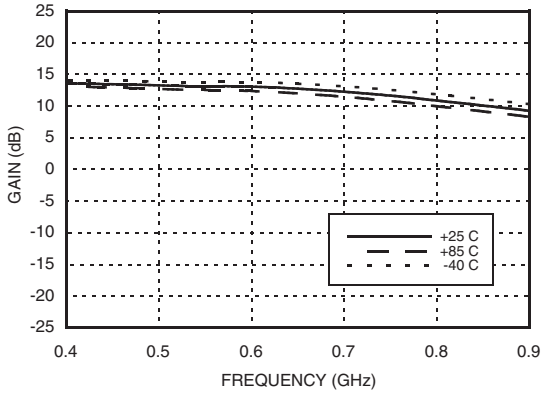


Output IP3 vs. Attenuation @ 350 MHz



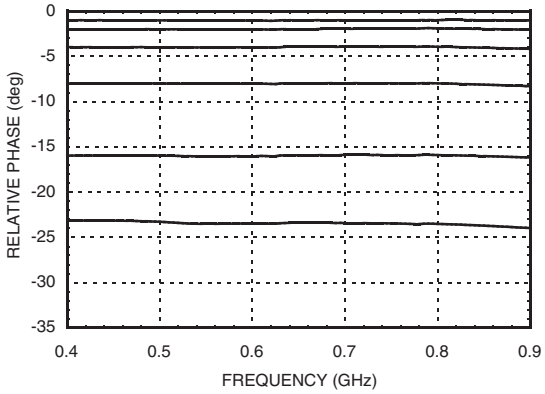
500 to 800 MHz Tuning

Maximum Gain vs. Frequency



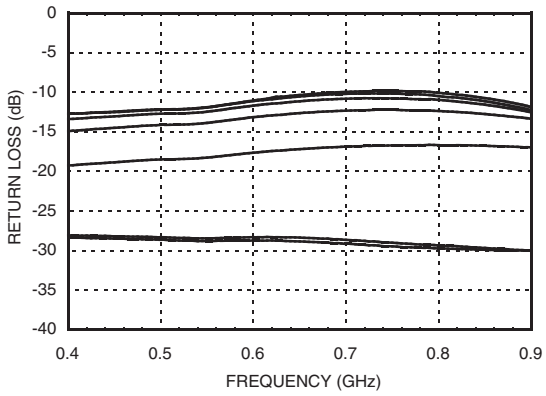
Normalized Attenuation

(Only Major States are Shown)



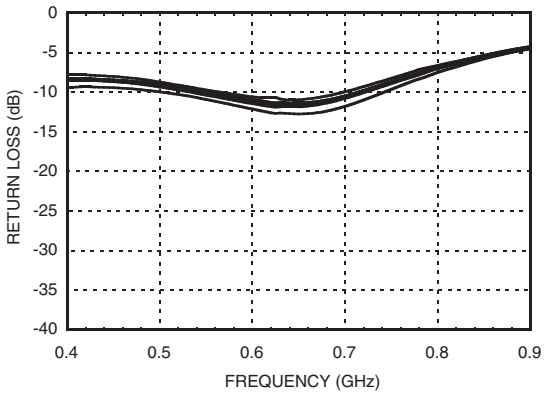
Input Return Loss

(Only Major States are Shown)

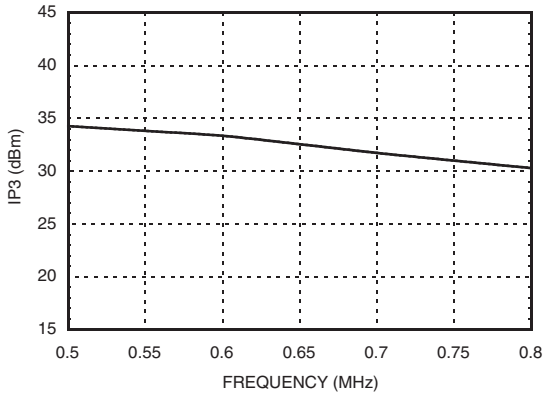


Output Return Loss

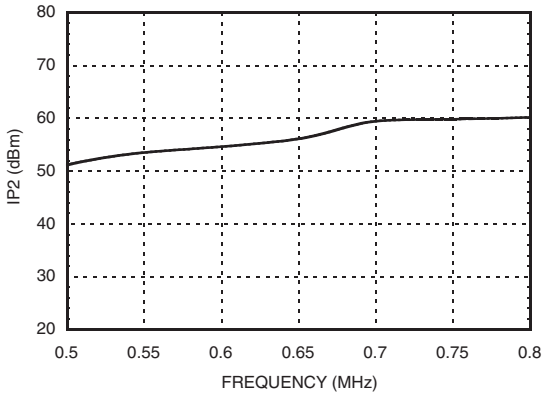
(Only Major States are Shown)



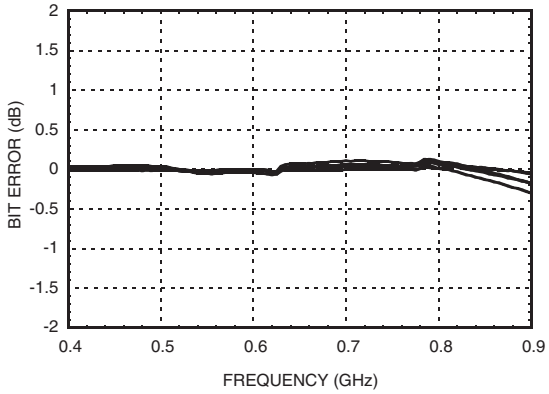
Output IP3 vs. Frequency



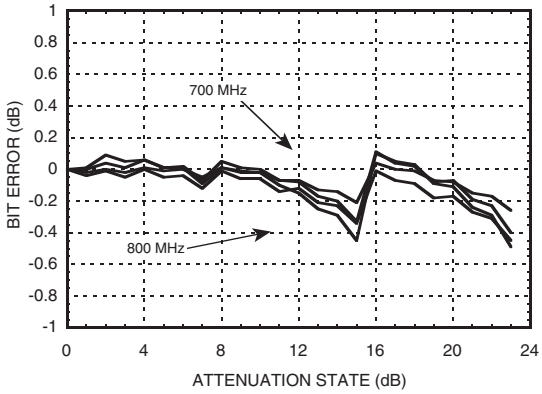
Output IP2 vs. Frequency



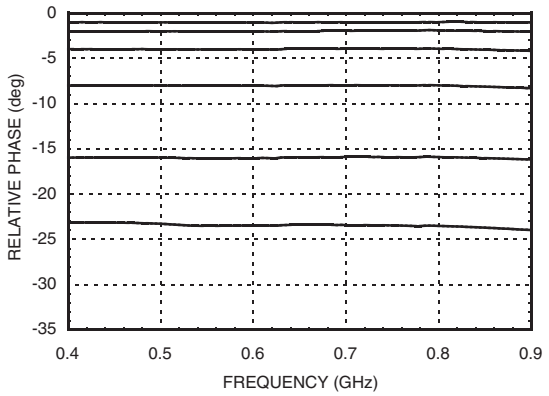
Bit Error vs. Frequency
(Only Major States are Shown)



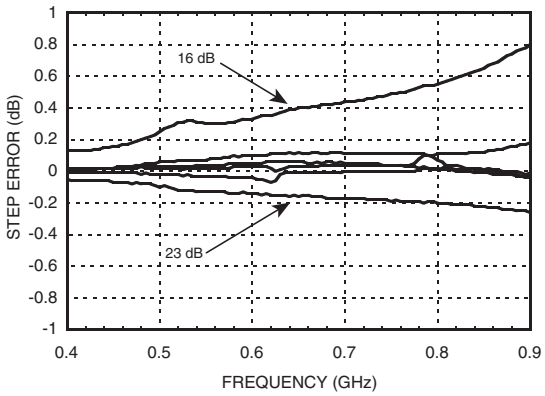
Bit Error vs. Attenuation State



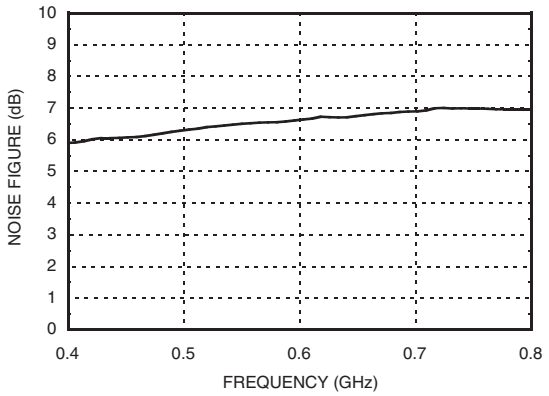
Normal Relative Phase vs. Frequency
(Only Major States are Shown)



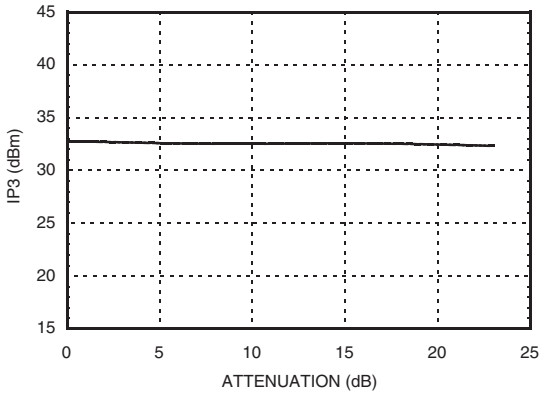
Step Error vs. Frequency
(Only Major States are Shown)



Noise Figure vs. Frequency



Output IP3 vs. Attenuation @ 650 MHz

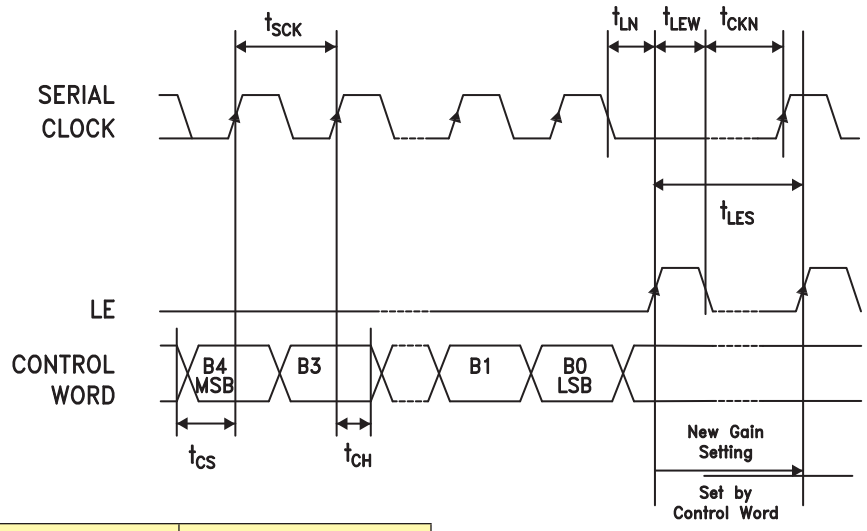


Serial Control Interface

The HMC628LP4(E) contains a 3-wire SPI compatible digital interface (DATA, CLK, LE). It is activated when P/S is kept high. The 5-bit serial word must be loaded MSB first. The positive-edge sensitive CLK and LE requires clean transitions. Standard logic families work well. If mechanical switches were used, sufficient debouncing should be provided. When LE is high, 5-bit data in the serial input register is transferred to the attenuator. When LE is high CLK is masked to prevent data transition during output loading.

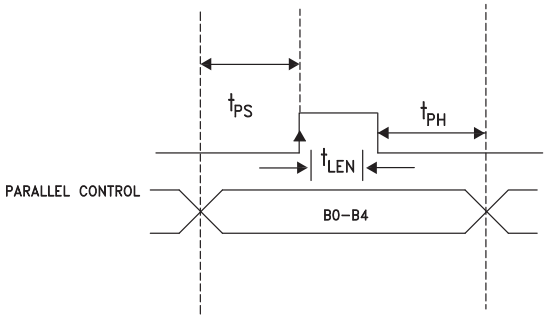
When P/S is low, 3-wire SPI interface inputs (DATA, CLK, LE) are disabled and serial input register is loaded asynchronously with parallel digital inputs (B0-B4). When Le is high, 5-bit parallel data is transferred to the attenuator.

For all modes of operations, attenuation state will stay constant while LE is kept low.



Parameter	Typ.
Min. serial period, t_{SCK}	100 ns
Control set-up time, t_{CS}	20 ns
Control hold-time, t_{CH}	20 ns
LE Set up-time, t_{LN}	10 ns
Min. LE pulse width, t_{LEW}	10 ns
Min LE pulse spacing, t_{LES}	530 ns
Serial clock hold-time from LE, t_{CKN}	10 ns
Hold Time, t_{PH}	0 ns
Latch Enable Minimum Width, t_{LEN}	10 ns
Setup Time, t_{PS}	2 ns

Timing Diagram *(Latched Parallel Mode)*



Parallel Mode

(Direct Parallel Mode & Latched Parallel Mode)

Note: The parallel mode is enabled when P/S is set to low.

Direct Parallel Mode - The attenuation state is changed by the Control Voltage Inputs directly. The LE (Latch Enable) must be at a logic high to control the attenuator in this manner.

Latched Parallel Mode - The attenuation state is selected using the Control Voltage Inputs and set while the LE is in the Low state. The attenuator will not change state while LE is Low. Once all Control Voltage Inputs are at the desired states the LE is pulsed. See timing diagram above for reference.

Power-Up States

If LE is set to logic LOW at power-up, the logic state of PUP1 and PUP2 determines the power-up state of the part per PUP truth table. If the LE is set to logic HIGH at power-up, the logic state of B4-B0 determines the power-up state of the part per truth table. The DVGA latches in the desired power-up state approximately 200 ms after power-up.

Power-On Sequence

The ideal power-up sequence is: GND, Vdd, digital inputs, RF inputs. The relative order of the digital inputs are not important as long as they are powered after Vdd / GND

Absolute Maximum Ratings

RF Input Power	20 dBm
RF Output Power	22 dBm
Digital Inputs (B0-B4, Shift Clock, Latch Enable & Data Input)	-0.5V to Vdd +0.5V
Bias Voltage (Vdd)	5.6 V
Junction Temperature	125 °C
Continuous Pdiss (T = 85 °C) (derate 13.5 mW/°C above 85 °C) [1]	0.54 W
Thermal Resistance (Junction to ground paddle)	74.3 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

Bias Voltage

Vdd (V)	Idd (Typ.) (mA)
5V	65

Control Voltage Table

State	Vdd = +3V	Vdd = +5V
Low	0 to 0.5V @ <1 µA	0 to 0.8V @ <1 µA
High	2 to 3V @ <1 µA	2 to 5V @ <1 µA

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

PUP Truth Table

LE	PUP1	PUP2	Gain Relative to Maximum Gain
0	0	0	Insertion Loss
0	1	0	-8
0	0	1	-16
0	1	1	-23
1	X	X	0 to -23 dB

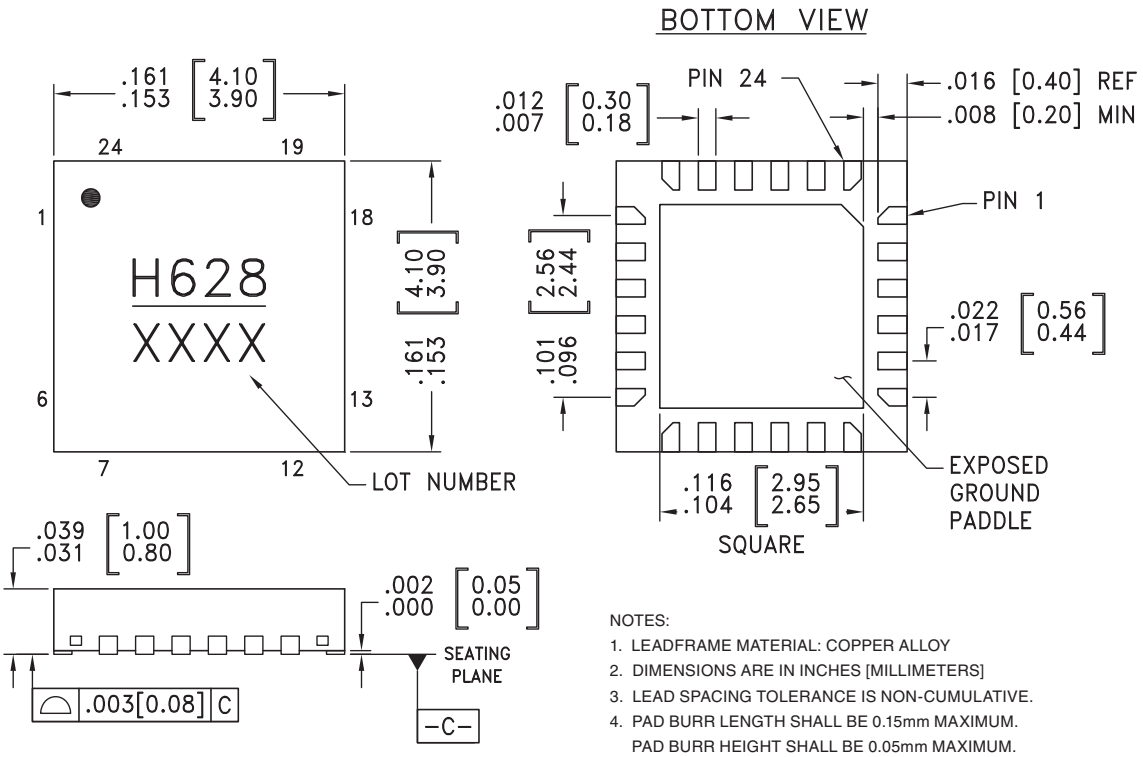
Note: Power-Up with LE= 1 provides direct parallel operation with B4-B0.

Truth Table

ATTENUATION (dB)	B4[1]	B3[1]	B2	B1	B0
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	0	1	0	1	1
12	0	1	1	0	0
13	0	1	1	0	1
14	0	1	1	1	0
15	0	1	1	1	1
16	1	X	0	0	0
17	1	X	0	0	1
18	1	X	0	1	0
19	1	X	0	1	1
20	1	X	1	0	0
21	1	X	1	0	1
22	1	X	1	1	0
23	1	X	1	1	1

[1] Enabling B4 disables B3, the minimum attenuation is 16 dB

Outline Drawing



NOTES:

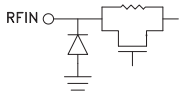
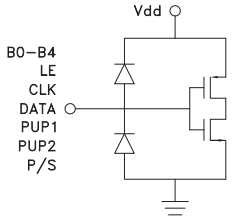
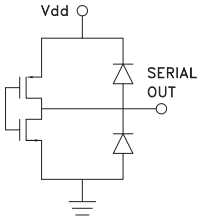
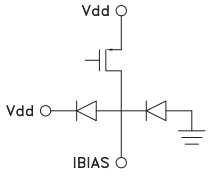
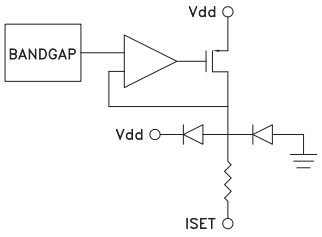
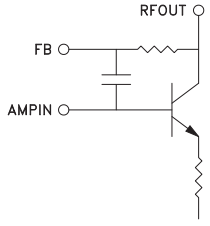
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

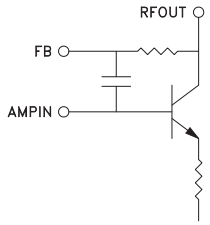
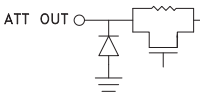
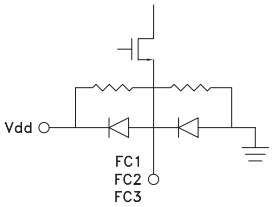
Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC628LP4	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H628 XXXX
HMC628LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H628 XXXX

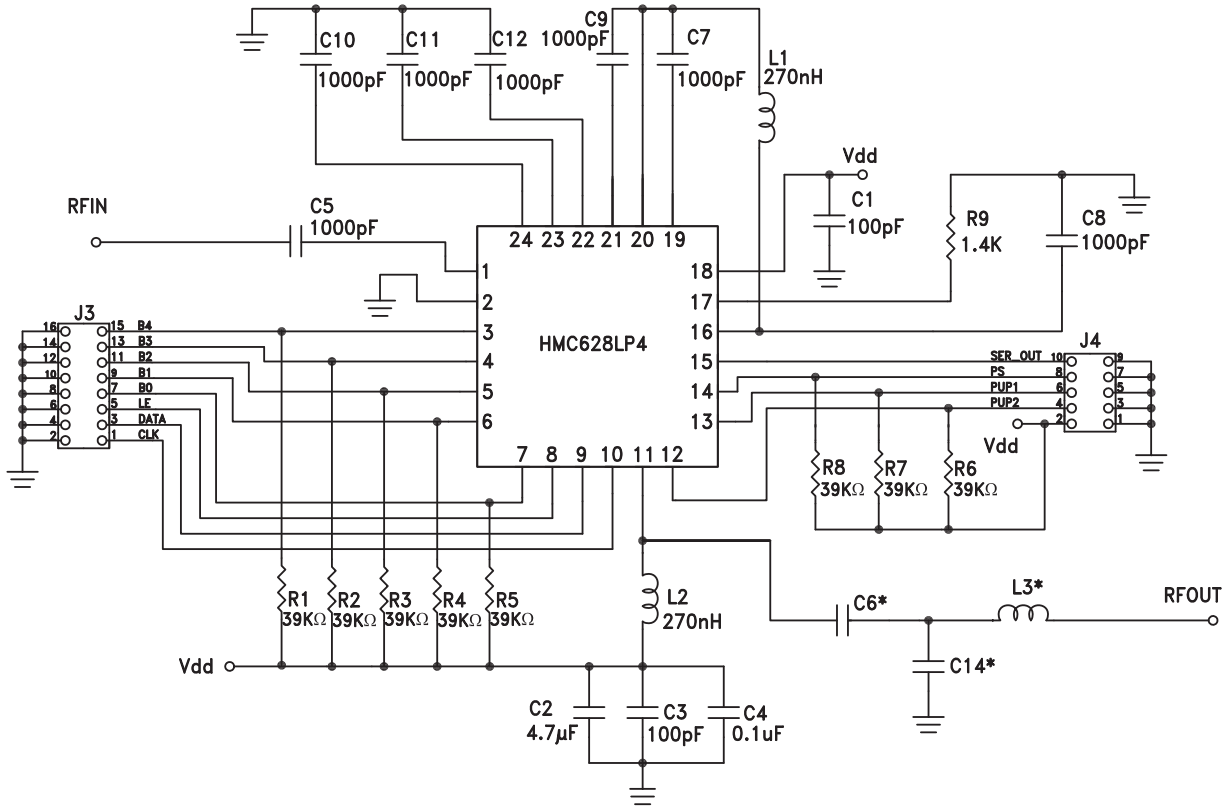
[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	RFIN	This pin is DC coupled and matched to 50 Ohms. A blocking capacitor is needed.	
2	GND	These pins and package bottom must be connected to RF/DC ground.	
3 - 7	B4, B3, B2, B1, B0	See Truth Table, Control Voltage Table and Timing Diagram.	
8	LE		
9	DATA		
10	CLK		
12	PUP2		
13	PUP1		
14	P/S		
15	SERIAL OUT	Serial input data delayed by 5 clock cycles.	
16	IBIAS	Bias current to amplifier. External inductor is needed.	
17	ISET	External bias resistor to adjust the current of the amplifier.	
18	Vdd	Supply Voltage.	
19	FB	Feedback capacitance for the amplifier.	

Pin Number	Function	Description	Interface Schematic
11, 20	RFOUT, AMP IN	Amplifier input. External blocking capacitor required.	
21	ATT OUT	Attenuator output.	
22 - 24	FC1, FC2, FC3	External capacitors to ground are required. Place these capacitors close to the package.	

Application Circuit

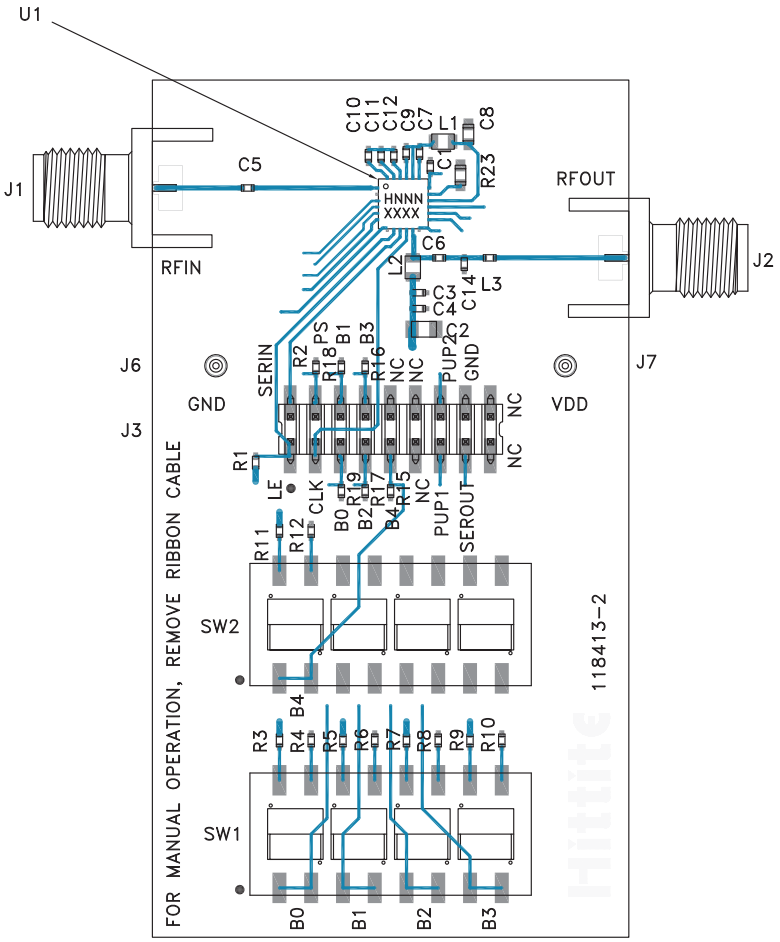


* Refer to Table X for values

Components For Selected Frequencies

Tuned Frequency	50 - 250 MHz	250 - 500 MHz	500 - 800 MHz
Evaluation Board P/N	118415	120101	120102
C6	1 nF	33 pF	33 pF
L3	0 Ohms	15 nH	12 nH
C14	N/A	4.7 pF	1.5 pF

Evaluation PCB



List of Materials for Evaluation PCB See Table[1]

Item	Description
J1, J2	PCB Mount SMA Connector
J3	18 Pin DC Connector
J6, J7	DC Pin
C1, C3	100 pF Capacitor, 0402 Pkg.
C2	4.7 µF Capacitor, 0805 Pkg.
C4	0.1 µF Capacitor, 0402 Pkg.
C6, C14	0402 Pkg.[1]
C5 - C7, C9 - C12	1000 pF Capacitor, 0402 Pkg.
C8	10 kpF Capacitor, 0805 Pkg.
R1 - R12	100 kOhm Resistor, 0402 Pkg.
R15 - R19	39 kOhm Resistor, 0402 Pkg.
R23	1.4 kOhm Resistor, 0603 Pkg.
L1, L2	270 nH Inductor, 0603 Pkg.
L3	0402 Pkg.[1]

Item	Description
SW1, SW2	SPDT 4 Position Dip Switch
U1	HMC628LP4(E) Variable Gain Amplifier
PCB [2]	118413 Evaluation PCB

[1] When requesting an evaluation board, please reference the appropriate PCB number listed in the table "Components for Selected Frequencies."

[2] Circuit Board Material: Arlon 25FR / FR4

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.