ADS7044 Ultra-Low Power, Ultra-Small Size, 12-Bit, 1-MSPS, SAR ADC

1 Features

- Industry's First SAR ADC with Nanowatt Power Consumption:
  - 261 µW at 1 MSPS with 1.8-V AVDD
  - 900 µW at 1 MSPS with 3-V AVDD
  - 90 µW at 100 kSPS with 3-V AVDD
  - Less than 1 µW at 1 kSPS with 3-V AVDD
- Industry's Smallest SAR ADC:
  - X2QFN-8 Package with 2.25-mm^2 Footprint
- 1-MSPS Throughput with Zero Data Latency
- Wide Operating Range:
  - AVDD: 1.65 V to 3.6 V
  - DVDD: 1.65 V to 3.6 V (Independent of AVDD)
  - Temperature Range: –40°C to 125°C
- Excellent Performance:
  - 12-Bit Resolution with NMC
  - ±1-LSB (Max) DNL and INL
  - 71-dB SNR with 3-V AVDD
  - –85-dB THD with 3-V AVDD
- Unipolar, Differential Input Range: –AVDD to AVDD
- Integrated Offset Calibration
- SPI™-Compatible Serial Interface: 16 MHz
- JESD8-7A Compliant Digital I/O

2 Applications

- Low-Power Data Acquisition
- Battery-Powered Handheld Equipment
- Level Sensors
- Ultrasonic Flow Meters
- Motor Controls
- Wearable Fitness
- Portable Medical Equipment
- Hard Drives
- Glucose Meters

3 Description

The ADS7044 is a 1-MSPS, analog-to-digital converter (ADC). The device supports a wide analog input voltage range (±1.65 V to ±3.6 V) and includes a capacitor-based, successive-approximation register (SAR) ADC with an inherent sample-and-hold circuit. The SPI-compatible serial interface is controlled by the $\overline{CS}$ and SCLK signals. The input signal is sampled with the $\overline{CS}$ falling edge and SCLK is used for conversion and serial data output. The device supports a wide digital supply range (1.65 V to 3.6 V), enabling direct interface to a variety of host controllers. The device complies with the JESD8-7A standard for normal DVDD range (1.65 V to 1.95 V).

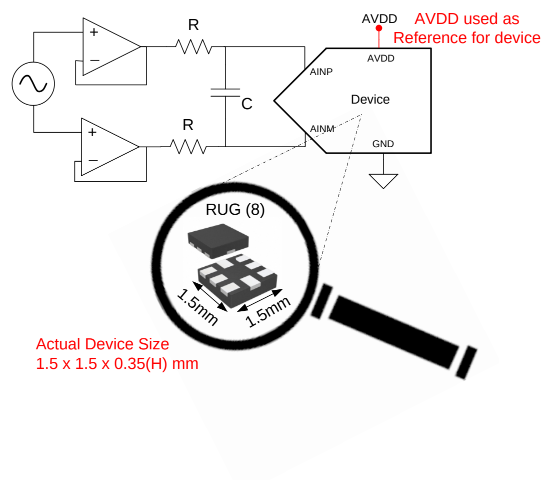
The device is available in 8-pin, miniature, leaded, and X2QFN packages and is specified for operation from –40°C to 125°C. Miniature form-factor and extremely low-power consumption make this device suitable for space-constrained, battery-powered applications.

Device Information(1)

PART NAME	PACKAGE	BODY SIZE (NOM)
ADS7044	X2QFN (8)	1.50 mm × 1.50 mm
	VSSOP (8)	2.30 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application



NOTE: The device is smaller than a 0805 (2012 metric) SMD component.

Table of Contents

1 **Features** 1
2 **Applications** 1
3 **Description** 1
4 **Revision History** 2
5 **Pin Configuration and Functions** 4
6 **Specifications** 5
  6.1 Absolute Maximum Ratings 5
  6.2 ESD Ratings 5
  6.3 Recommended Operating Conditions 5
  6.4 Thermal Information 5
  6.5 Electrical Characteristics 6
  6.6 Timing Characteristics 7
  6.7 Typical Characteristics 9
7 **Parameter Measurement Information** 14
  7.1 Digital Voltage Levels 14
8 **Detailed Description** 15
  8.1 Overview 15
  8.2 Functional Block Diagram 15
  8.3 Feature Description 16
  8.4 Device Functional Modes 20
9 **Application and Implementation** 23
  9.1 Application Information 23
  9.2 Typical Applications 23
10 **Power-Supply Recommendations** 29
  10.1 AVDD and DVDD Supply Recommendations 29
  10.2 Estimating Digital Power Consumption 29
  10.3 Optimizing Power Consumed by the Device 29
11 **Layout** 30
  11.1 Layout Guidelines 30
  11.2 Layout Example 30
12 **Device and Documentation Support** 31
  12.1 Documentation Support 31
  12.2 Community Resources 31
  12.3 Trademarks 31
  12.4 Electrostatic Discharge Caution 31
  12.5 Glossary 31
13 **Mechanical, Packaging, and Orderable Information** 31

4 Revision History

Changes from Revision C (February 2015) to Revision D	Page
• Changed Figure 1	8
• Changed *Serial Interface* section: changed last half of first paragraph, changed Figure 35	19
• Changed Figure 38	22
• Added *Community Resources* section	31

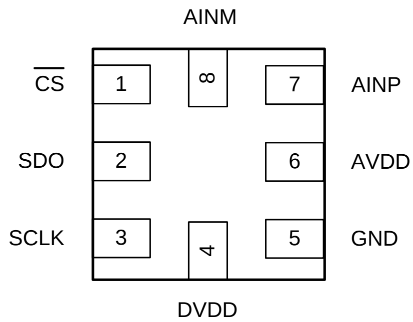
Changes from Revision B (December 2014) to Revision C	Page
• Changed *Wide Operating Range* Features bullet: changed the value of AVDD from 1.8 V to 1.65 V	1
• Changed the wide analog input voltage range value to ±1.65 V in first paragraph of Description section	1
• Changed AVDD parameter minimum specification in *Recommended Operating Conditions* table	5
• Changed E_O parameter uncalibrated test conditions in *Electrical Characteristics* table	6
• Changed *Maximum throughput rate* parameter test conditions in *Electrical Characteristics* table	6
• Changed *AVDD* parameter minimum specification in *Electrical Characteristics* table	7
• Changed conditions for *Timing Characteristics* table: changed range of AVDD and added C_{LOAD} condition	7
• Changed t_{D_CKDO} specification in *Timing Characteristics* table	7
• Added f_{SCLK} minimum specification to *Timing Characteristics* table	7
• Changed titles of Figure 26 to Figure 30	12
• Changed *Reference* sub-section in *Feature Description* section	16
• Changed AVDD range in description of $f_{CLK\text{-}CAL}$ parameter in Table 2	21
• Changed AVDD range in description of $f_{CLK\text{-}CAL}$ parameter in Table 3	22
• Changed *Reference Circuit* section in *Application Information*	25
• Added last two sentences to *AVDD and DVDD Supply Recommendations* section	29

Changes from Revision A (November 2014) to Revision B	Page
• Changed ESD Ratings table to latest standards	5
• Added footnote 3 to *Electrical Characteristics* table	6
• Changed y-axis unit in Figure 30	13

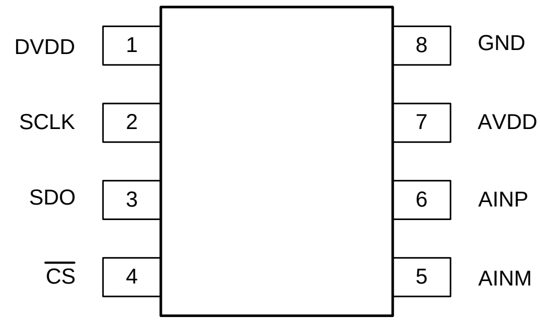
Changes from Original (November 2014) to Revision A	Page
• Made changes to product preview data sheet	1

5 Pin Configuration and Functions

RUG Package
8-Pin X2QFN
Top View



DCU Package
8-Pin Leaded VSSOP
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO. RUG	NO. DCU		
AINM	8	5	Analog input	Analog signal input, negative
AINP	7	6	Analog input	Analog signal input, positive
AVDD	6	7	Supply	Analog power-supply input, also provides the reference voltage to the ADC
$\overline{CS}$	1	4	Digital input	Chip-select signal, active low
DVDD	4	1	Supply	Digital I/O supply voltage
GND	5	8	Supply	Ground for power supply, all analog and digital signals are referred to this pin
SCLK	3	2	Digital input	Serial clock
SDO	2	3	Digital output	Serial data out

6 Specifications

6.1 Absolute Maximum Ratings(1)

	MIN	MAX	UNIT
AVDD to GND	–0.3	3.9	V
DVDD to GND	–0.3	3.9	V
AINP to GND	–0.3	AVDD + 0.3	V
AINM to GND	–0.3	AVDD + 0.3	V
Digital input voltage to GND	–0.3	DVDD + 0.3	V
Storage temperature, T_{stg}	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
AVDD	Analog supply voltage range	1.65	3.6	V
DVDD	Digital supply voltage range	1.65	3.6	V
T_A	Operating free-air temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		ADS7044		UNIT
		RUG (X2QFN)	DCU (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	177.5	235.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.5	79.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	76.7	117.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.0	8.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	76.7	116.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At T_A = –40°C to 125°C, AVDD = 3 V, DVDD = 1.65 V to 3.6 V, f_{SAMPLE} = 1 MSPS, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
	Full-scale input voltage span (1)		–AVDD		AVDD	V
	Absolute input voltage range: AINP to GND		–0.1		AVDD + 0.1	V
	Absolute input voltage range: AINM to GND		–0.1		AVDD + 0.1	V
C_S	Sampling capacitance			15		pF
SYSTEM PERFORMANCE						
	Resolution			12		Bits
NMC	No missing codes		12			Bits
INL	Integral nonlinearity	AVDD = 3 V	–1	±0.7	1	LSB (2)
		AVDD = 1.8 V	–2	±1	2	
DNL	Differential nonlinearity	AVDD = 3 V	–0.99	±0.5	1	LSB
		AVDD = 1.8 V	–0.99	±0.7	2	
E_O	Uncalibrated offset error	AVDD = 1.65 V to 3.6 V		±12		LSB
	Calibrated offset error (3)	AVDD = 3 V	–3	±0.5	3	
		AVDD = 1.8 V	–4	±1	4	
dV_{OS}/dT	Offset error drift with temperature			5		ppm/°C
E_G	Gain error	AVDD = 3 V	–0.1	±0.05	0.1	%FS
		AVDD = 1.8 V	–0.2	±0.1	0.2	
	Gain error drift with temperature			2		ppm/°C
CMRR	Common-mode rejection ratio	f_{IN} = 2 kHz, AVDD = 3 V		53		dB
SAMPLING DYNAMICS						
t_{ACQ}	Acquisition time		200			ns
	Maximum throughput rate	16-MHz SCLK, AVDD = 1.65 V to 3.6 V			1	MHz
DYNAMIC CHARACTERISTICS						
SNR	Signal-to-noise ratio (4)	f_{IN} = 2 kHz, AVDD = 3 V	70	71		dB
		f_{IN} = 2 kHz, AVDD = 1.8 V		70		
THD	Total harmonic distortion (4)(5)	f_{IN} = 2 kHz, AVDD = 3 V		–85		dB
SINAD	Signal-to-noise and distortion (4)	f_{IN} = 2 kHz, AVDD = 3 V	69.5	71		dB
		f_{IN} = 2 kHz, AVDD = 1.8 V		70		
SFDR	Spurious-free dynamic range (4)	f_{IN} = 2 kHz, AVDD = 3 V		85		dB
$BW_{(fp)}$	Full-power bandwidth	At –3 dB, AVDD = 3 V		25		MHz
DIGITAL INPUT/OUTPUT (CMOS Logic Family)						
V_{IH}	High-level input voltage (6)		0.65 DVDD		DVDD + 0.3	V
V_{IL}	Low-level input voltage (6)		–0.3		0.35 DVDD	V
V_{OH}	High-level output voltage (6)	At I_{source} = 500 µA	0.8 DVDD		DVDD	V
		At I_{source} = 2 mA	DVDD – 0.45		DVDD	
V_{OL}	Low-level output voltage (6)	At I_{sink} = 500 µA	0		0.2 DVDD	V
		At I_{sink} = 2 mA	0		0.45	

(1) Ideal input span; does not include gain or offset error.
(2) LSB means least significant bit.
(3) Refer to the *Offset Calibration* section for more details.
(4) All specifications expressed in decibels (dB) refer to the full-scale input (FSR) and are tested with an input signal 0.5 dB below full-scale, unless otherwise specified.
(5) Calculated on the first nine harmonics of the input frequency.
(6) Digital voltage levels comply with the JESD8-7A standard for DVDD from 1.65 V to 1.95 V. See the *Digital Voltage Levels* section for more details.

Electrical Characteristics (continued)

At T_A = –40°C to 125°C, AVDD = 3 V, DVDD = 1.65 V to 3.6 V, f_{SAMPLE} = 1 MSPS, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER-SUPPLY REQUIREMENTS						
AVDD	Analog supply voltage		1.65	3	3.6	V
DVDD	Digital I/O supply voltage		1.65	3	3.6	V
I_{AVDD}	Analog supply current	At 1 MSPS with AVDD = 3 V			300	µA
		At 100 kSPS with AVDD = 3 V			30	
		At 1 MSPS with AVDD = 1.8 V		145		
P_D	Power dissipation	At 1 MSPS with AVDD = 3 V			900	µW
		At 100 kSPS with AVDD = 3 V			90	
		At 1 MSPS with AVDD = 1.8 V		261		

6.6 Timing Characteristics

All specifications are at T_A = –40°C to 125°C, AVDD = 1.65 V to 3.6 V, DVDD = 1.65 V to 3.6 V, and C_{LOAD} on SDO = 20 pF, unless otherwise specified.

		MIN	TYP	MAX	UNIT
TIMING SPECIFICATIONS					
$f_{THROUGHPUT}$	Throughput			1	MSPS
t_{CYCLE}	Cycle time	1			µs
t_{CONV}	Conversion time			12.5 × t_{SCLK} + t_{SU_CSCK}	ns
t_{DV_CSDO}	Delay time: $\overline{CS}$ falling to data enable			10	ns
t_{D_CKDO}	Delay time: SCLK falling to (next) data valid on DOUT, AVDD = 1.8 V to 3.6 V			30	ns
	Delay time: SCLK falling to (next) data valid on DOUT, AVDD = 1.65 V to 1.8 V			50	
t_{DZ_CSDO}	Delay time: $\overline{CS}$ rising to DOUT going to 3-state	5			ns
TIMING REQUIREMENTS					
t_{ACQ}	Acquisition time	200			ns
f_{SCLK}	SCLK frequency	0.016		16	MHz
t_{SCLK}	SCLK period	62.5			ns
t_{PH_CK}	SCLK high time	0.45		0.55	t_{SCLK}
t_{PL_CK}	SCLK low time	0.45		0.55	t_{SCLK}
t_{PH_CS}	$\overline{CS}$ high time	60			ns
t_{SU_CSCK}	Setup time: $\overline{CS}$ falling to SCLK falling	15			ns
t_{D_CKCS}	Delay time: last SCLK falling to $\overline{CS}$ rising	10			ns

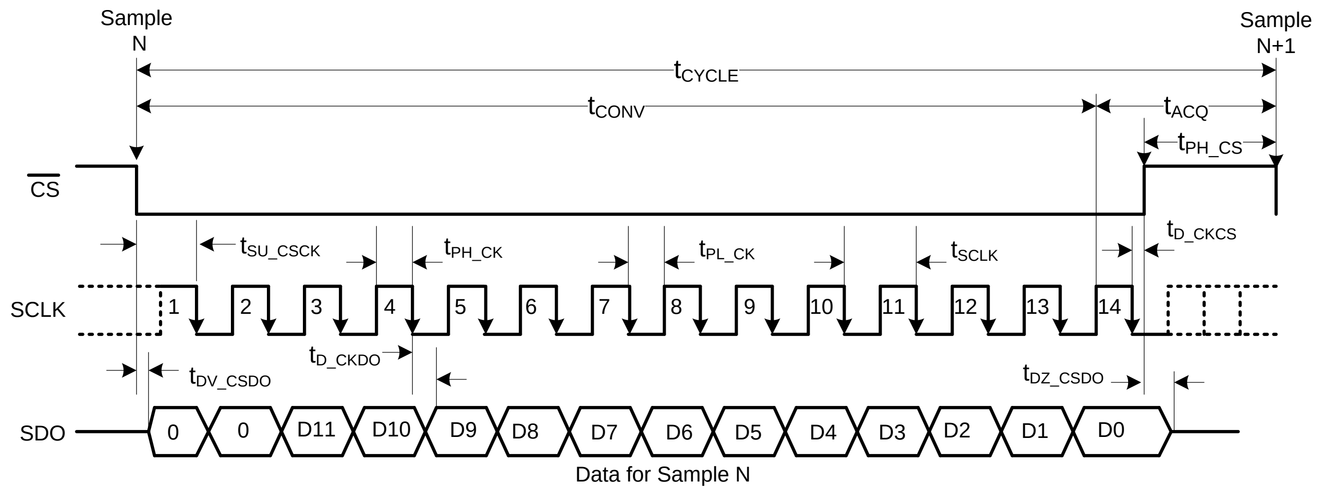
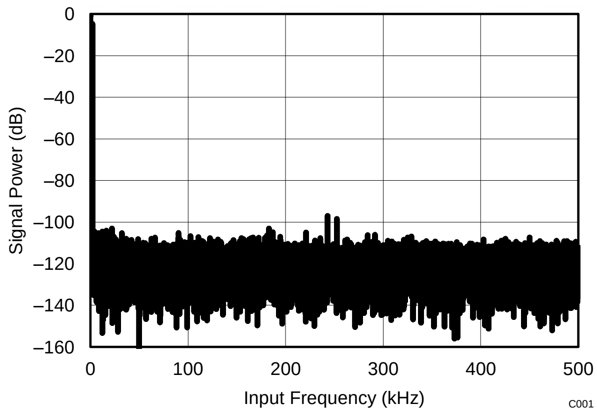


Figure 1. Timing Diagram

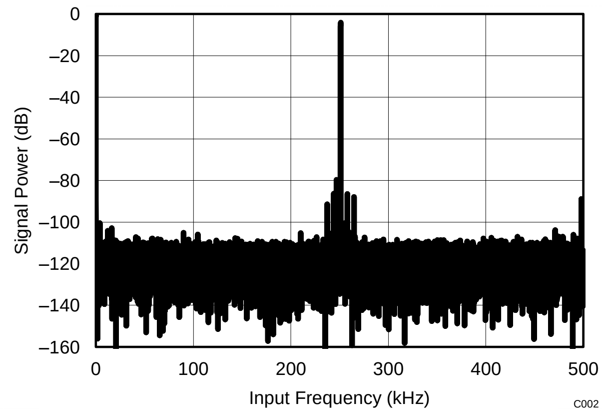
6.7 Typical Characteristics

At T_A = 25°C, AVDD = 3 V, DVDD = 1.8 V, and f_{SAMPLE} = 1 MSPS, unless otherwise noted.



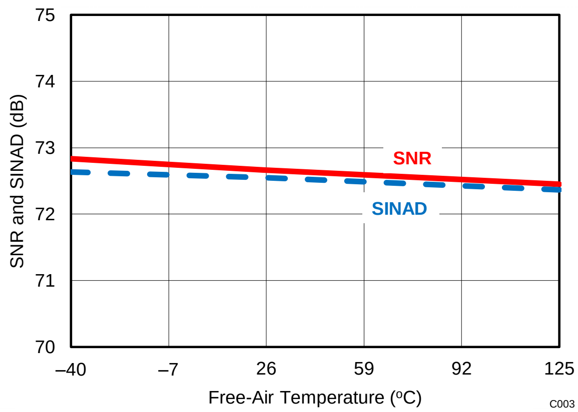
SNR = 72.58 dB THD = –93 dB f_{IN} = 2 kHz
Number of samples = 32768

Figure 2. Typical FFT



SNR = 71.95 dB THD = –76.5 dB f_{IN} = 250 kHz
Number of samples = 32768

Figure 3. Typical FFT



f_{IN} = 2 kHz

Figure 4. SNR and SINAD vs Temperature

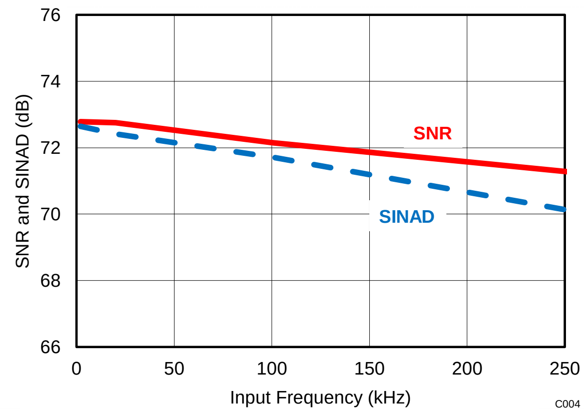


Figure 5. SNR and SINAD vs Input Frequency

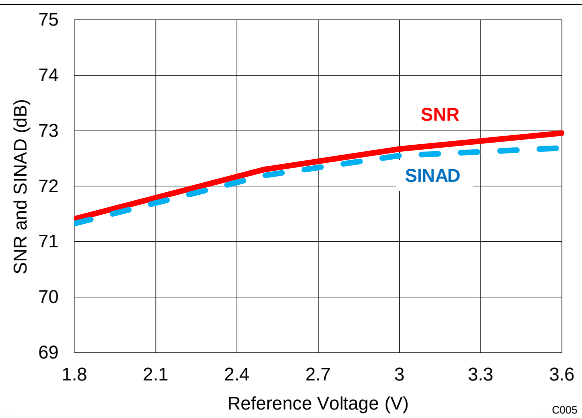


Figure 6. SNR and SINAD vs Reference Voltage (AVDD)

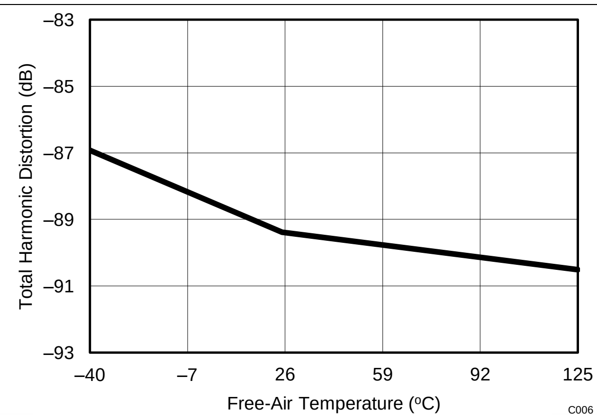


Figure 7. THD vs Free-Air Temperature

Typical Characteristics (continued)

At T_A = 25°C, AVDD = 3 V, DVDD = 1.8 V, and f_{SAMPLE} = 1 MSPS, unless otherwise noted.

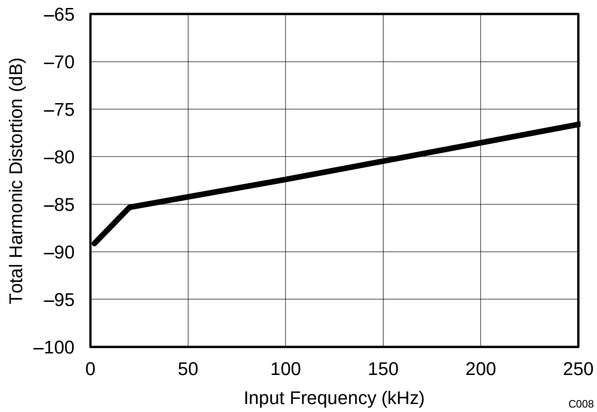


Figure 8. THD vs Input Frequency

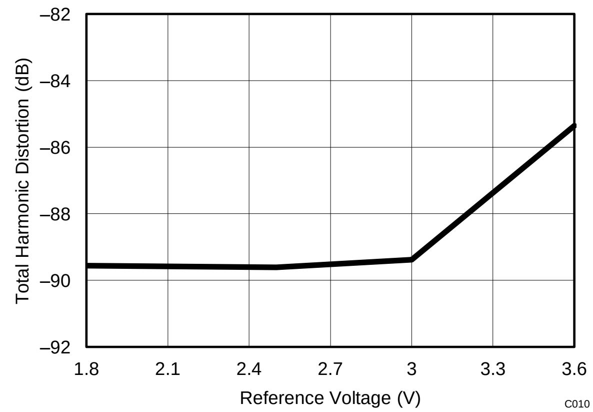


Figure 9. THD vs Reference Voltage (AVDD)

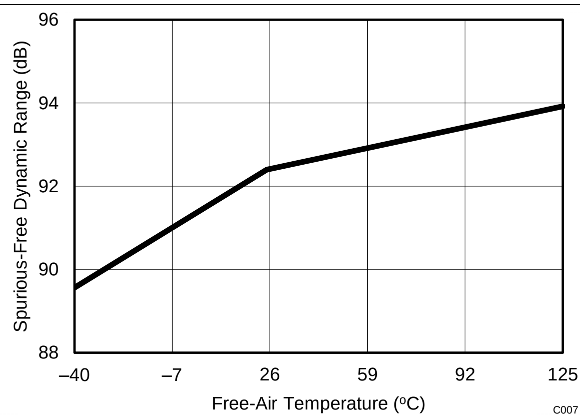


Figure 10. SFDR vs Free-Air Temperature

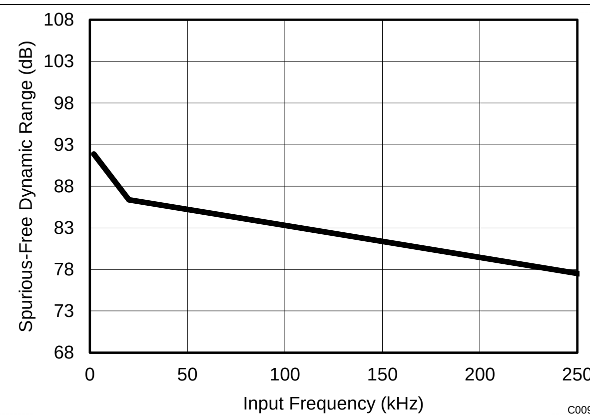


Figure 11. SFDR vs Input Frequency

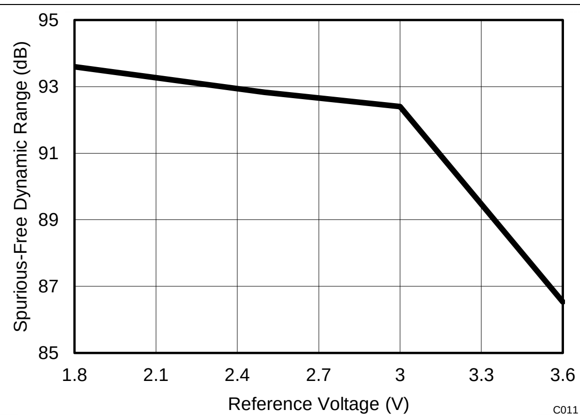
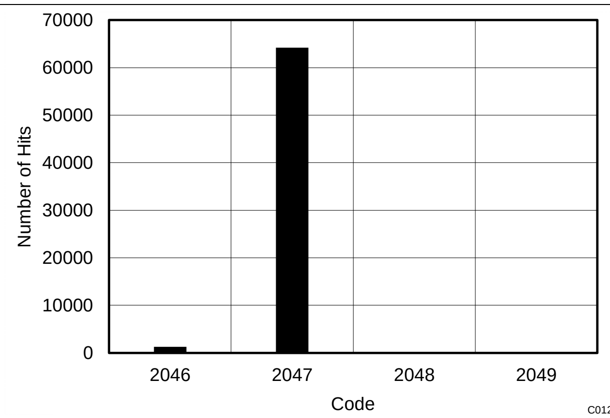


Figure 12. SFDR vs Reference Voltage (AVDD)



Mean code = 2046.98 Sigma = 0.14

Figure 13. DC Input Histogram

Typical Characteristics (continued)

At T_A = 25°C, AVDD = 3 V, DVDD = 1.8 V, and f_{SAMPLE} = 1 MSPS, unless otherwise noted.

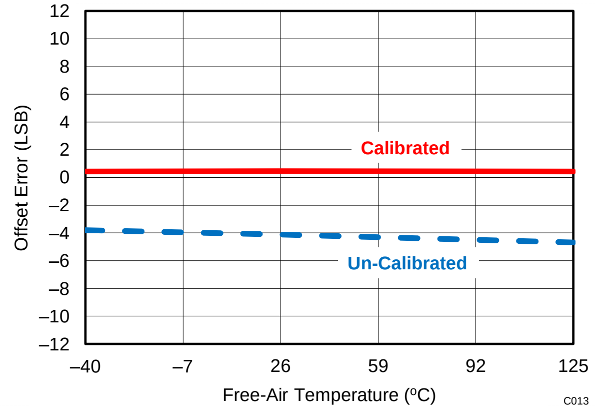


Figure 14. Offset vs Free-Air Temperature

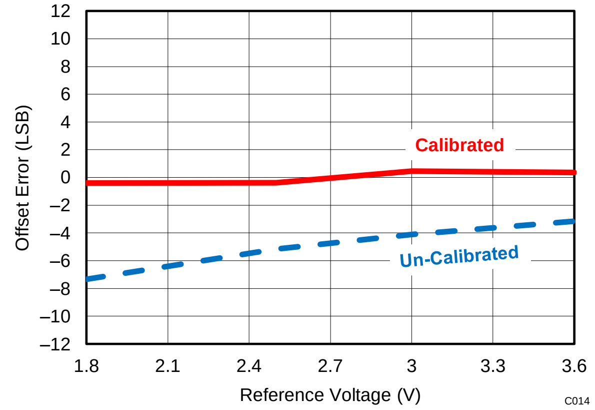


Figure 15. Offset vs Reference Voltage (AVDD)

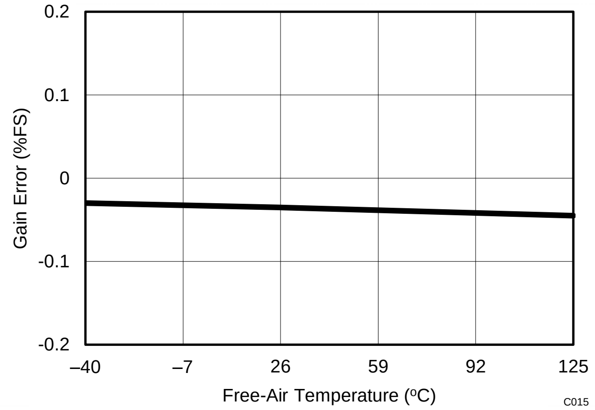


Figure 16. Gain Error vs Free-Air Temperature

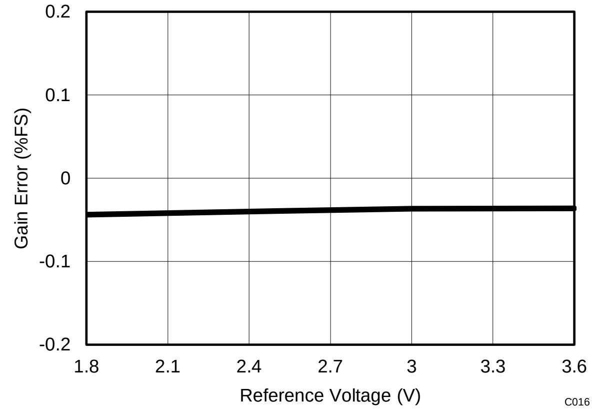
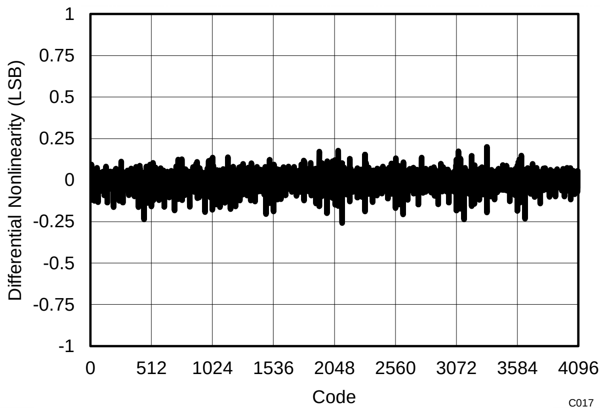
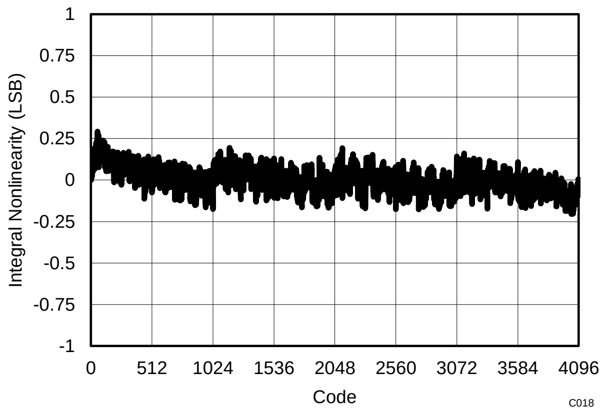


Figure 17. Gain Error vs Reference Voltage (AVDD)



AVDD = 3 V

Figure 18. Typical DNL

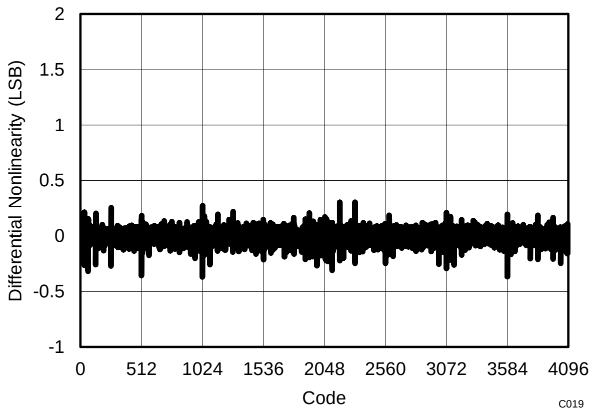


AVDD = 3 V

Figure 19. Typical INL

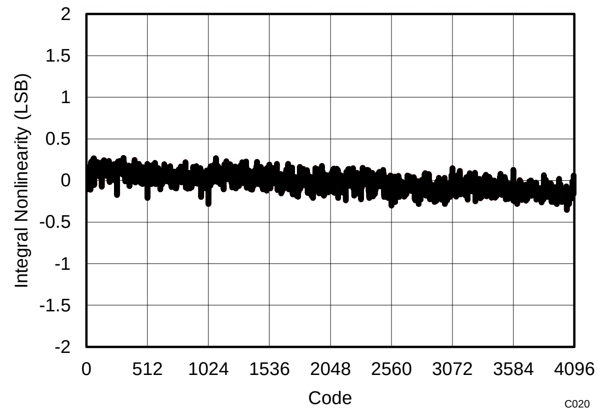
Typical Characteristics (continued)

At T_A = 25°C, AVDD = 3 V, DVDD = 1.8 V, and f_{SAMPLE} = 1 MSPS, unless otherwise noted.



AVDD = 1.8 V

Figure 20. Typical DNL



AVDD = 1.8 V

Figure 21. Typical INL

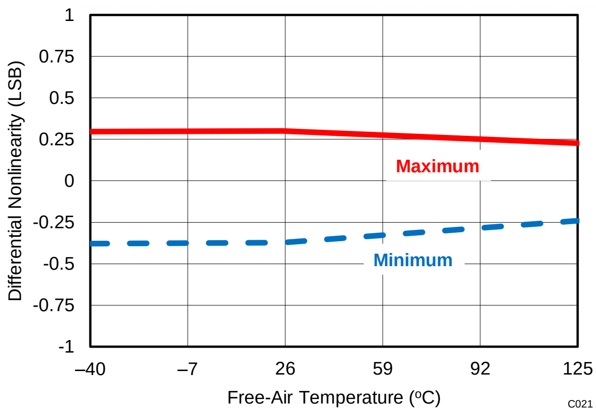


Figure 22. DNL vs Free-Air-Temperature

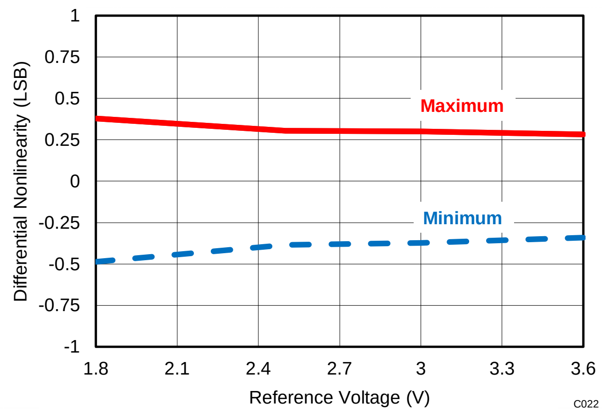


Figure 23. DNL vs Reference Voltage (AVDD)

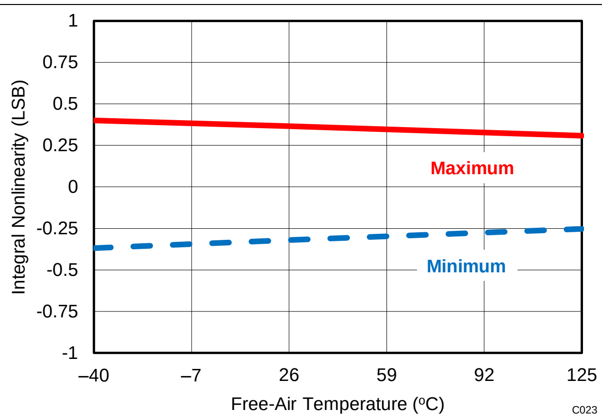


Figure 24. INL vs Free-Air Temperature

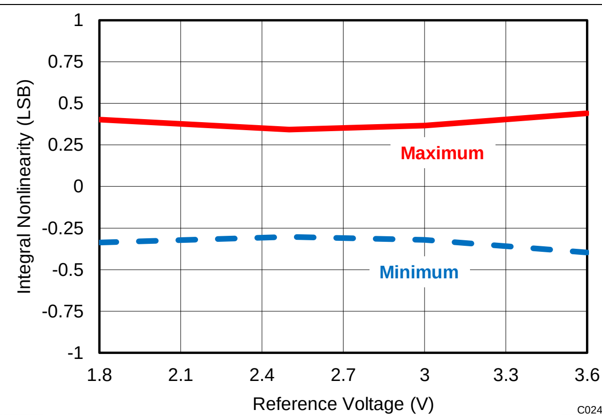


Figure 25. INL vs Reference Voltage (AVDD)

Typical Characteristics (continued)

At T_A = 25°C, AVDD = 3 V, DVDD = 1.8 V, and f_{SAMPLE} = 1 MSPS, unless otherwise noted.

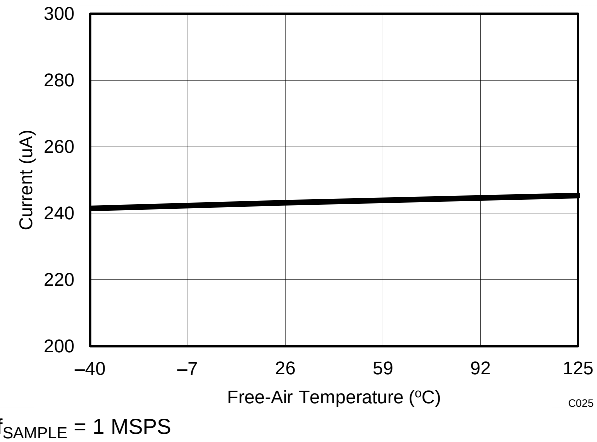


Figure 26. AVDD Supply Current vs Free-Air Temperature

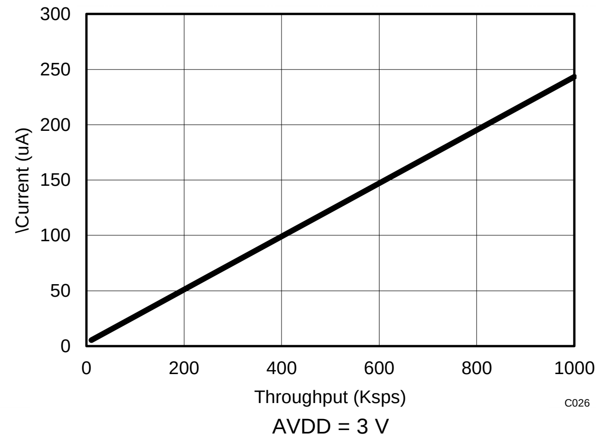


Figure 27. AVDD Supply Current vs Throughput

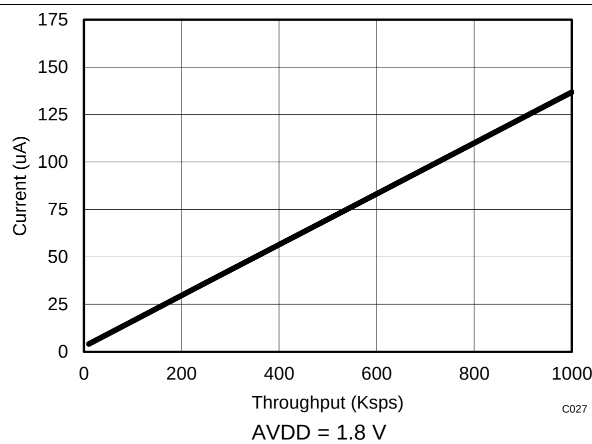


Figure 28. AVDD Supply Current vs Throughput

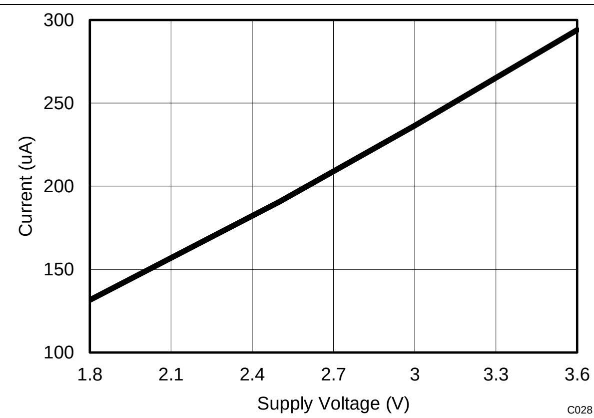


Figure 29. AVDD Supply Current vs AVDD Voltage

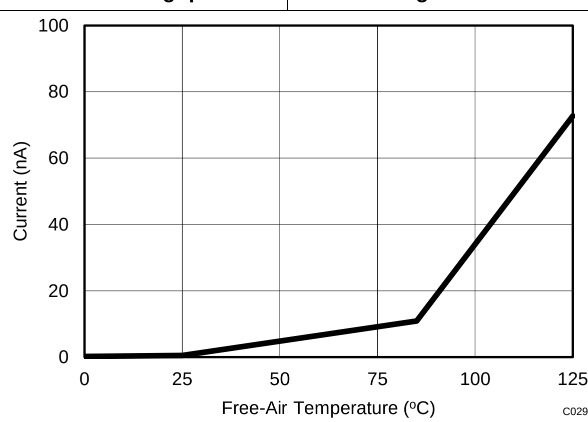


Figure 30. AVDD Static Current vs Free-Air Temperature

7 Parameter Measurement Information

7.1 Digital Voltage Levels

The device complies with the JESD8-7A standard for DVDD from 1.65 V to 1.95 V. Figure 31 shows voltage levels for the digital input and output pins.

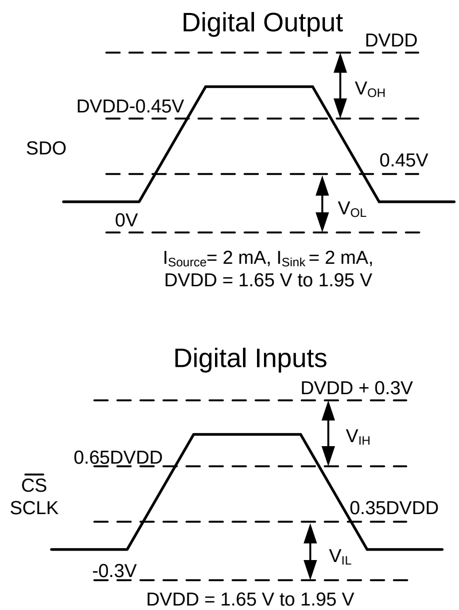


Figure 31. Digital Voltage Levels as per the JESD8-7A Standard

8 Detailed Description

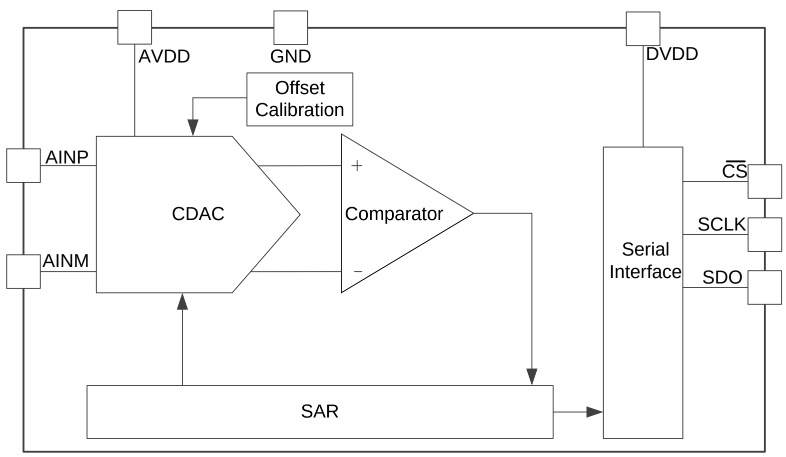
8.1 Overview

The ADS7044 is an ultralow-power, ultra-small analog-to-digital converter (ADC) that supports a wide analog input range. The analog input range for the device is defined by the AVDD supply voltage. The device samples the input voltage across the AINP and AINM pins on the $\overline{\text{CS}}$ falling edge and starts the conversion. The clock provided on the SCLK pin is used for conversion and data transfer. During conversions, both the AINP and AINM pins are disconnected from the sampling circuit. After the conversion completes, the sampling capacitors are reconnected across the AINP and AINM pins and the device enters acquisition phase.

The device has an internal offset calibration. The offset calibration can be initiated by the user either on power-up or during normal operation; see the *Offset Calibration* section for more details.

The device also provides a simple serial interface to the host controller and operates over a wide range of digital power supplies. The device requires only a 16-MHz SCLK for supporting a throughput of 1 MSPS. The digital interface also complies with the JESD8-7A (normal range) standard. The *Functional Block Diagram* section provides a block diagram of the device.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Reference

The device uses the analog supply voltage (AVDD) as a reference, as shown in Figure 32. TI recommends decoupling the AVDD pin with a 1-µF, low equivalent series resistance (ESR) ceramic capacitor. The minimum capacitor value required for AVDD is 200 nF. The AVDD pin functions as a switched capacitor load to the source powering AVDD. The decoupling capacitor provides the instantaneous charge required by the internal circuit and helps in maintaining a stable dc voltage on the AVDD pin. TI recommends powering the AVDD pin with a low output impedance and low-noise regulator (such as the TPS79101).

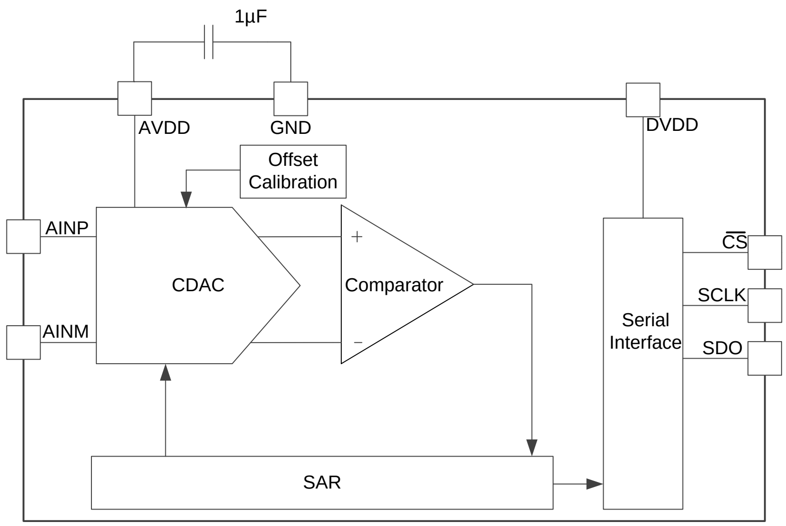


Figure 32. Reference for the Device

Feature Description (continued)

8.3.2 Analog Input

The device supports differential analog inputs. The ADC samples the difference between AINP and AINM and converts for this voltage. The device is capable of accepting a signal from 0 V to AVDD on the AINM input and a signal from 0 V to AVDD on the AINP input. Figure 33 represents the equivalent analog input circuits for the sampling stage. The device has a low-pass filter followed by the sampling switch and sampling capacitor. The sampling switch is represented by an R_S (typically 50 Ω) resistor in series with an ideal switch and C_S (typically 15 pF) is the sampling capacitor. The ESD diodes are connected from both analog inputs to AVDD and ground.

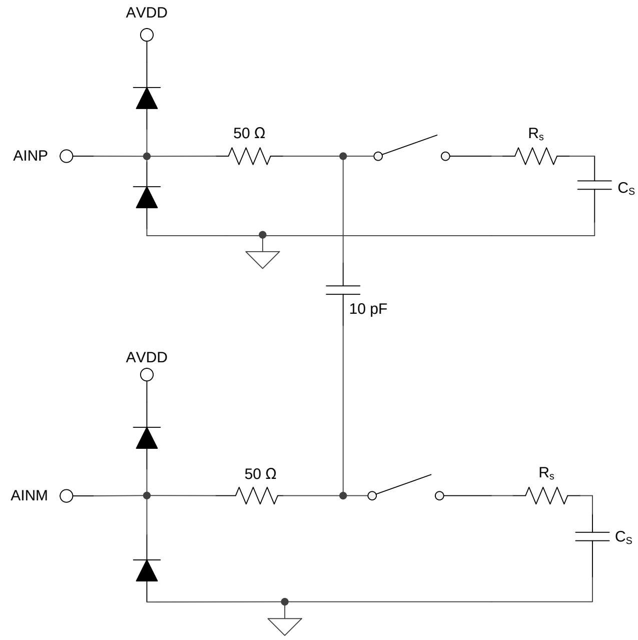


Figure 33. Equivalent Input Circuit for the Sampling Stage

The analog input full-scale range (FSR) is defined by the reference voltage of the ADC. The relationship between the FSR and the reference voltage can be determined by: FSR = 2 × V_{REF} = 2 × AVDD.

8.3.3 ADC Transfer Function

The device output is in twos compliment format. The device resolution can be computed by Equation 1:

$$1 \text{ LSB} = \text{FSR} / 2^N$$

where:

- FSR = 2 × V_{REF} = 2 × AVDD and
- N = 12 (1)

Feature Description (continued)

Figure 34 and Table 1 show the ideal transfer characteristics for the device.

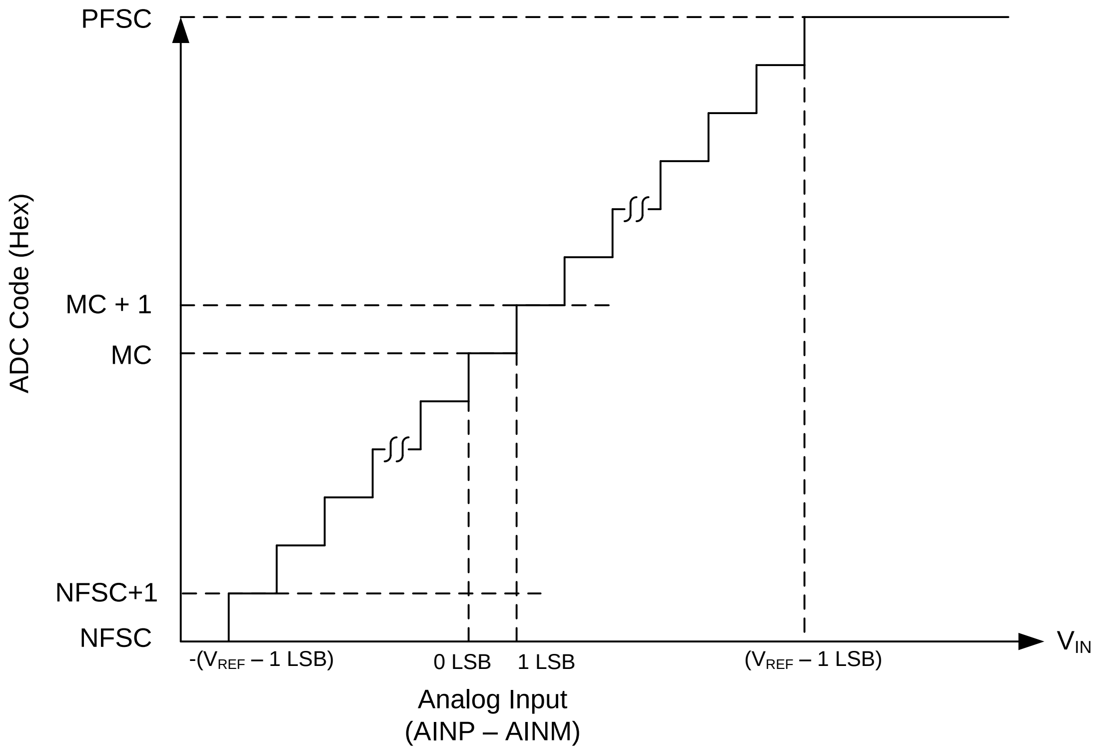


Figure 34. Ideal Transfer Characteristics

Table 1. Transfer Characteristics

INPUT VOLTAGE (AINP-AINM)	CODE	DESCRIPTION	IDEAL OUTPUT CODE
≤ –(V_{REF} – 1 LSB)	NFSC	Negative full-scale code	800
–(V_{REF} – 1 LSB) to –(V_{REF} – 2 LSBs)	NFSC + 1	—	801
0 to 1 LSB	MC	Mid code	000
1 LSB to 2 LSBs	MC + 1	—	001
≥V_{REF} – 1 LSB	PFSC	Positive full-scale code	7FF

8.3.4 Serial Interface

The device supports a simple, SPI-compatible interface to the external host. The $\overline{CS}$ signal defines one conversion and serial transfer frame. A frame starts with a $\overline{CS}$ falling edge and ends with a $\overline{CS}$ rising edge. The SDO pin outputs the ADC conversion results. Figure 35 shows a detailed timing diagram for the serial interface. A minimum delay of t_{SU_CSCK} must elapse between the $\overline{CS}$ falling edge and the first SCLK falling edge. The device uses the clock provided on the SCLK pin for conversion and data transfer. The conversion result is available on the SDO pin with the first two bits set to 0, followed by 12 bits of the conversion result. The first zero is launched on the SDO pin on the $\overline{CS}$ falling edge. Subsequent bits (starting with another 0 followed by the conversion result) are launched on the SDO pin on subsequent SCLK falling edges. The SDO output remains low after 14 SCLKs. A $\overline{CS}$ rising edge ends the frame and brings the serial data bus to 3-state. For the acquisition of the next sample, a minimum time of t_{ACQ} must be provided after the conversion of the current sample is completed. For details on timing specifications, see the *Timing Characteristics* table.

The device initiates offset calibration on first $\overline{CS}$ falling edge after power-up and the SDO output remains low during the first serial transfer frame after power-up. For details, refer to the *Offset Calibration* section.

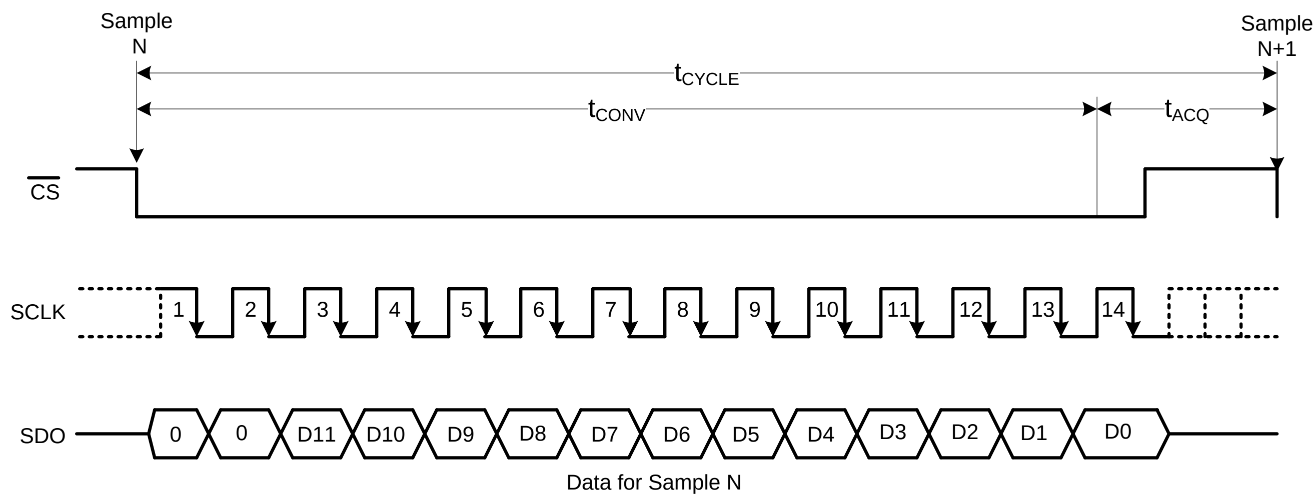


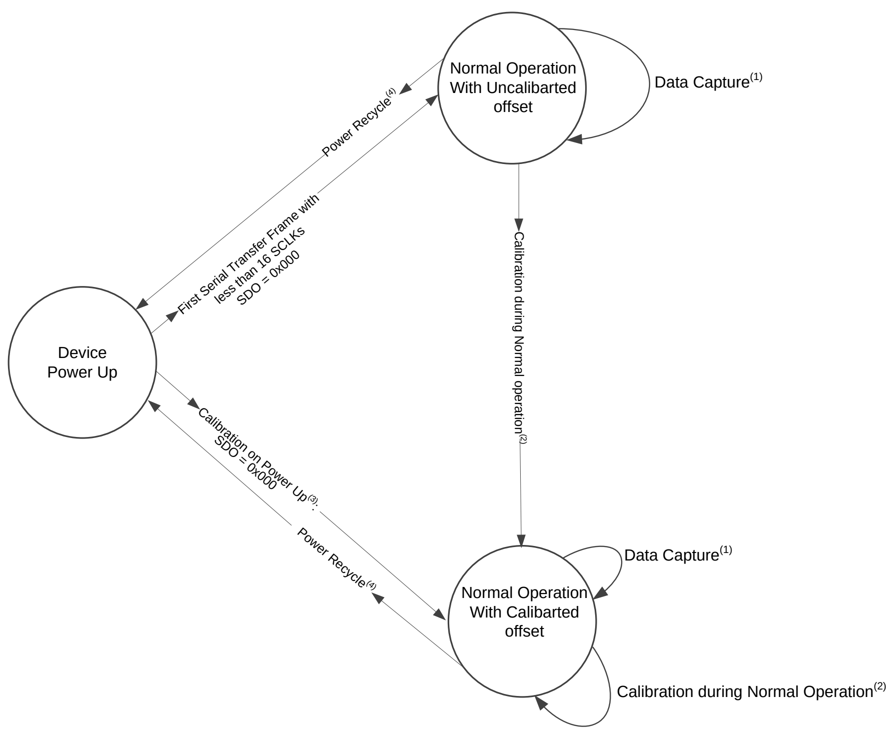
Figure 35. Serial Interface Timing Diagram

8.4 Device Functional Modes

8.4.1 Offset Calibration

The device includes a feature to calibrate its internal offset. The device initiates offset calibration on the first $\overline{CS}$ falling edge after power up and during offset calibration, the analog input pins (AINP and AINM) are disconnected from the sampling stage. After the first serial transfer frame, the device starts operating with either uncalibrated or calibrated offset, depending on the number of SCLKs provided in the first serial transfer frame. Offset calibration can also be initiated by the user during normal operation. Figure 36 shows the offset calibration process. The SDO output remains low during the first serial transfer frame.

The device includes an internal offset calibration register (OCR) that stores the offset calibration result. The OCR is an internal register and cannot be accessed by the user through the serial interface. The OCR is reset to zero on power-up. Therefore, TI recommends calibrating the offset on power-up to bring the offset within the specified limits. If there is a significant change in operating temperature or analog supply voltage, the offset can be recalibrated during normal operation.



(1) See the *Timing Characteristics* section for timing specifications.
(2) See the *Offset Calibration During Normal Operation* section for details.
(3) See the *Offset Calibration on Power-Up* section for details.
(4) The power recycle on the AVDD supply is required to reset the offset calibration and to bring the device to a power-up state.

Figure 36. Offset Calibration

Device Functional Modes (continued)

8.4.1.1 Offset Calibration on Power-Up

The device starts offset calibration on the first $\overline{CS}$ falling edge after power-up and calibration completes if the $\overline{CS}$ pin remains low for at least 16 SCLKs after the first $\overline{CS}$ falling edge. The SDO output remains low during calibration. The minimum acquisition time must be provided after calibration for acquiring the first sample. If the device is not provided with at least 16 SCLKs during the first serial transfer frame after power-up, the OCR is not updated. Table 2 provides the timing parameters for offset calibration on power-up.

For subsequent samples, the device adjusts the conversion results with the value stored in the OCR. The conversion result adjusted with the value stored in OCR is provided by the device on the SDO output. Figure 37 shows the timing diagram for offset calibration on power-up.

Table 2. Offset Calibration on Power-Up

		MIN	TYP	MAX	UNIT
$f_{CLK-CAL}$	SCLK frequency for calibration at 2.25 V < AVDD < 3.6 V			16	MHz
$f_{CLK-CAL}$	SCLK frequency for calibration at 1.65 V < AVDD < 2.25 V			12	MHz
$t_{POWERUP-CAL}$	Calibration time at power-up	16 t_{SCLK}			ns
t_{ACQ}	Acquisition time	200			ns
t_{PH_CS}	$\overline{CS}$ high time	t_{ACQ}			ns

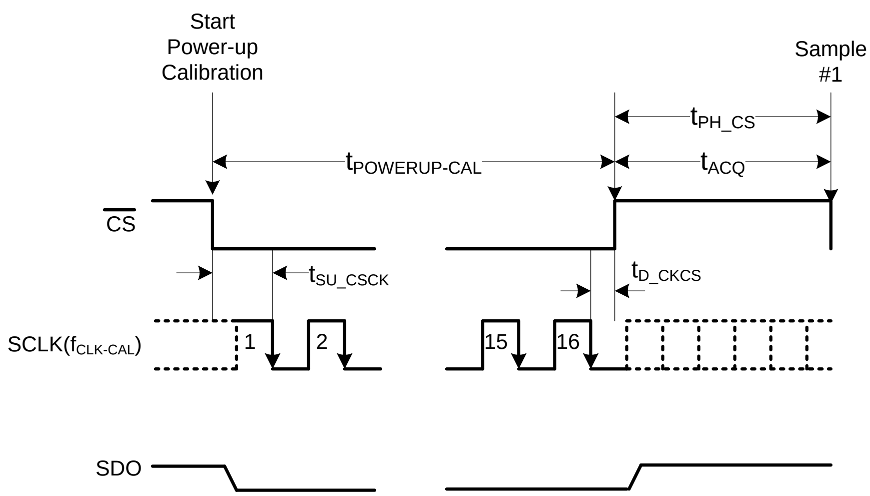


Figure 37. Offset Calibration on Power-Up Timing Diagram

8.4.1.2 Offset Calibration During Normal Operation

The offset can also be calibrated during normal device operation. Offset calibration can be done during normal device operation if at least 32 SCLKs are provided in one serial transfer frame. During the first 14 SCLKs, the device converts the sample acquired on the $\overline{CS}$ falling edge and provides data on the SDO output. The device initiates the offset calibration on the 17th SCLK falling edge and calibration is completed on the 32nd SCLK falling edge. The SDO output remains low after the 14th SCLK falling edge and SDO goes to 3-state after $\overline{CS}$ goes high. If the device is provided with less than 32 SCLKs during a serial transfer frame, the OCR is not updated. Table 3 provides the timing parameters for offset calibration during normal operation.

For subsequent samples, the device adjusts the conversion results with the value stored in OCR. The conversion result adjusted with the value stored in the OCR is provided by the device on the SDO output. Figure 38 shows the timing diagram for offset calibration during normal operation.

Table 3. Offset Calibration During Normal Operation

		MIN	TYP	MAX	UNIT
$f_{CLK-CAL}$	SCLK frequency for calibration for 2.25 V < AVDD < 3.6 V			16	MHz
$f_{CLK-CAL}$	SCLK frequency for calibration for 1.65 V < AVDD < 2.25 V			12	MHz
t_{CAL}	Calibration time during normal operation	16 t_{SCLK}			ns
t_{ACQ}	Acquisition time	200			ns
t_{PH_CS}	$\overline{CS}$ high time	t_{ACQ}			ns

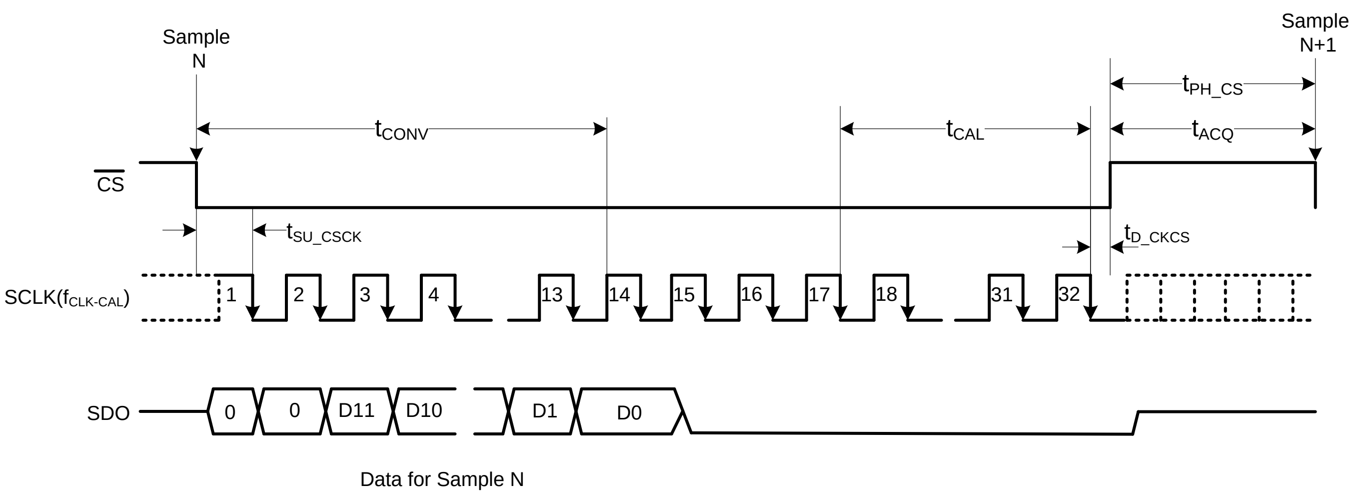


Figure 38. Offset Calibration During Normal Operation Timing Diagram

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The two primary circuits required to maximize the performance of a high-precision, successive approximation register (SAR), analog-to-digital converter (ADC) are the input driver and the reference driver circuits. This section details some general principles for designing the input driver circuit, reference driver circuit, and provides some application circuits designed for the ADS7044.

9.2 Typical Applications

9.2.1 Single-Supply DAQ with the ADS7044

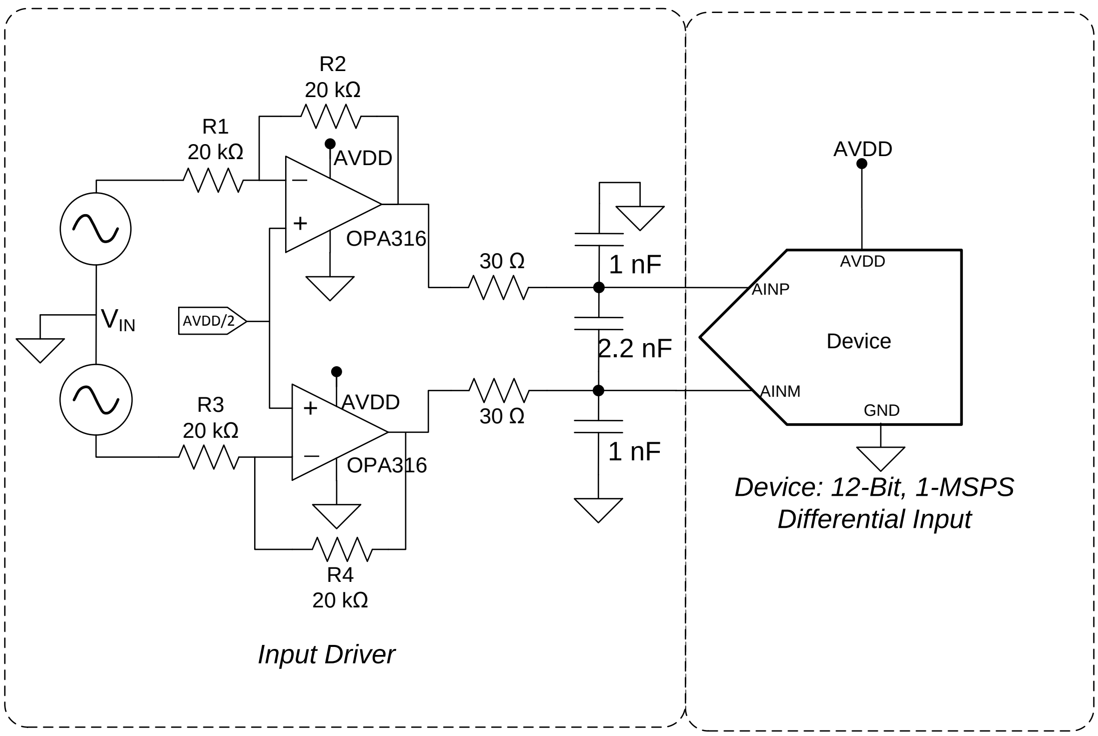


Figure 39. DAQ Circuit: Single-Supply DAQ

9.2.1.1 Design Requirements

The goal of this application is to design a single-supply digital acquisition (DAQ) circuit based on the ADS7044 with SNR greater than 71 dB and THD less than –85 dB for a differential input signal having an amplitude of AVDD with a common-mode voltage of AVDD / 2 and input frequencies of 5 kHz at a throughput of 1 MSPS.

9.2.1.2 Detailed Design Procedure

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and an antialiasing filter. Careful design of the front-end circuit is critical to meet the linearity and noise performance of a high-precision ADC.

Typical Applications (continued)

9.2.1.2.1 Antialiasing Filter

Converting analog-to-digital signals requires sampling an input signal at a rate greater than or equal to the Nyquist rate. Any higher frequency content in the input signal beyond half the sampling frequency is digitized and folded back into the low-frequency spectrum. This process is called *aliasing*. Therefore, an external, antialiasing filter must be used to remove the harmonic content from the input signal before being sampled by the ADC. An antialiasing filter is designed as a low-pass RC filter, for which the 3-dB bandwidth is optimized for noise, response time, and throughput. For dc signals with fast transients (including multiplexed input signals), a high-bandwidth filter is designed to allow the signal to be accurately set at the ADC inputs during the small acquisition time window. Figure 40 provides the equation for determining the bandwidth of antialiasing filter.

$$f_{-3dB} = \frac{1}{2\pi \times 2R_{FLT} \times C_{FLT}}$$

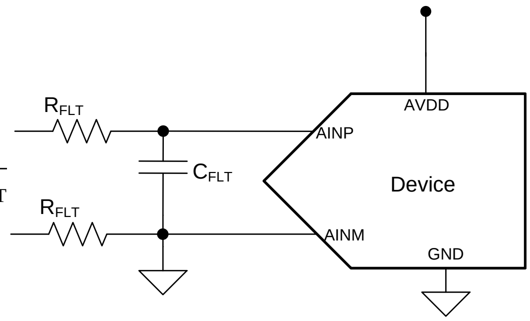


Figure 40. Antialiasing Filter

For ac signals, the filter bandwidth must be kept low to band limit the noise fed into the ADC input, thereby increasing the signal-to-noise ratio (SNR) of the system. Besides filtering the noise from the front-end drive circuitry, the RC filter also helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC. A filter capacitor, C_{FLT}, is connected across the ADC inputs. This capacitor helps reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. As a rule of thumb, the value of this capacitor must be at least 20 times the specified value of the ADC sampling capacitance. For this device, the input sampling capacitance is equal to 15 pF. Thus, the value of C_{FLT} must be greater than 300 pF. The capacitor must be a COG- or NPO-type because these capacitor types have a high-Q, low-temperature coefficient, and stable electrical characteristics under varying voltages, frequency, and time.

Note that driving capacitive loads can degrade the phase margin of the input amplifiers, thus making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors (R_{FLT}) are used at the output of the amplifiers. A higher value of R_{FLT} is helpful from the amplifier stability perspective, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of R_{FLT} requires balancing the stability and distortion of the design.

The input amplifier bandwidth must be much higher than the cutoff frequency of the antialiasing filter. TI strongly recommends performing a SPICE simulation to confirm that the amplifier has more than 40° phase margin with the selected filter. Simulation is critical because even with high-bandwidth amplifiers, some amplifiers may require more bandwidth than others to drive similar filters.

Typical Applications (continued)

9.2.1.2.2 Input Amplifier Selection

Selection criteria for the input amplifiers is highly dependent on the input signal type and the performance goals of the data acquisition system. Some key amplifier specifications to consider while selecting an appropriate amplifier to drive the inputs of the ADC are:

- Small-signal bandwidth: Select the small-signal bandwidth of the input amplifiers to be high enough to settle the input signal in the acquisition time of the ADC. Higher bandwidth reduces the closed-loop output impedance of the amplifier, thus allowing the amplifier to more easily drive the low cutoff frequency RC filter at the ADC inputs. Higher bandwidth also minimizes the harmonic distortion at higher input frequencies. In order to maintain the overall stability of the input driver circuit, select the amplifier bandwidth as described in Equation 2:

$$\mathrm{GBW} \geq 4 \times \frac{1}{2\pi \times 2R_{FLT} \times C_{FLT}}$$

  where:
  - GBW = Unity-gain bandwidth (2)

- Noise: Noise contribution of the front-end amplifiers must be low enough to prevent any degradation in SNR performance of the system. As a rule of thumb, to ensure that the noise performance of the data acquisition system is not limited by the front-end circuit, keep the total noise contribution from the front-end circuit below 20% of the input-referred noise of the ADC. Noise from the input driver circuit is band limited by designing a low cutoff frequency RC filter, as explained in Equation 3.

$$\sqrt{\left(\frac{V_{1/f\_AMP\_PP}}{6.6 \times 2\beta}\right)^2 + \left[\frac{\left(2 \times e_{n\_RMS}\right)^2 + \left(\left(2 \times i_n \times \beta\right)^2 \times \left(R_2^2 + R_4^2\right)\right) + \left(\left(2 \times \sqrt{4kT} \times (1-\beta)\right)^2 \times \left(R_1 + R_3\right)\right)}{(2\beta)^2} + 4kT\left(R_2 + R_4\right)\right] \times \frac{\pi}{2} \times f_{-3dB}} \leq \frac{1}{5} \times \frac{V_{REF}}{\sqrt{2}} \times 10^{-\left(\frac{SNR(dB)}{20}\right)}$$

  where:
  - V_{1/f_AMP_PP} is the peak-to-peak flicker noise in µVrms,
  - e_{n_RMS} is the amplifier broadband noise,
  - f_{-3dB} is the –3-dB bandwidth of the RC filter,
  - k is the Boltzmann's constant, and
  - T is absolute temperature in kelvin.
  - For symmetrical feedback, β = R1 / (R1 + R2) = R3 / (R3 + R4).
  - For details on noise analysis, refer to the technical brief *Analysis of fully differential amplifiers* (SLYT157) (3)

- Settling time: For dc signals with fast transients that are common in a multiplexed application, the input signal must settle to the desired accuracy at the inputs of the ADC during the acquisition time window. This condition is critical to maintain the overall linearity performance of the ADC. Typically, the amplifier data sheets specify the output settling performance only up to 0.1% to 0.001%, which may not be sufficient for the desired accuracy. Therefore, always verify the settling behavior of the input driver with TINA™-SPICE simulations before selecting the amplifier.

The OPA316 is selected for this application for its rail-to-rail input and output swing, low-noise (11 nV/√Hz), and low-power (400 µA) performance to support a single-supply data acquisition circuit.

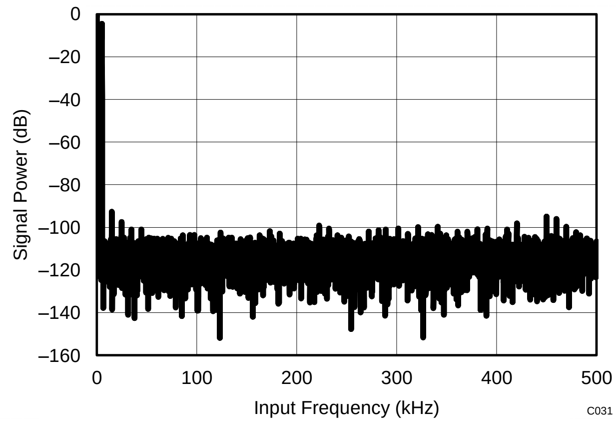
9.2.1.2.3 Reference Circuit

The analog supply voltage of the device is also used as a voltage reference for conversion. TI recommends decoupling the AVDD pin with a 1-µF, low-ESR ceramic capacitor. The minimum capacitor value required for AVDD is 200 nF.

TI Precision Designs	For a step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to TI Precision Design TIPD168, *Three 12-Bit Data Acquisition Reference Designs Optimized for Low Power and Ultra-Small Form Factor* (TIDU390).

9.2.1.3 Application Curve

Figure 41 shows the FFT plot for the device with a 5-kHz input frequency for the circuit in Figure 39.



SNR = 72.2 dB   THD = –85.7 dB   SINAD = 72 dB

Number of samples = 8192

Figure 41. Test Results for the ADS7044 and OPA316 for a 5-kHz Input

9.2.2 Ultra-Low Power and Ultra-Small, High CMRR DAQ Circuit with the ADS7044

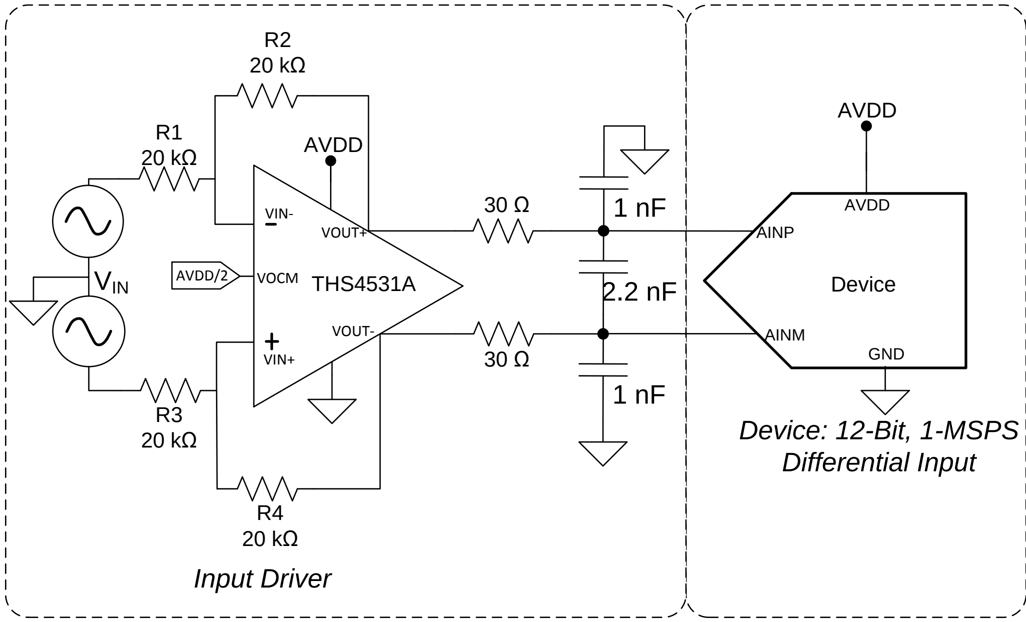


Figure 42. ADS7044 DAQ Circuit

9.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 4 as input parameters.

Table 4. Design Parameters

DESIGN PARAMETER	GOAL VALUE
SINAD	71 dB
Throughput	1 MSPS
AVDD	3.3 V
AVDD current consumption	800 µA (at a 5-kHz f_{IN}) and 1500 µA (at a 25-kHz f_{IN})
V_{IN} to the THS4531A	–AVDD to AVDD
Common-mode voltage for V_{IN} to the THS4531A	0 V to AVDD / 2

9.2.2.2 Detailed Design Procedure

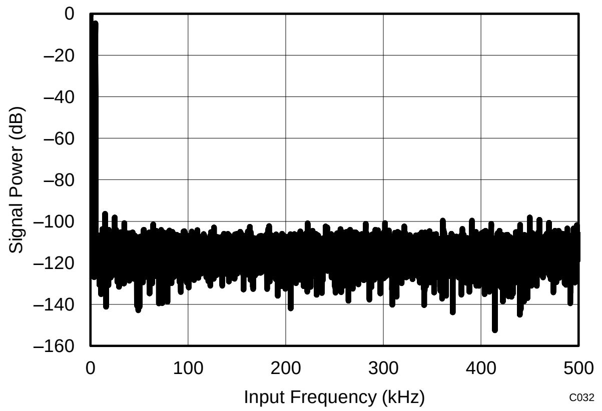
See the *Detailed Design Procedure* section in the *Single-Supply DAQ with the ADS7044* application for further details.

To achieve a SINAD of 71 dB, the operational amplifier must have high bandwidth to settle the input signal within the acquisition time of the ADC. The operational amplifier must have low noise to keep the total system noise below 20% of the input-referred noise of the ADC.

For the application circuit shown in Figure 42, the THS4531A is selected for its high bandwidth (36 MHz), low noise (10 nV/$\sqrt{Hz}$), and for its capability to set the common-mode voltage for the ADC. The THS4531A rejects the variation of common-mode at its input and provides a CMRR of 90 dB (min).

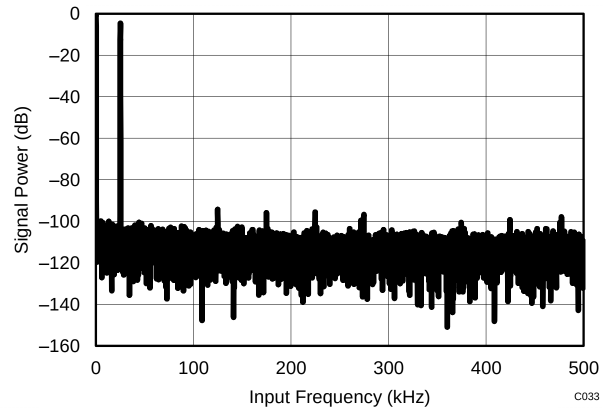
9.2.2.3 Application Curves

Figure 43 shows the FFT plot for the device with a 5-kHz input frequency for the circuit in Figure 42. Figure 44 shows the FFT plot for the device with a 25-kHz input frequency for the circuit in Figure 42.



SNR = 72.3 dB THD = –87.8 dB SINAD = 72.2 dB
AVDD current = 740 µA, Number of samples = 8192

Figure 43. Test Results for the ADS7044 and THS4531A for a 5-kHz Input



SNR = 71.6 dB THD = –85 dB SINAD = 71.4 dB
AVDD current = 1375 µA, Number of samples = 8192

Figure 44. Test Results for the ADS7044 and THS4531A for a 25-kHz Input

10 Power-Supply Recommendations

10.1 AVDD and DVDD Supply Recommendations

The device has two separate power supplies: AVDD and DVDD. The device operates on AVDD; DVDD is used for the interface circuits. AVDD and DVDD can be independently set to any value within the permissible ranges. The AVDD supply also defines the full-scale input range of the device. Decouple the AVDD and DVDD pins individually with 1-µF ceramic decoupling capacitors, as shown in Figure 45. The minimum capacitor value required for AVDD and DVDD is 200 nF and 20 nF, respectively. If both supplies are powered from the same source, a minimum capacitor value of 220 nF is required for decoupling.

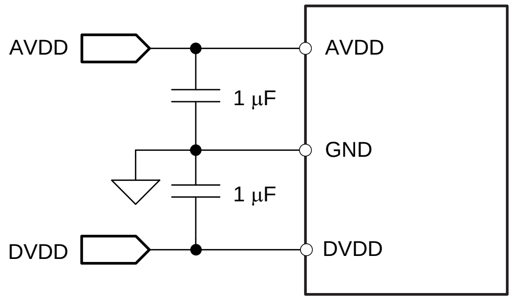


Figure 45. Power-Supply Decoupling

10.2 Estimating Digital Power Consumption

The current consumption from the DVDD supply depends on the DVDD voltage, load capacitance on the SDO line, and the output code. The load capacitance on the SDO line is charged by the current from the SDO pin on every rising edge of the data output and is discharged on every falling edge of the data output. The current consumed by the device from the DVDD supply can be calculated by Equation 4:

$$I_{DVDD} = C \times V \times f$$

where:

- C = Load capacitance on the SDO line,
- V = DVDD supply voltage, and
- f = Number of transitions on the SDO output. (4)

The number of transitions on the SDO output depends on the output code, and thus changes with the analog input. The maximum value of f occurs when data output on the SDO change on every SCLK. SDO changing on every SCLK results in an output code of AAAh or 555h. For an output code of AAAh or 555h at a 1-MSPS throughput, the frequency of transitions on the SDO output is 6 MHz.

To keep the current consumption at the lowest possible value, the DVDD supply must be kept at the lowest permissible value and the capacitance on the SDO line must be kept as low as possible.

10.3 Optimizing Power Consumed by the Device

- Keep the analog supply voltage (AVDD) as per the analog input full-scale range (FSR) requirement.
- Keep the digital supply voltage (DVDD) at the lowest permissible value.
- Reduce the load capacitance on the SDO output.
- Run the device at optimum throughput. Power consumption reduces with throughput.

11 Layout

11.1 Layout Guidelines

Figure 46 shows a board layout example for the ADS7044. Use a ground plane underneath the device and partition the PCB into analog and digital sections. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference input signals away from noise sources. In Figure 46, the analog input and reference signals are routed on the top and left side of the device while the digital connections are routed on the bottom and right side of the device.

The power sources to the device must be clean and well-bypassed. Use 1-µF ceramic bypass capacitors in close proximity to the analog (AVDD) and digital (DVDD) power-supply pins. Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors. Connect all ground pins to the ground plane using short, low-impedance paths. The AVDD supply voltage for the ADS7044 also functions as a reference for the device. Place the decoupling capacitor (C_{REF}) for AVDD close to the device AVDD and GND pins. C_{REF} must be connected to the device pins with thick copper tracks, as shown in Figure 46.

The fly-wheel RC filters are placed close to the device. Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors provide the best capacitance precision. The type of dielectric used in COG (NPO) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.

11.2 Layout Example

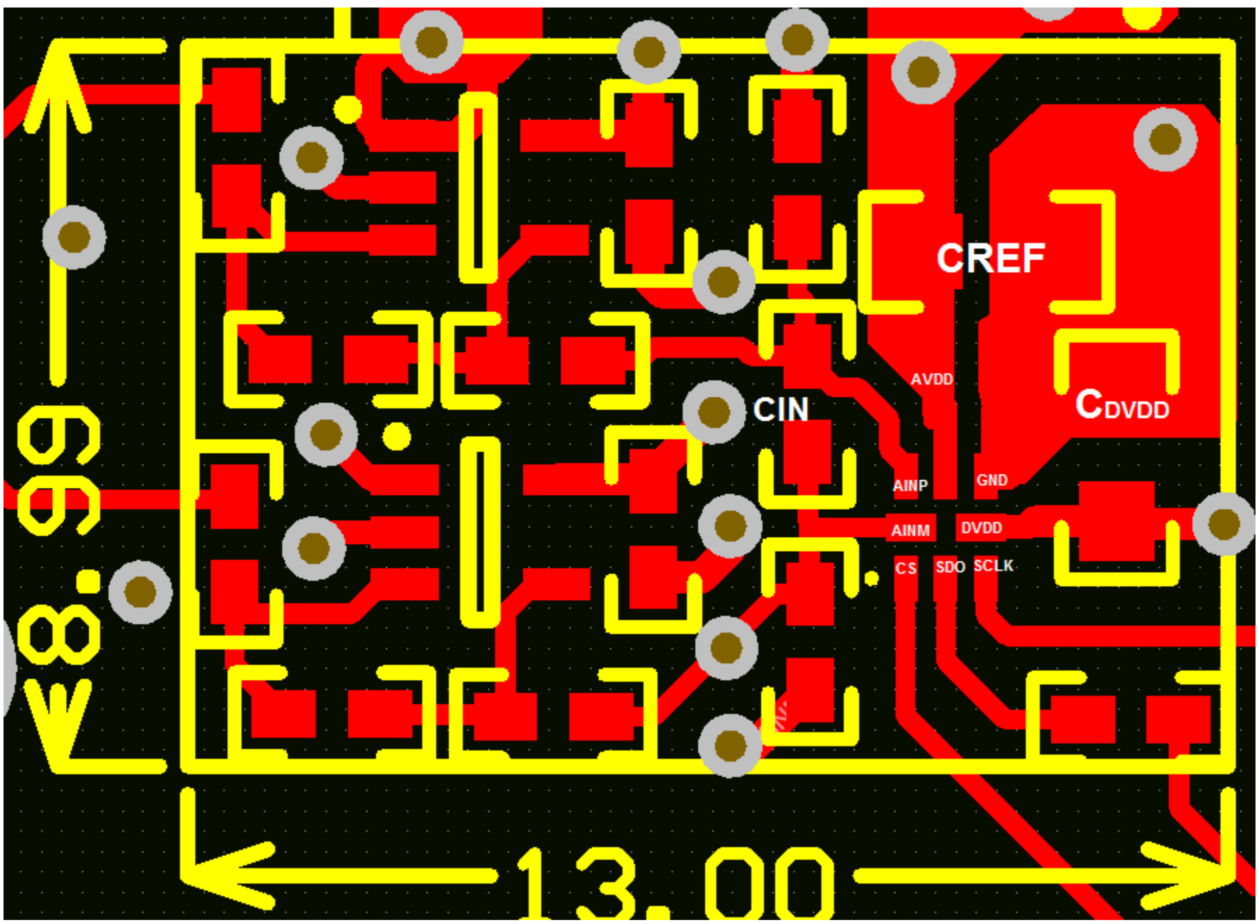


Figure 46. Example Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- OPA316 Data Sheet, SBOS703
- OPA835 Data Sheet, SLOS713
- THS4531A Data Sheet, SLOS823
- TPS79101 Data Sheet, SLVS325
- *Analysis of fully differential amplifiers*, SLYT157

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
TINA is a trademark of Texas Instruments, Inc.
SPI is a trademark of Motorola.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

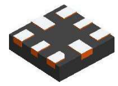
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

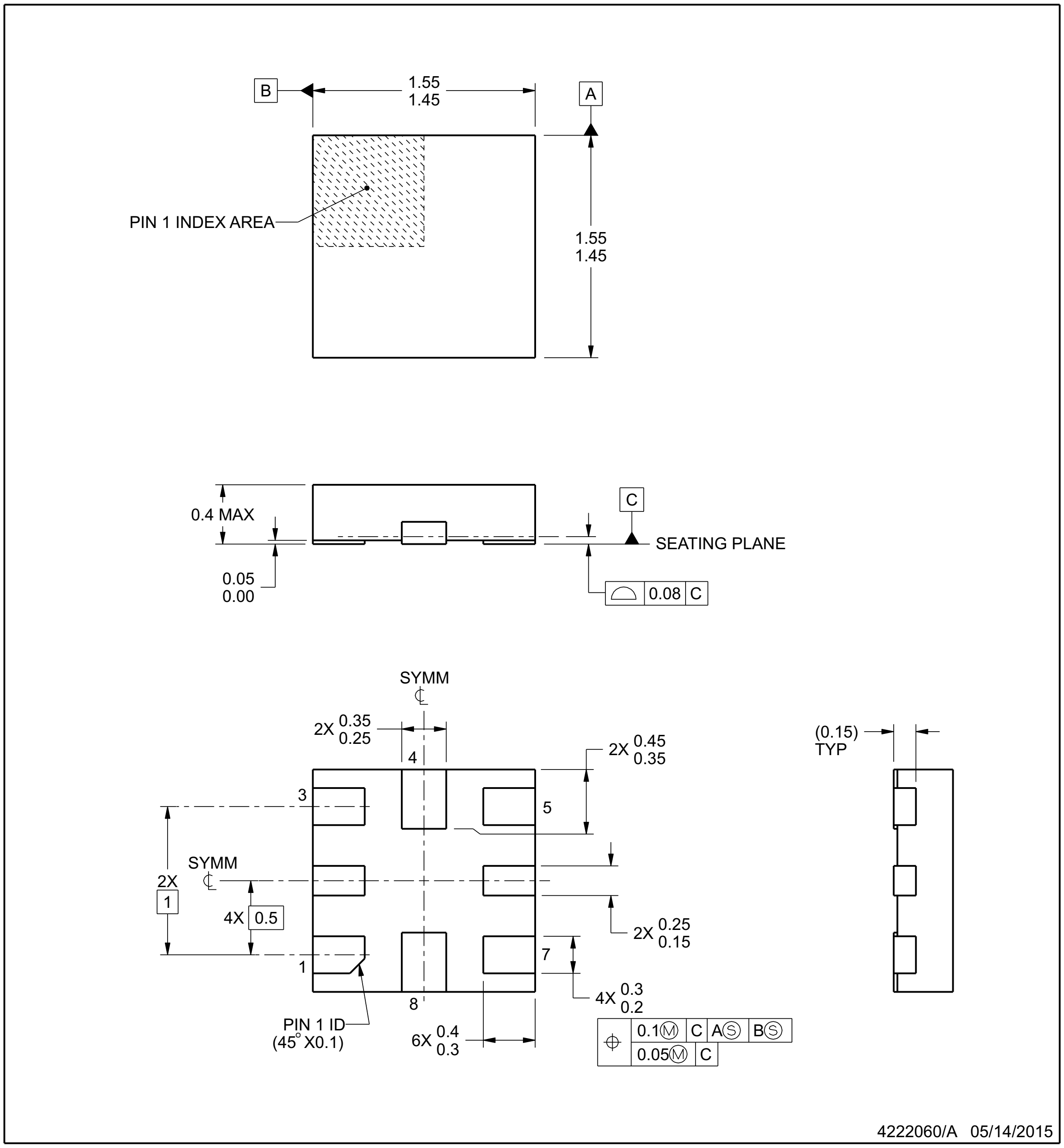
PACKAGE OUTLINE



RUG0008A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

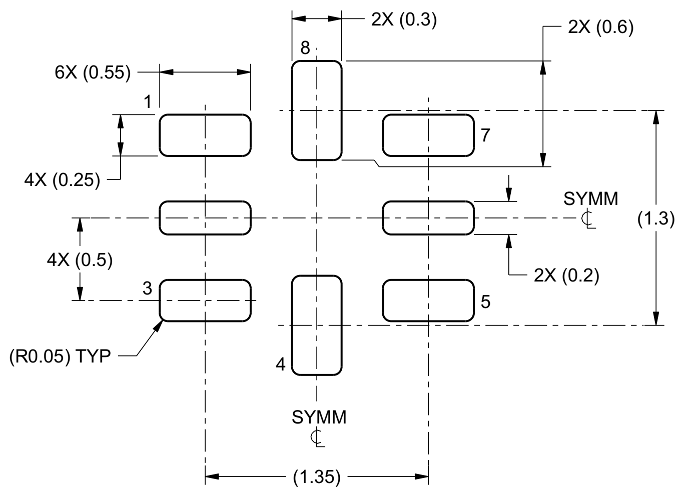
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

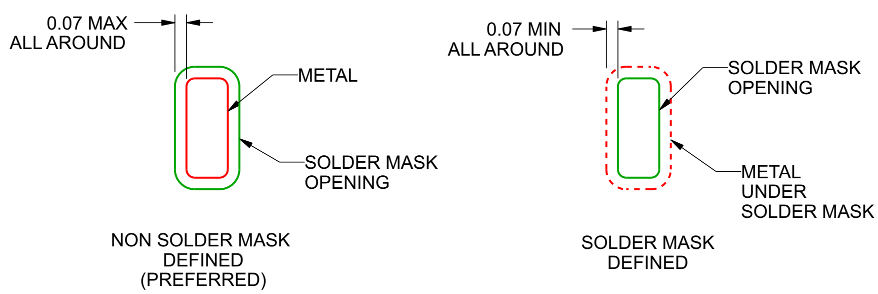
RUG0008A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS
NOT TO SCALE

4222060/A 05/14/2015

NOTES: (continued)

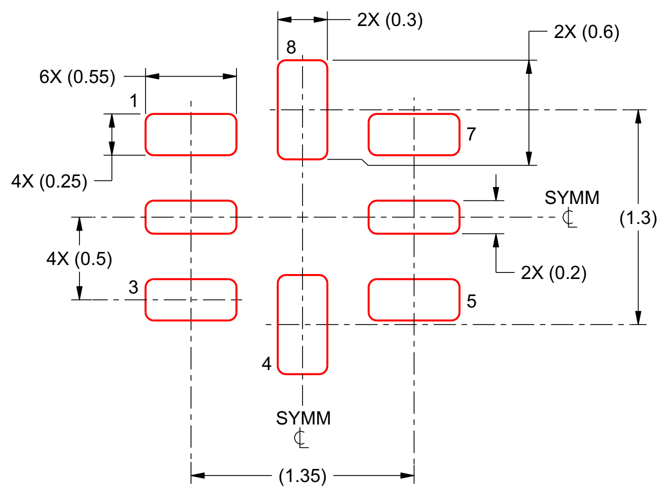
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RUG0008A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE:25X

4222060/A 05/14/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7044IDCUR	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7044	Samples
ADS7044IDCUT	ACTIVE	VSSOP	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7044	Samples
ADS7044IRUGR	ACTIVE	X2QFN	RUG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	FX	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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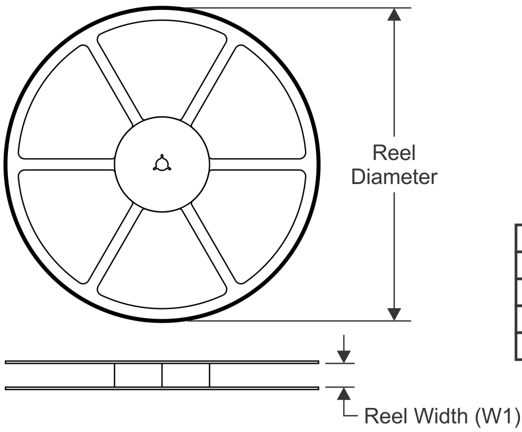
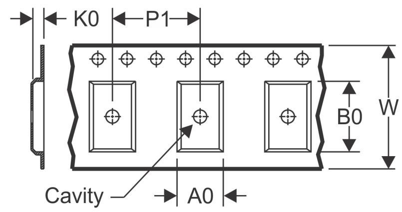
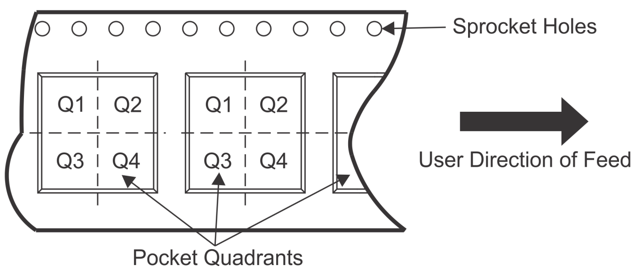
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





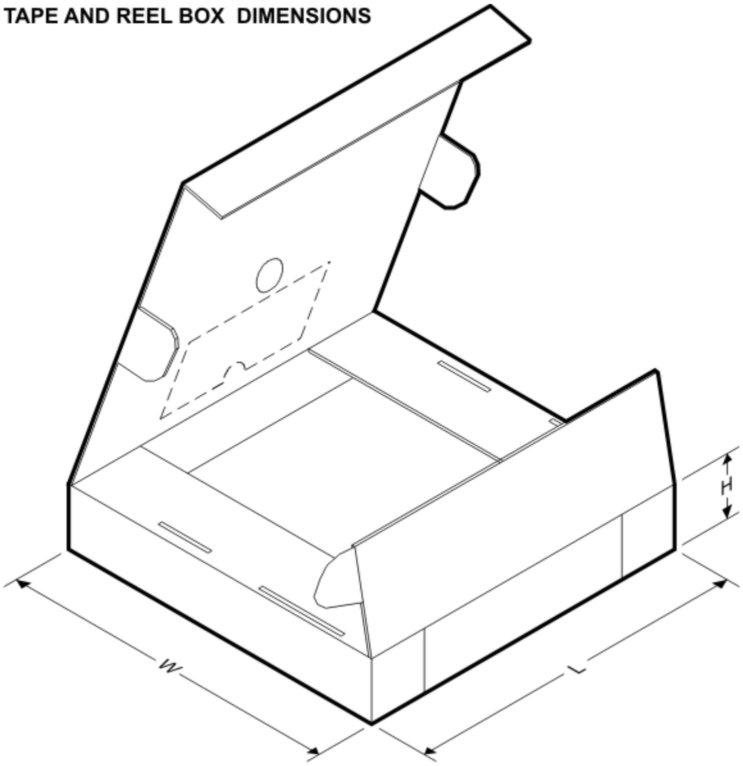
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7044IDCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
ADS7044IDCUT	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
ADS7044IRUGR	X2QFN	RUG	8	3000	180.0	8.4	1.6	1.6	0.66	4.0	8.0	Q2

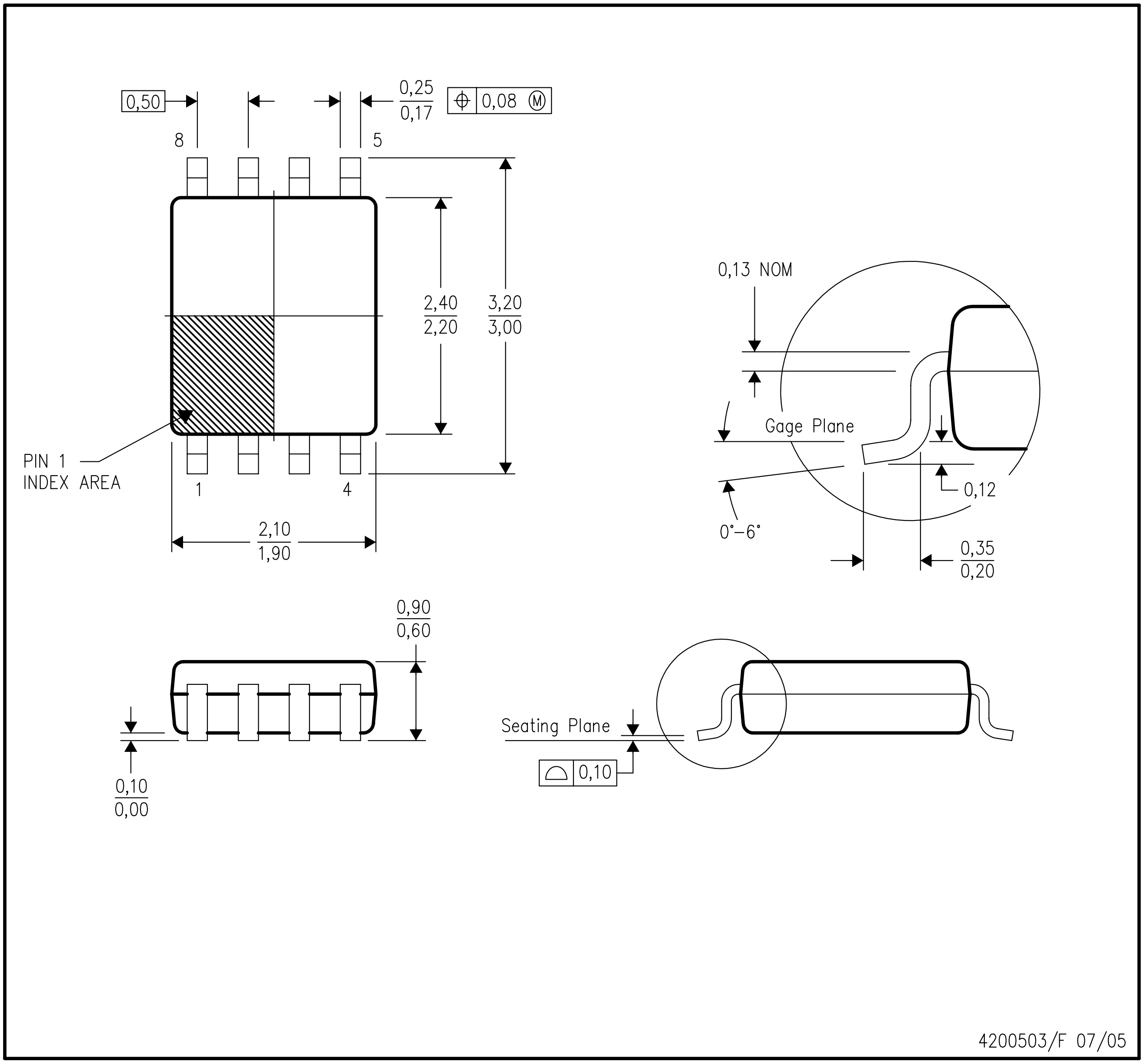
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

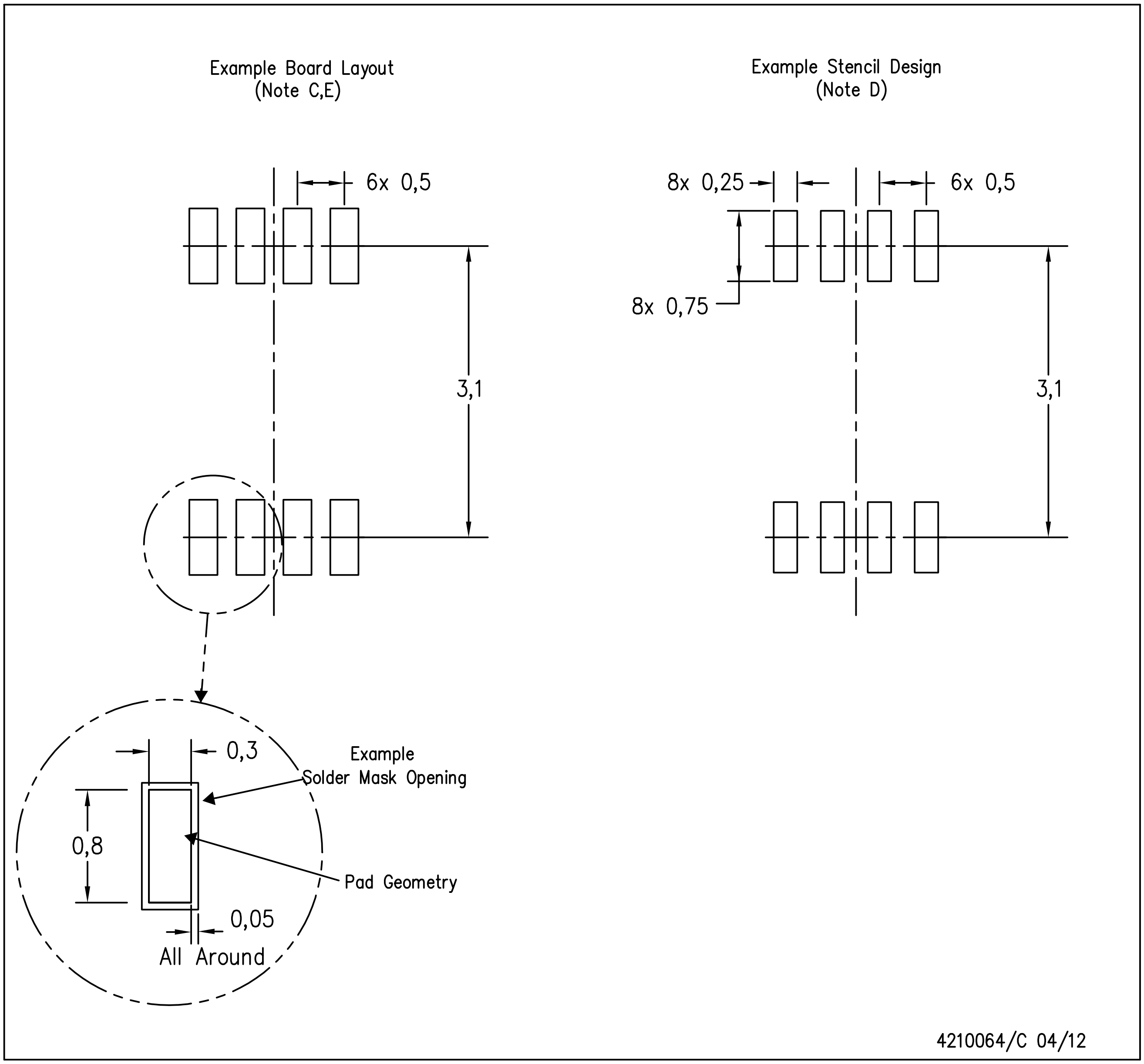
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7044IDCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
ADS7044IDCUT	VSSOP	DCU	8	250	202.0	201.0	28.0
ADS7044IRUGR	X2QFN	RUG	8	3000	202.0	201.0	28.0

DCU (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO–187 variation CA.

DCU (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.