16-BIT, HIGH-SPEED, 2.7-V TO 5-V, MICROPOWER SAMPLING ANALOG-TO-DIGITAL CONVERTER

Check for Samples: ADS8320-HT

FEATURES

- **100-kHz Sampling Rate**
- **Micropower:**
  - **3.8 mW at 100 kHz and 2.7 V**
  - **0.3 mW at 10 kHz and 2.7 V**
- **Power Down: 6 µA max**
- **8-Pin Ceramic Package**
- **Pin Compatible to ADS7816 and ADS7822**
- **Serial (SPI™/SSI) Interface**

APPLICATIONS

- **Down-Hole Drilling**
- **High Temperature Environments**
- **Vibration/Modal Analysis**
- **Multi-Channel Data Acquisition**
- **Acoustics/Dynamic Strain Gauges**
- **Pressure Sensors**

SUPPORTS EXTREME TEMPERATURE APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Extreme (–55°C/210°C) Temperature Range** (1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**
- **Texas Instruments' high temperature products utilize highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.**

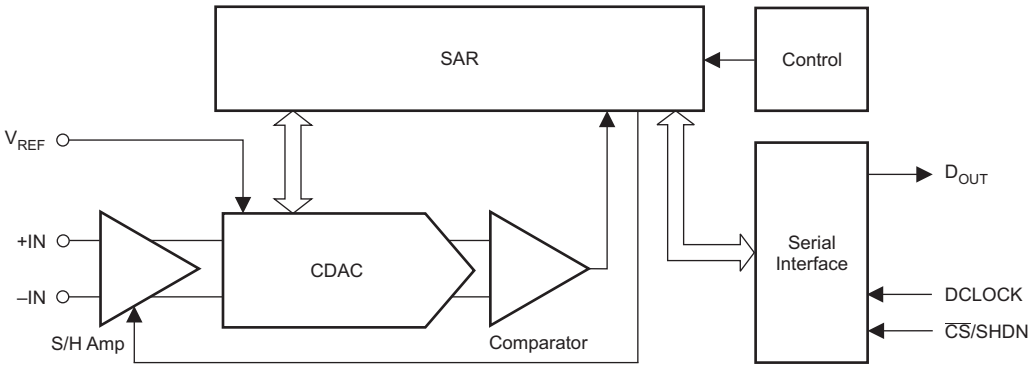
(1) Custom temperature ranges available

DESCRIPTION

The ADS8320 is a 16-bit, sampling analog-to-digital (A/D) converter with ensured specifications over a 2.7-V to 5.25-V supply range. It requires very little power even when operating at the full 100-kHz data rate. At lower data rates, the high speed of the device enables it to spend most of its time in the power-down mode—the average power dissipation is less than 100 mW at 10-kHz data rate.

The ADS8320 also features operation from 2 V to 5.25 V, a synchronous serial (SPI/SSI compatible) interface, and a differential input. The reference voltage can be set to any level within the range of 500 mV to V_{CC}.

Ultra-low power and small size make the ADS8320 ideal for portable and battery-operated systems. It is also a perfect fit for remote data acquisition modules, simultaneous multi-channel systems, and isolated data acquisition. The ADS8320 is available in 8-pin ceramic surface-mount packages, specified for the –55°C to 210°C temperature range.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SPI is a trademark of Motorola, Inc..

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING	PACKAGE QTY | CARRIER
–55°C to 210°C	HKJ	ADS8320SHKJ	ADS8320SHKJ	1 | TUBE
	HKQ	ADS8320SHKQ	ADS8320SHKQ	1 | TUBE
	KGD	ADS8320SKGD1	NA	240 | TRAY
		ADS8320SKGD2	NA	10 | TRAY

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

BARE DIE INFORMATION

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION
15 mils	Silicon backgrind	GND	Al-Si-Cu

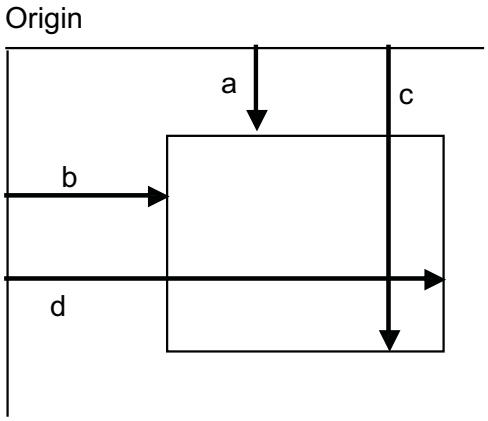
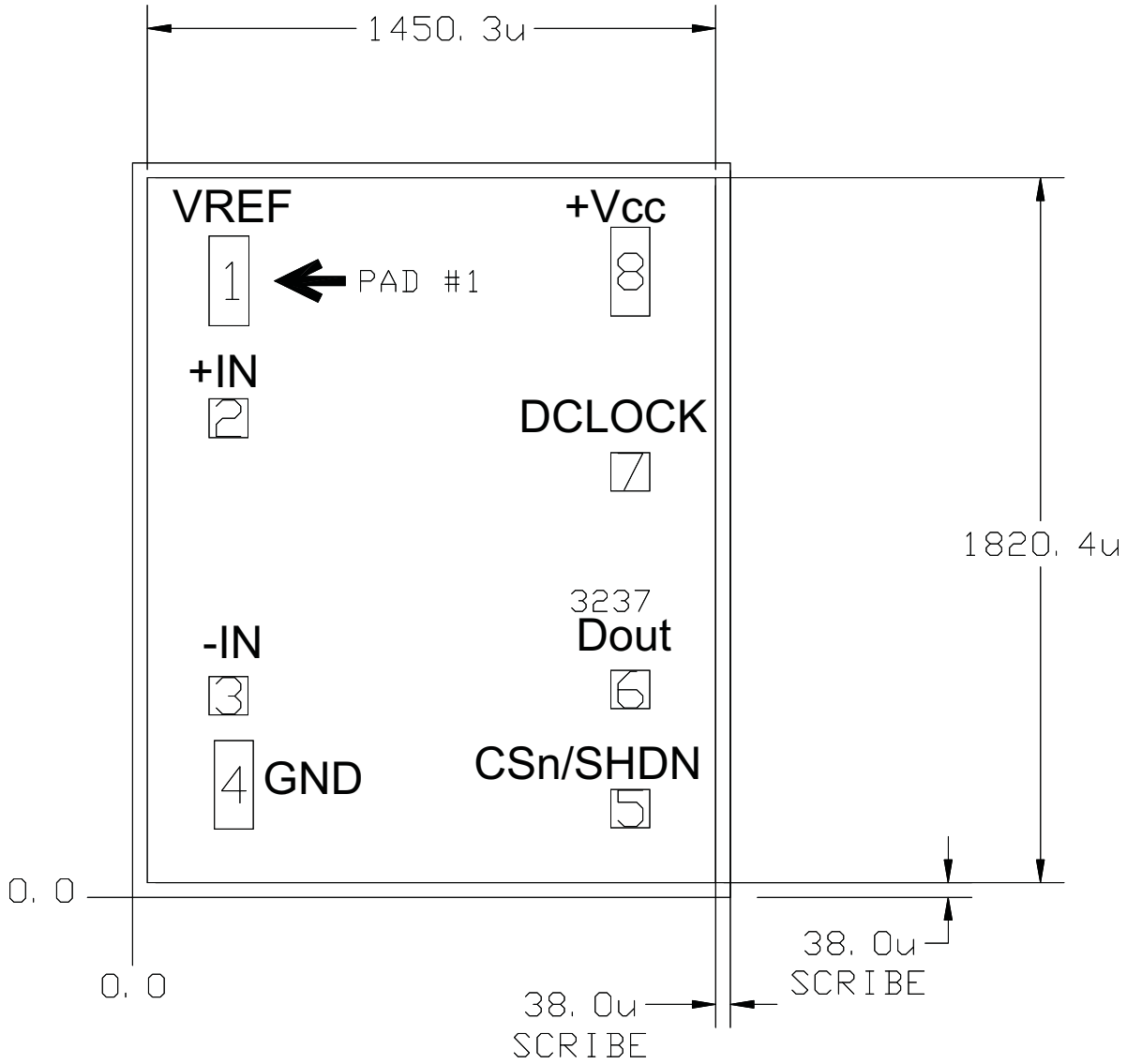


Table 1. Bond Pad Coordinates in Microns - Rev A

DISCRIPTION	PAD NUMBER	a	b	c	d
VREF	1	157.3	1437.4	259.5	1669.6
+IN	2	157.3	1149.4	256.6	1248.7
-IN	3	157.3	432.3	256.6	531.6
GND	4	171.2	137.4	270.4	366.6
$\overline{CS}$/SHDN	5	1183.1	141.3	1282.4	240.6
DOUT	6	1183.1	448.6	1282.4	547.8
DCLOCK	7	1183.1	1011.1	1282.4	1110.4
+VCC	8	1183.1	1462.8	1282.4	1692



ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted).(1)

		UNIT
V_{CC}	6	V
Analog input voltage	-0.3 to 6	V
Case temperature	100	°C
Junction temperature	–55 to 210	°C
Storage temperature	–55 to 210	°C
External referance voltage	5.5	V
Input current to any pin except supply	±10	mA

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

THERMAL CHARACTERISTICS FOR HKJ OR HKQ PACKAGE

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
θ_{JC}	Junction-to-case thermal resistance	to ceramic side of case			5.7	°C/W
		to top of case lid (metal side of case)			13.7	

ELECTRICAL CHARACTERISTICS

V_{CC} = 2.7 V, V_{REF} = 2.5 V, -IN = GND, f_{SAMPLE} = 100 kHz and f_{CLK} = 24 x f_{SAMPLE}, unless otherwise noted.

PARAMETER	CONDITIONS	T_A = -55°C to 125°C			T_A = 210°C(1)			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Resolution				16			16	Bits
Analog Input								
Full-zcale input span	+IN – (–IN)	0		VREF	0		VREF	V
Absolute input range	+IN	–0.1		VCC + 0.1	–0.1		VCC + 0.1	V
	–IN	–0.1		0.5	–0.1		0.5	
Capacitance			45			45		pF
Leakage current			1			1		nA
System Performance								
No missing codes		14			14			Bits
Integral linearity error			±0.008	±0.032		±0.018	±0.034	% of FSR
Offset error	V_{IN} = 3 V		±0.6	±3.8		±0.5	±3.8	mV
Offset temperature drift	V_{IN} = 3 V		±3			±4		µV/°C
Gain error	V_{IN} = 3 V			±0.05			±0.05	% of FSR
Gain temperature drift	V_{IN} = 3 V		±0.3			±0.3		ppm/°C
Noise			20			21		µVrms
Power-supply rejection ratio	2.7 V < V_{CC} < 3.3 V		3			5		LSB(2)

(1) Minimum and maximum parameters are characterized for operation at T_A = 210°C, but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.
(2) LSB means least significant bit. With V_{REF} = 2.5 V, one LSB is 0.038 V.

ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 2.7 V, V_{REF} = 2.5 V, -IN = GND, f_{SAMPLE} = 100 kHz and f_{CLK} = 24 x f_{SAMPLE}, unless otherwise noted.

PARAMETER		CONDITIONS	T_A = -55°C to 125°C			T_A = 210°C(1)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Sampling Dynamics									
Conversion time					16			16	Clk cycles
Acquisition time			4.5			4.5			Clk cycles
Throughput rate					100			100	kHz
Clock frequency range			0.02		2.4	0.02		2.4	MHz
Dynamic Characteristics									
Total harmonic distortion		V_{IN} = 2.7 x Vp-p at 1 kHz		-86			-82		dB
SINAD		V_{IN} = 2.7 x Vp-p at 1 kHz		84			79		dB
Spurious-free dynamic range		V_{IN} = 2.7 x Vp-p at 1 kHz		86			82		dB
SNR				88			83		dB
Reference Input									
Voltage range			0.5		V_{CC}	0.5		V_{CC}	V
Resistance		$\overline{CS}$ = GND, f_{SAMPLE} = 0 Hz		5			5		GΩ
		$\overline{CS}$ = V_{CC}		5			5		
Current drain				20	50		25	55	µA
		$\overline{CS}$ = V_{CC}		0.1	7		0.9	12	
Digital Input/Output									
Logic family				CMOS			CMOS		
Logic Levels	V_{IH}	I_{IH} = 5 µA	2		V_{CC} + 0.3	2		V_{CC} + 0.3	V
	V_{IL}	I_{IL} = 5 µA	-0.3		0.8	-0.3		0.8	V
	V_{OH}	I_{OH} = –250 µA	2.1			2.1			V
	V_{OL}	I_{OL} = 250 µA			0.4			0.4	V
Data format				Straight binary					
Power Supply Requirements									
V_{CC}		Specified performance	2.7		3.3	2.7		3.3	V
V_{CC} range(3)			2		5.25	2		5.25	V
		See (4)	2		2.7	2		2.7	
Quiescent current				850	1300		650	1300	µA
		f_{SAMPLE} = 10 kHz(5)(6)		100			100		
Power dissipation				2.3	3.8		1.75	3.8	mW
Power-down		$\overline{CS}$ = V_{CC}		0.3	4		6		µA
Temperature Range									
Specified performance			-55		125	-55		210	°C

(3) See the Typical Performance Curves for more information.
(4) The maximum clock rate of the ADS8320 is less than 2.4 MHz in this power supply range.
(5) f_{CLK} = 2.4 MHz, $\overline{CS}$ = V_{CC} for 216 clock cycles out of every 240.
(6) See the Power Dissipation section for more information regarding lower sample rates.

ELECTRICAL CHARACTERISTICS

V_{CC} = 5 V, V_{REF} = 5 V, -IN = GND, f_{SAMPLE} = 100 kHz and f_{CLK} = 24 x f_{SAMPLE}, unless otherwise noted.

PARAMETER		CONDITIONS	T_A = -55°C to 125°C			T_A = 210°C(1)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution					16			16	Bits
Analog Input									
Full-zcale input span		+IN – (–IN)	0		VREF	0		VREF	V
Absolute input range		+IN	–0.1		VCC + 0.1	–0.1		VCC + 0.1	V
		–IN	–0.1		0.5	–0.1		0.5	
Capacitance				45			45		pF
Leakage current				1			1		nA
System Performance									
No missing codes			14			14			Bits
Integral linearity error				±0.008	±0.032		±0.018	±0.034	% of FSR
Offset error				±0.6	±3.8		±0.5	±3.8	mV
Offset temperature drift				±3			±4		µV/°C
Gain error					±0.05			±0.05	% of FSR
Gain temperature drift				±0.3			±0.3		ppm/°C
Noise				20			21		µVrms
Power-supply rejection ratio		4.7 V < V_{CC} < 5.25 V		3			35		LSB(2)
Sampling Dynamics									
Conversion time					16			16	Clk cycles
Acquisition time			4.5			4.5			Clk cycles
Throughput rate					100			100	kHz
Clock frequency range			0.02		2.4	0.02		2.4	MHz
Dynamic Characteristics									
Total harmonic distortion		V_{IN} = 5 x Vp-p at 10 kHz		-84			-83		dB
SINAD		V_{IN} = 5 x Vp-p at 10 kHz		82			81		dB
Spurious-free dynamic range		V_{IN} = 5 x Vp-p at 10 kHz		84			83		dB
SNR				90			88		dB
Reference Input									
Voltage range			0.5		V_{CC}	0.5		V_{CC}	V
Resistance		$\overline{CS}$ = GND, f_{SAMPLE} = 0 Hz		5			5		GΩ
		$\overline{CS}$ = V_{CC}		5			5		
Current drain				40	80		50	80	µA
		f_{SAMPLE} = 10 kHz		0.8			0.8		
		$\overline{CS}$ = V_{CC}		0.1	5		2	5	
Digital Input/Output									
Logic family				CMOS			CMOS		
Logic Levels	V_{IH}	I_{IH} = 5 µA	3		V_{CC} + 0.3	3		V_{CC} + 0.3	V
	V_{IL}	I_{IL} = 5 µA	-0.3		0.8	-0.3		0.8	V
	V_{OH}	I_{OH} = –250 µA	4			4			V
	V_{OL}	I_{OL} = 250 µA			0.4			0.4	V
Data format			Straight binary						

(1) Minimum and maximum parameters are characterized for operation at T_A = 210°C, but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.

(2) LSB means least significant bit. With V_{REF} = 5 V, one LSB is 0.076 V.

ELECTRICAL CHARACTERISTICS (continued)

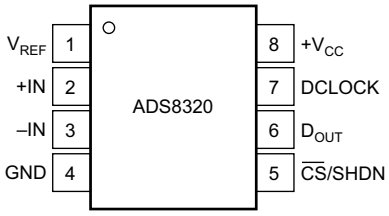
V_{CC} = 5 V, V_{REF} = 5 V, -IN = GND, f_{SAMPLE} = 100 kHz and f_{CLK} = 24 x f_{SAMPLE}, unless otherwise noted.

PARAMETER	CONDITIONS	T_A = -55°C to 125°C			T_A = 210°C(1)			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Power Supply Requirements								
V_{CC}	Specified performance	4.75		5.25	4.75		5.25	V
V_{CC} range(3)		2		5.25	2		5.25	V
Quiescent current			1150	1700		850	1700	µA
	f_{SAMPLE} = 10 kHz(4)(5)		200			200		
Power dissipation			5.5	8.5		4.5	8.5	mW
Power-down	$\overline{CS}$ = V_{CC}		0.3	3		5		µA
Temperature Range								
Specified performance		-55		125	-55		210	°C

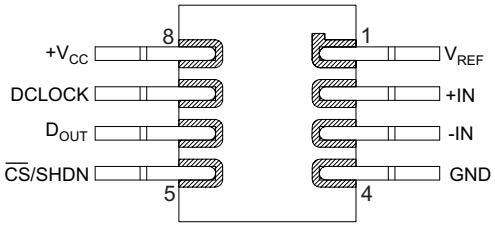
(3) See the Typical Performance Curves for more information.
(4) f_{CLK} = 2.4 MHz, $\overline{CS}$ = V_{CC} for 216 clock cycles out of every 240.
(5) See the Power Dissipation section for more information regarding lower sample rates.

PIN CONFIGURATION

HKJ PACKAGE
(TOP VIEW)



HKQ PACKAGE
(TOP VIEW)



HKQ as formed or HKJ mounted dead bug

PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	V_{REF}	Reference input
2	+IN	Noninverting input
3	-IN	Inverting input. Connect to ground or to remote ground sense point.
4	GND	Ground
5	$\overline{CS}$/SHDN	Chip select when LOW, shutdown mode when HIGH.
6	D_{OUT}	The serial output data word is comprised of 16 bits of data. In operation the data is valid on the falling edge of DCLOCK. The second clock pulse after the falling edge of CS enables the serial output. After one null bit the data is valid for the next 16 edges.
7	DCLOCK	Data clock synchronizes the serial data transfer and determines conversion speed.
8	+V_{CC}	Power supply

TYPICAL CHARACTERISTICS

At T_A = 25°C, V_{CC} = 5 V, V_{REF} = 5 V, f_{SAMPLE} = 100 kHz, and f_{CLK} = 24 x f_{SAMPLE}, unless otherwise specified.

INTEGRAL LINEARITY ERROR vs CODE (25°C)

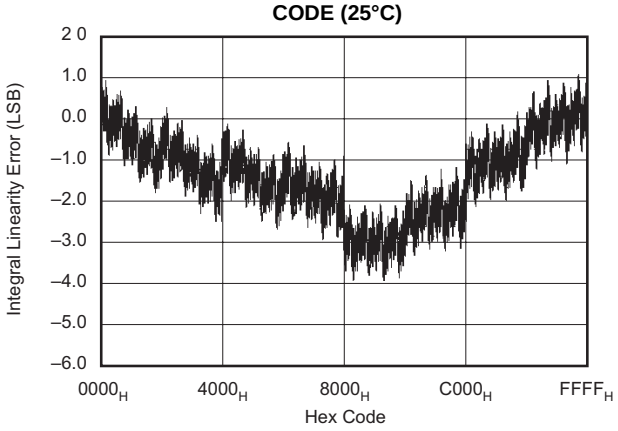


Figure 1.

DIFFERENTIAL LINEARITY ERROR vs CODE (25°C)

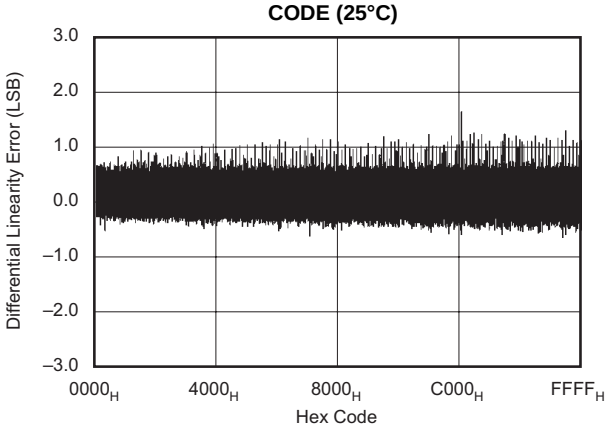


Figure 2.

SUPPLY CURRENT vs TEMPERATURE

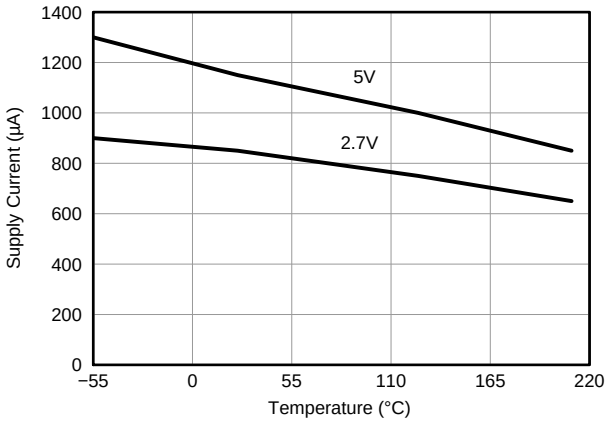


Figure 3.

POWER-DOWN SUPPLY CURRENT vs TEMPERATURE

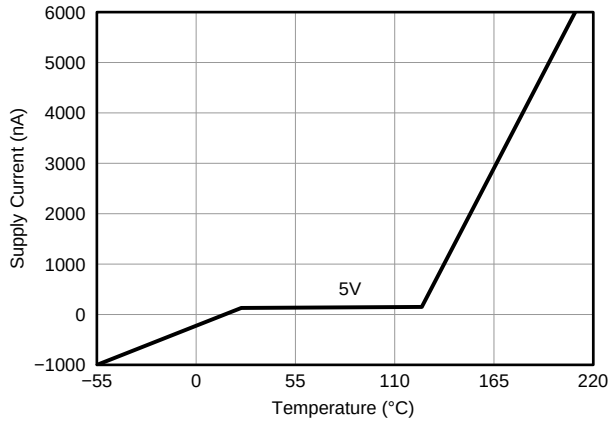


Figure 4.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_{CC} = 5 V, V_{REF} = 5 V, f_{SAMPLE} = 100 kHz, and f_{CLK} = 24 x f_{SAMPLE}, unless otherwise specified.

QUIESCENT CURRENT vs V_{CC}

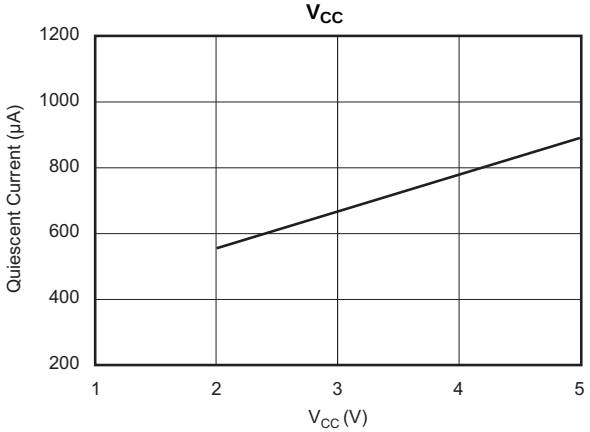


Figure 5.

MAXIMUM SAMPLE RATE vs V_{CC}

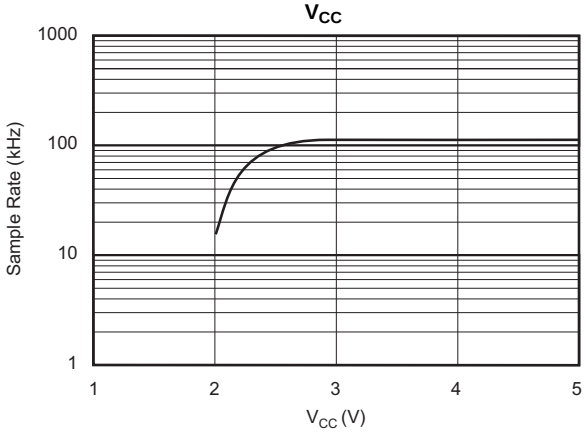


Figure 6.

CHANGE IN OFFSET vs REFERENCE VOLTAGE

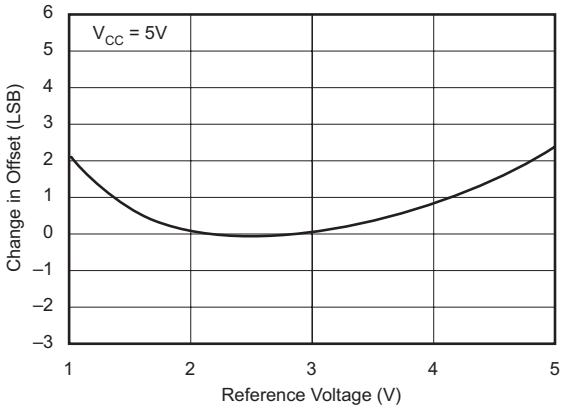


Figure 7.

CHANGE IN OFFSET vs TEMPERATURE

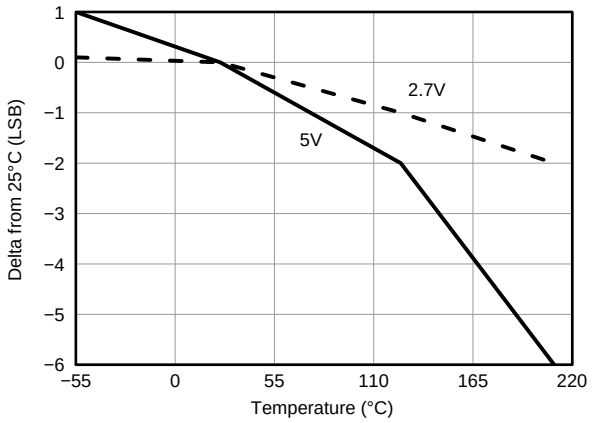


Figure 8.

CHANGE IN GAIN vs REFERENCE VOLTAGE

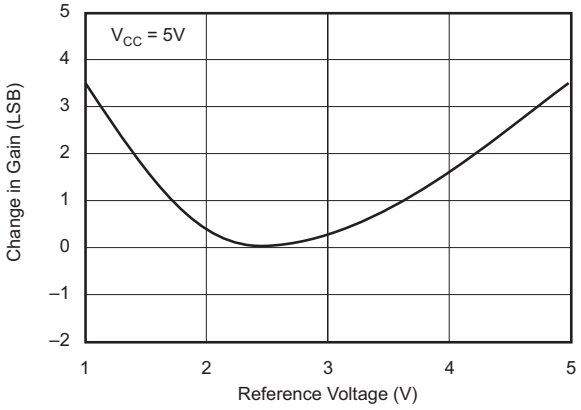


Figure 9.

CHANGE IN GAIN vs TEMPERATURE

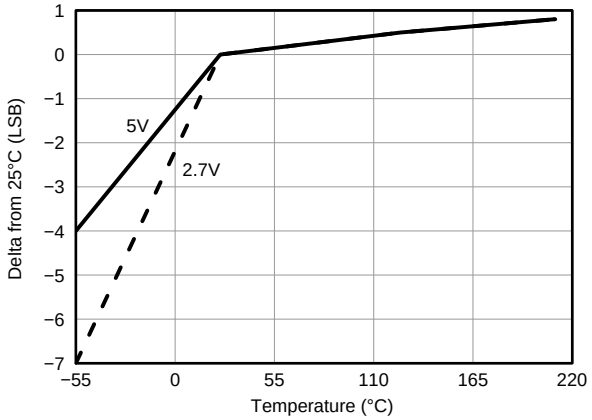


Figure 10.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_{CC} = 5 V, V_{REF} = 5 V, f_{SAMPLE} = 100 kHz, and f_{CLK} = 24 x f_{SAMPLE}, unless otherwise specified.

FREQUENCY SPECTRUM
(8192 Point FFT, F_{IN} = 10.120 kHz, –0.3 dB)

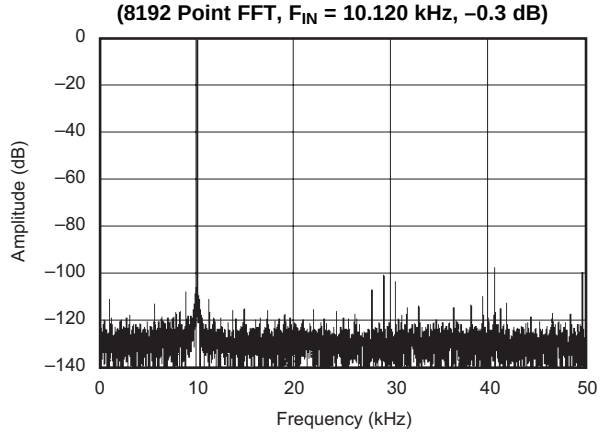


Figure 11.

PEAK-TO-PEAK NOISE
vs
REFERENCE VOLTAGE

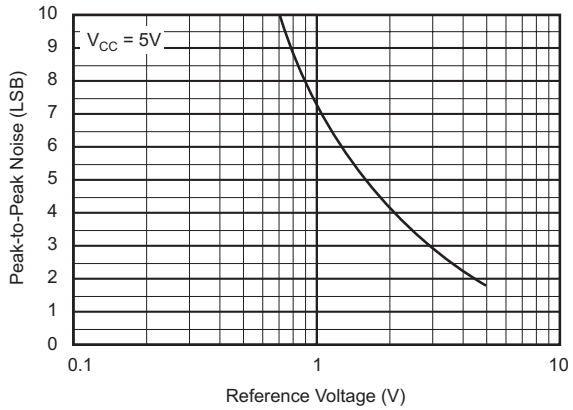


Figure 12.

SPURIOUS-FREE DYNAMIC RANGE AND SIGNAL-TO-NOISE RATIO
vs
FREQUENCY

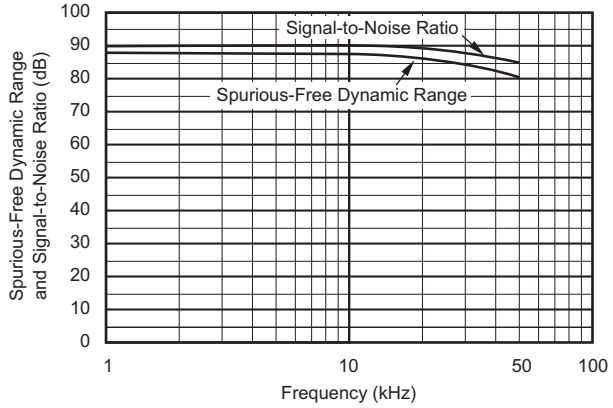


Figure 13.

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

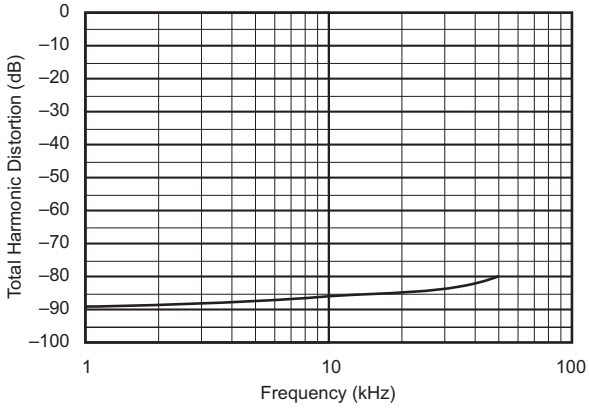


Figure 14.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_{CC} = 5 V, V_{REF} = 5 V, f_{SAMPLE} = 100 kHz, and f_{CLK} = 24 x f_{SAMPLE}, unless otherwise specified.

SIGNAL-TO-(NOISE + DISTORTION) vs FREQUENCY

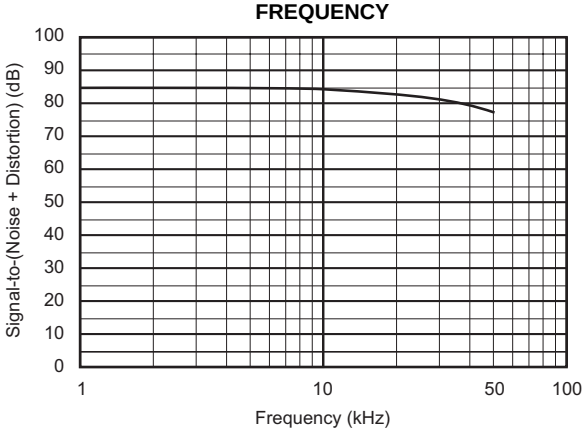


Figure 15.

SIGNAL-TO-(NOISE + DISTORTION) vs INPUT LEVEL

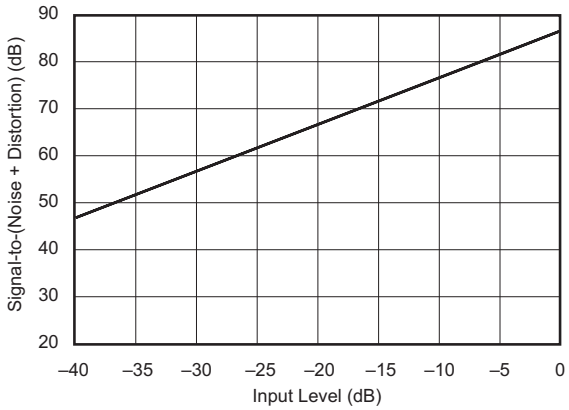


Figure 16.

REFERENCE CURRENT vs SAMPLE RATE

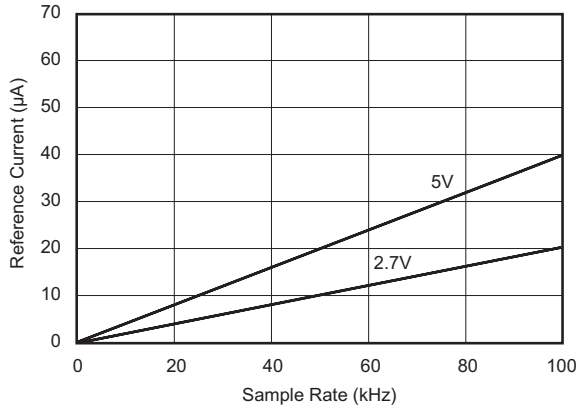


Figure 17.

REFERENCE CURRENT vs TEMPERATURE

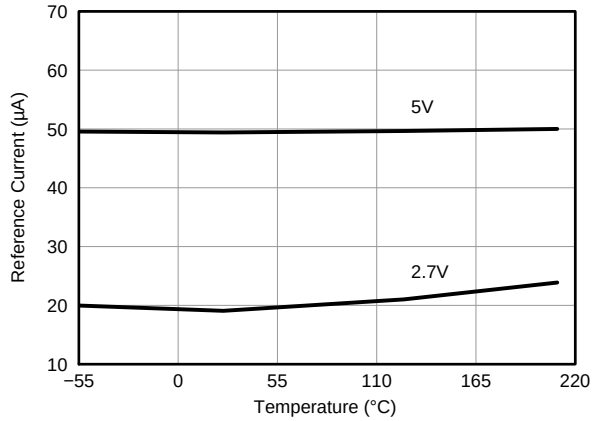


Figure 18.

THEORY OF OPERATION

The ADS8320 is a classic successive approximation register (SAR) analog-to-digital (A/D) converter. The architecture is based on capacitive redistribution, which inherently includes a sample/hold function. The converter is fabricated on a 0.6µ CMOS process. The architecture and process allow the ADS8320 to acquire and convert an analog signal at up to 100,000 conversions per second while consuming less than 4.5 mW from+V_{CC}.

The ADS8320 requires an external reference, an external clock, and a single power source (V_{CC}). The external reference can be any voltage between 500 mV and V_{CC}. The value of the reference voltage directly sets the range of the analog input. The reference input current depends on the conversion rate of the ADS8320.

The external clock can vary between 24 kHz (1-kHz throughput) and 2.4 MHz (100-kHz throughput). The duty cycle of the clock is essentially unimportant, as long as the minimum high and low times are at least 200 ns (V_{CC} = 2.7 V or greater). The minimum clock frequency is set by the leakage on the capacitors internal to the ADS8320.

The analog input is provided to two input pins: +IN and –IN. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

The digital result of the conversion is clocked out by the DCLOCK input and is provided serially, most significant bit first, on the D_{OUT} pin. The digital data that is provided on the DOUT pin is for the conversion currently in progress—there is no pipeline delay. It is possible to continue to clock the ADS8320 after the conversion is complete and to obtain the serial data least significant bit first. See the digital timing section for more information.

ANALOG INPUT

The +IN and –IN input pins allow for a differential input signal. Unlike some converters of this type, the –IN input is not re-sampled later in the conversion cycle. When the converter goes into the hold mode, the voltage difference between +IN and –IN is captured on the internal capacitor array.

The range of the –IN input is limited to –0.1 V to 1 V (–0.1 V to 0.5 V when using a 2.7-V supply). Because of this, the differential input can be used to reject only small signals that are common to both inputs. Thus, the –IN input is best used to sense a remote signal ground that may move slightly with respect to the local ground potential.

The input current on the analog inputs depends on a number of factors: sample rate, input voltage, source impedance, and power-down mode. Essentially, the current into the ADS8320 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (45 pF) to a 16-bit settling level within 4.5 clock cycles. When the converter goes into the hold mode or while it is in the powerdown mode, the input impedance is greater than 1 GΩ.

Care must be taken regarding the absolute analog input voltage. To maintain the linearity of the converter, the –IN input should not drop below GND – 100 mV or exceed GND + 1 V. The +IN input should always remain within the range of GND – 100 mV to V_{CC} + 100 mV. Outside of these ranges, the converter linearity may not meet specifications. To minimize noise, low bandwidth input signals with lowpass filters should be used.

REFERENCE INPUT

The external reference sets the analog input range. The ADS8320 operates with a reference in the range of 500 mV to V_{CC}. There are several important implications of this.

As the reference voltage is reduced, the analog voltage weight of each digital output code is reduced. This is often referred to as the Least Significant Bit (LSB) size and is equal to the reference voltage divided by 65,536. This means that any offset or gain error inherent in the A/D converter will appear to increase, in terms of LSB size, as the reference voltage is reduced.

The noise inherent in the converter also appears to increase with lower LSB size. With a 5-V reference, the internal noise of the converter typically contributes only 1.5 LSB peak-to-peak of potential error to the output code. When the external reference is 500 mV, the potential error contribution from the internal noise will be 10 times larger—15 LSBs. The errors due to the internal noise are gaussian in nature and can be reduced by averaging consecutive conversion results.

For more information regarding noise, consult the typical performance curve “Peak-to-Peak Noise vs Reference Voltage.” Note that the Effective Number of Bits (ENOB) figure is calculated based on the converter’s signal-to-(noise + distortion) ratio with a 1-kHz, 0-dB input signal. SINAD is related to ENOB as follows:

$$SINAD = 6.02 \bullet ENOB + 1.76 \quad (1)$$

With lower reference voltages, extra care should be taken to provide a clean layout including adequate bypassing, a clean power supply, a low-noise reference, and a low-noise input signal. Because the LSB size is lower, the converter is also more sensitive to external sources of error such as nearby digital signals and electromagnetic interference.

NOISE

The noise floor of the ADS8320 itself is extremely low, as can be seen in Figure 19 and Figure 20, and is much lower than competing A/D converters. It was tested by applying a lownoise DC input and a 5-V reference to the ADS8320 and initiating 5000 conversions. The digital output of the A/D converter varies in output code due to the internal noise of the ADS8320. This is true for all 16-bit SAR-type A/D converters. Using a histogram to plot the output codes, the distribution should appear bell-shaped with the peak of the bell curve representing the nominal code for the input value. The ±1σ, ±2σ and ±3σ distributions represents the 68.3%, 95.5%, and 99.7%, respectively, of all codes. The transition noise can be calculated by dividing the number of codes measured by 6 and this yields the ±3σ distribution or 99.7% of all codes. Statistically, up to 3 codes could fall outside the distribution when executing 1000 conversions. The ADS8320, with < 3 output codes for ±3σ distribution, yields a < ±0.5 LSB transition noise. Remember, to achieve this low noise performance, the peak-to-peak noise of the input signal and reference must be < 50 µV.

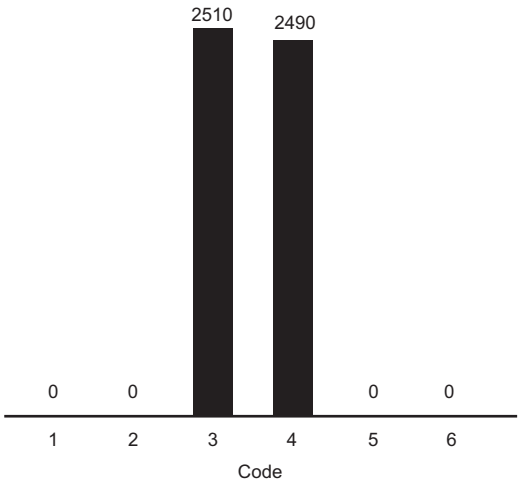


Figure 19. Histogram of 5000 Conversions of a DC Input at the Code Transition

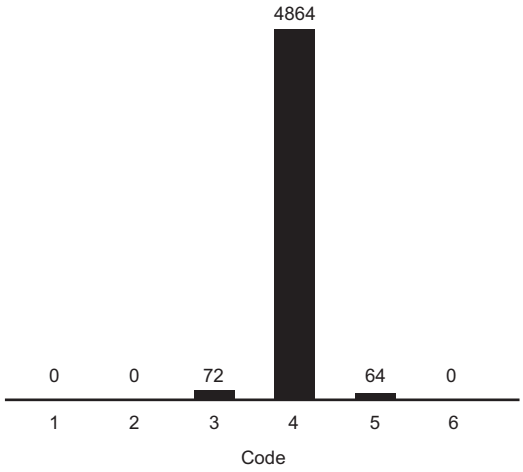


Figure 20. Histogram of 5000 Conversions of a DC Input at the Code Center

DIGITAL INTERFACE

SIGNAL LEVELS

The digital inputs of the ADS8320 can accommodate logic levels up to 5.5 V regardless of the value of V_{CC}. Thus, the ADS8320 can be powered at 3 V and still accept inputs from logic powered at 5 V.

The CMOS digital output (D_{OUT}) swings 0 V to V_{CC}. If V_{CC} is 3 V and this output is connected to a 5-V CMOS logic input, then that IC may require more supply current than normal and may have a slightly longer propagation delay.

SERIAL INTERFACE

The ADS8320 communicates with microprocessors and other digital systems via a synchronous 3-wire serial interface, as shown in Figure 21 and Table 2. The DCLOCK signal synchronizes the data transfer with each bit being transmitted on the falling edge of DCLOCK. Most receiving systems will capture the bitstream on the rising edge of DCLOCK. However, if the minimum hold time for D_{OUT} is acceptable, the system can use the falling edge of DCLOCK to capture each bit.

A falling $\overline{CS}$ signal initiates the conversion and data transfer. The first 4.5 to 5.0 clock periods of the conversion cycle are used to sample the input signal. After the fifth falling DCLOCK edge, D_{OUT} is enabled and outputs a LOW value for one clock period. For the next 16 DCLOCK periods, D_{OUT} outputs the conversion result, most significant bit first. After the least significant bit (B0) has been output, subsequent clocks repeat the output data but in a least significant bit first format.

After the most significant bit (B15) has been repeated, D_{OUT} will tri-state. Subsequent clocks will have no effect on the converter. A new conversion is initiated only when $\overline{CS}$ has been taken HIGH and returned LOW.

Table 2. Timing Specifications (V_{CC} = 2.7 V and Above, –55°C to 210°C)

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{SMPL}	Analog input sample time	4.5		5	Clk cycles
t_{CONV}	Conversion time		16		Clk cycles
t_{CYC}	Throughput rate			100	kHz
t_{CSD}	$\overline{CS}$ falling to DCLOCK LOW			0	ns
t_{SUCS}	$\overline{CS}$ falling to DCLOCK Rising	20			ns
t_{hDO}	DCLOCK falling to current D_{OUT} not valid	5	15		ns
t_{dDO}	DCLOCK falling to next D_{OUT} valid		30	50	ns
t_{dis}	$\overline{CS}$ rising to D_{OUT} tri-state		70	100	ns
t_{en}	DCLOCK falling to D_{OUT} enabled		20	50	ns
t_f	D_{OUT} fall time		5	25	ns
t_r	D_{OUT} rise time		7	25	ns

DATA FORMAT

The output data from the ADS8320 is in straight binary format, as shown in Table 3. This table represents the ideal output code for the given input voltage and does not include the effects of offset, gain error, or noise.

Table 3. Ideal Input Voltages and Output Codes

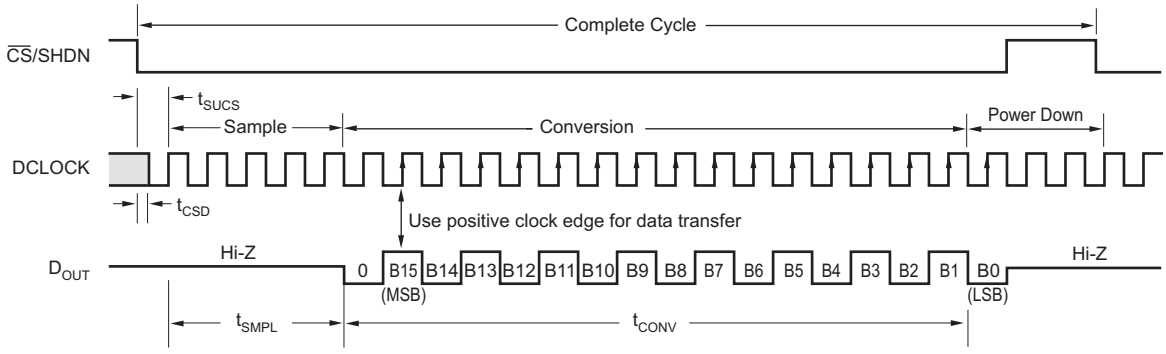
DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT STRAIGHT BINARY	
		BINARY CODE	HEX CODE
Full-scale range	V_{REF}		
Least significant bit (LSB)	V_{REF}/65,536		
Full scale	V_{REF} – 1 LSB	1111 1111 1111 1111	FFFF
Midscale	V_{REF}/2	1000 0000 0000 0000	8000
Midscale – 1 LSB	V_{REF}/2 – 1 LSB	0111 1111 1111 1111	7FFF
Zero	0 V	0000 0000 0000 0000	0000

POWER DISSIPATION

The architecture of the converter, the semiconductor fabrication process, and a careful design allow the ADS8320 to convert at up to a 100-kHz rate while requiring very little power. Still, for the absolute lowest power dissipation, there are several things to keep in mind.

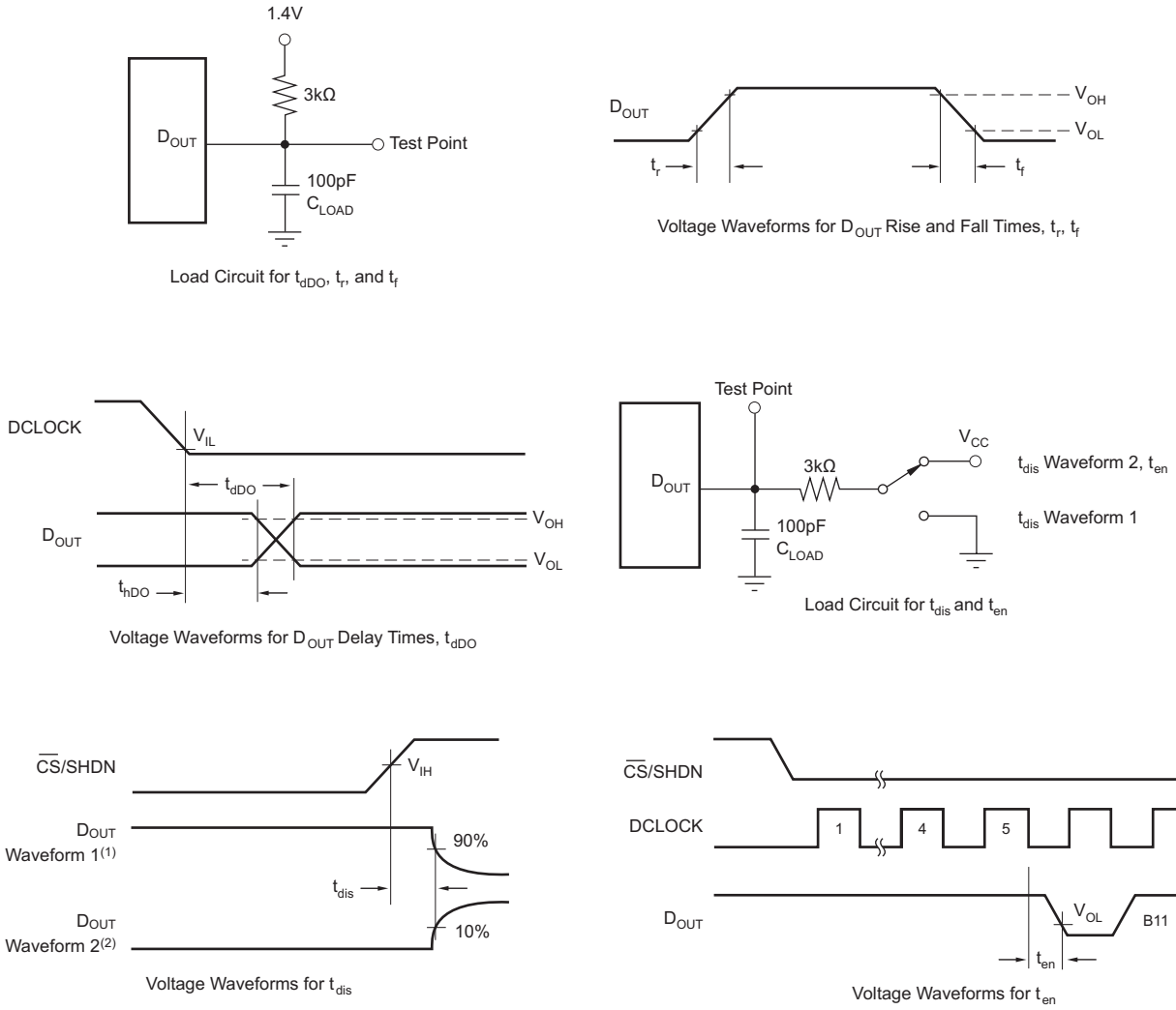
The power dissipation of the ADS8320 scales directly with conversion rate. Therefore, the first step to achieving the lowest power dissipation is to find the lowest conversion rate that satisfies the requirements of the system.

In addition, the ADS8320 is in power-down mode under two conditions: when the conversion is complete and whenever $\overline{CS}$ is HIGH (as shown in Figure 21). Ideally, each conversion should occur as quickly as possible, preferably at a 2.4-MHz clock rate. This way, the converter spends the longest possible time in the power-down mode. This is very important as the converter not only uses power on each DCLOCK transition (as is typical for digital CMOS components), but also uses some current for the analog circuitry, such as the comparator. The analog section dissipates power continuously, until the power-down mode is entered.



NOTE: Minimum 22 clock cycles required for 16-bit conversion. Shown are 24 clock cycles.
If $\overline{CS}$ remains LOW at the end of conversion, a new datastream with LSB-first is shifted out again.

Figure 21. ADS8320 Basic Timing Diagrams



NOTES: (1) Waveform 1 is for an output with internal conditions such that the output is HIGH unless disabled by the output control. (2) Waveform 2 is for an output with internal conditions such that the output is LOW unless disabled by the output control.

Figure 22. Timing Diagrams and Test Circuits for the Parameters in Table 2

Figure 23 shows the current consumption of the ADS8320 versus sample rate. For this graph, the converter is clocked at 2.4 MHz regardless of the sample rate—$\overline{CS}$ is HIGH for the remaining sample period. Figure 24 also shows current consumption versus sample rate. However, in this case, the DCLOCK period is 1/24th of the sample period—$\overline{CS}$ is HIGH for one DCLOCK cycle out of every 16.

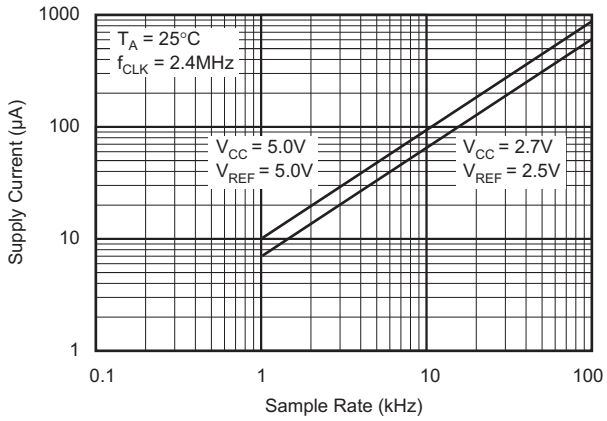


Figure 23. Maintaining f_{CLK} at the Highest Possible Rate Allows Supply Current to Drop Linearly With Sample Rate

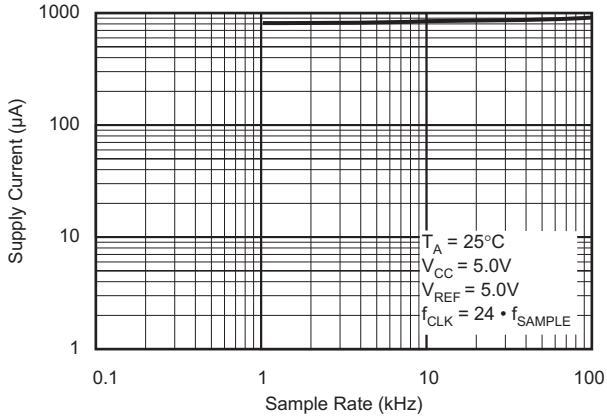


Figure 24. Scaling f_{CLK} Reduces Supply Current Only Slightly With Sample Rate

There is an important distinction between the power-down mode that is entered after a conversion is complete and the full power-down mode which is enabled when $\overline{CS}$ is HIGH. $\overline{CS}$ LOW will shut down only the analog section. The digital section is completely shut down only when $\overline{CS}$ is HIGH. Thus, if $\overline{CS}$ is left LOW at the end of a conversion and the converter is continually clocked, the power consumption will not be as low as when $\overline{CS}$ is HIGH. Figure 25 shows more information.

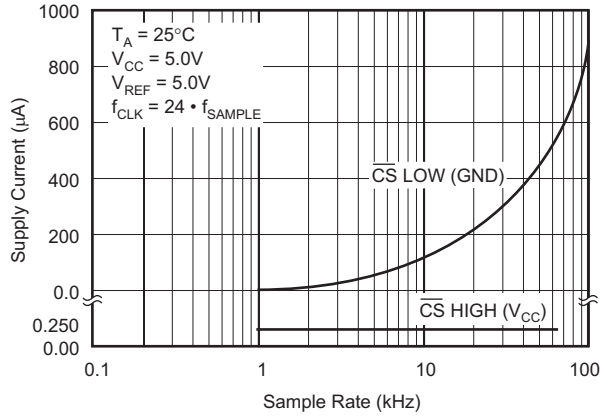


Figure 25. Shutdown Current With $\overline{CS}$ HIGH is 50 nA Typically, Regardless of the Clock. Shutdown Current With $\overline{CS}$ LOW Varies With Sample Rate

Power dissipation can also be reduced by lowering the power-supply voltage and the reference voltage. The ADS8320 operates over a V_{CC} range of 2.0 V to 5.25 V. However, at voltages below 2.7 V, the converter will not run at a 100-kHz sample rate. See the typical performance curves for more information regarding power supply voltage and maximum sample rate.

SHORT CYCLING

Another way of saving power is to utilize the $\overline{CS}$ signal to short cycle the conversion. Because the ADS8320 places the latest data bit on the D_{OUT} line as it is generated, the converter can easily be short cycled. This term means that the conversion can be terminated at any time. For example, if only 14 bits of the conversion result are needed, then the conversion can be terminated (by pulling $\overline{CS}$ HIGH) after the 14th bit has been clocked out.

This technique can be used to lower the power dissipation (or to increase the conversion rate) in those applications where an analog signal is being monitored until some condition becomes true. For example, if the signal is outside a predetermined range, the full 16-bit conversion result may not be needed. If so, the conversion can be terminated after the first n bits, where n might be as low as 3 or 4. This results in lower power dissipation in both the converter and the rest of the system, as they spend more time in the power-down mode.

LAYOUT (1)

For optimum performance, care should be taken with the physical layout of the ADS8320 circuitry. This is particularly true if the reference voltage is low and/or the conversion rate is high. At a 100-kHz conversion rate, the ADS8320 makes a bit decision every 416 ns. That is, for each subsequent bit decision, the digital output must be updated with the results of the last bit decision, the capacitor array appropriately switched and charged, and the input to the comparator settled to a 16-bit level all within one clock cycle.

The basic SAR architecture is sensitive to spikes on the power supply, reference, and ground connections that occur just prior to latching the comparator output. Thus, during any single conversion for an n-bit SAR converter, there are n “windows” in which large external transient voltages can easily affect the conversion result. Such spikes might originate from switching power supplies, digital logic, and high power devices, to name a few. This particular source of error can be very difficult to track down if the glitch is almost synchronous to the converter DCLOCK signal—as the phase difference between the two changes with time and temperature, causing sporadic misoperation.

With this in mind, power to the ADS8320 should be clean and well bypassed. A 0.1-µF ceramic bypass capacitor should be placed as close to the ADS8320 package as possible. In addition, a 1-µF to 10-µF capacitor and a 5-Ω or 10-Ω series resistor may be used to low-pass filter a noisy supply.

The reference should be similarly bypassed with a 0.1-µF capacitor. Again, a series resistor and large capacitor can be used to low-pass filter the reference voltage. If the reference voltage originates from an op amp, be careful that the op amp can drive the bypass capacitor without oscillation (the series resistor can help in this case). Keep in mind that while the ADS8320 draws very little current from the reference on average, there are still instantaneous current demands placed on the external input and reference circuitry.

Texas Instruments' OPA627 op amp provides optimum performance for buffering both the signal and reference inputs. For low-cost, low-voltage, single-supply applications, the OPA2350 or OPA2340 dual op amps are recommended.

Also, keep in mind that the ADS8320 offers no inherent rejection of noise or voltage variation in regards to the reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results. While high-frequency noise can be filtered out as described in the previous paragraph, voltage variation due to the line frequency (50 Hz or 60 Hz), can be difficult to remove.

The GND pin on the ADS8320 should be placed on a clean ground point. In many cases, this will be the “analog” ground. Avoid connecting the GND pin too close to the grounding point for a microprocessor, microcontroller, or digital signal processor. If needed, run a ground trace directly from the converter to the power-supply connection point. The ideal layout includes an analog ground plane for the converter and associated analog circuitry.

(1) OPA627, OPA2350 and OPA2340 have not been characterized or tested at 210°C.

APPLICATION CIRCUITS

Figure 26 shows a basic data acquisition system. The ADS8320 input range is 0 V to V_{CC}, as the reference input is connected directly to the power supply. The 5-Ω resistor and 1-µF to 10-µF capacitor filter the microcontroller "noise" on the supply, as well as any high-frequency noise from the supply itself. The exact values should be picked such that the filter provides adequate rejection of the noise.

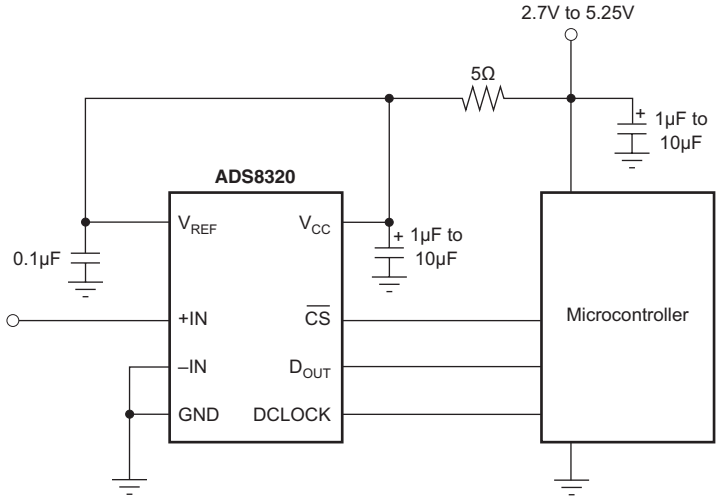


Figure 26. Basic Data Acquisition System

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8320SHKJ	ACTIVE	CFP	HKJ	8	1	TBD	Call TI	N / A for Pkg Type	-55 to 210	ADS8320S HKJ	Samples
ADS8320SHKQ	ACTIVE	CFP	HKQ	8	1	TBD	AU	N / A for Pkg Type	-55 to 210	ADS8320S HKQ	Samples
ADS8320SKGD1	ACTIVE	XCEPT	KGD	0	240	TBD	Call TI	N / A for Pkg Type	-55 to 210		Samples
ADS8320SKGD2	ACTIVE	XCEPT	KGD	0	10	TBD	Call TI	N / A for Pkg Type	-55 to 210		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

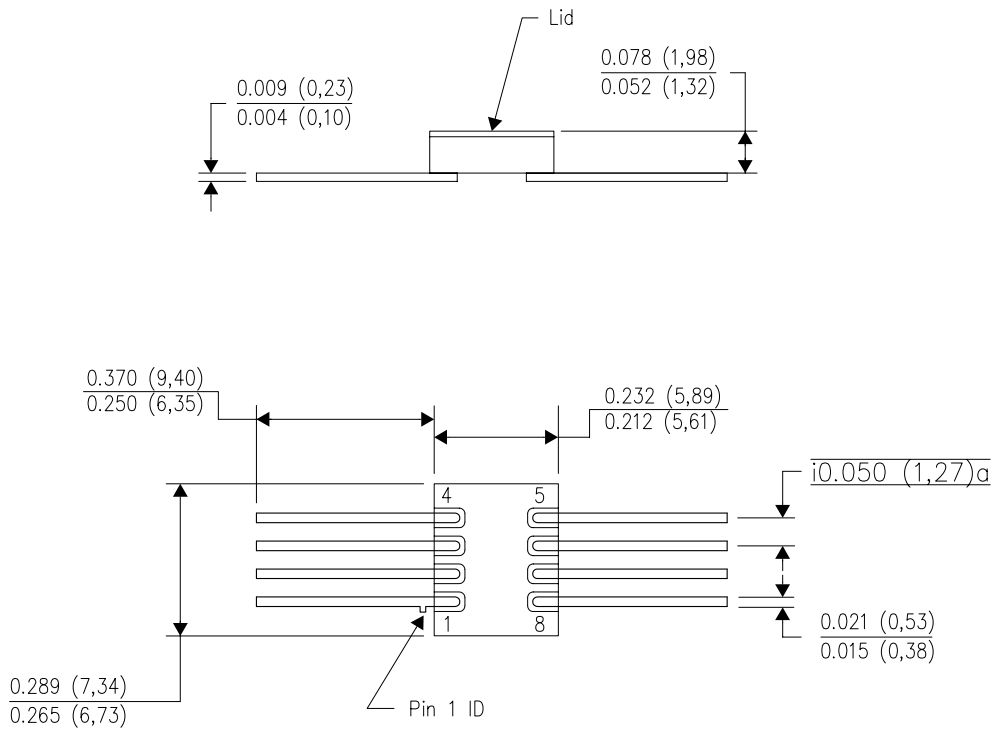
OTHER QUALIFIED VERSIONS OF ADS8320-HT :

- Catalog: ADS8320

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

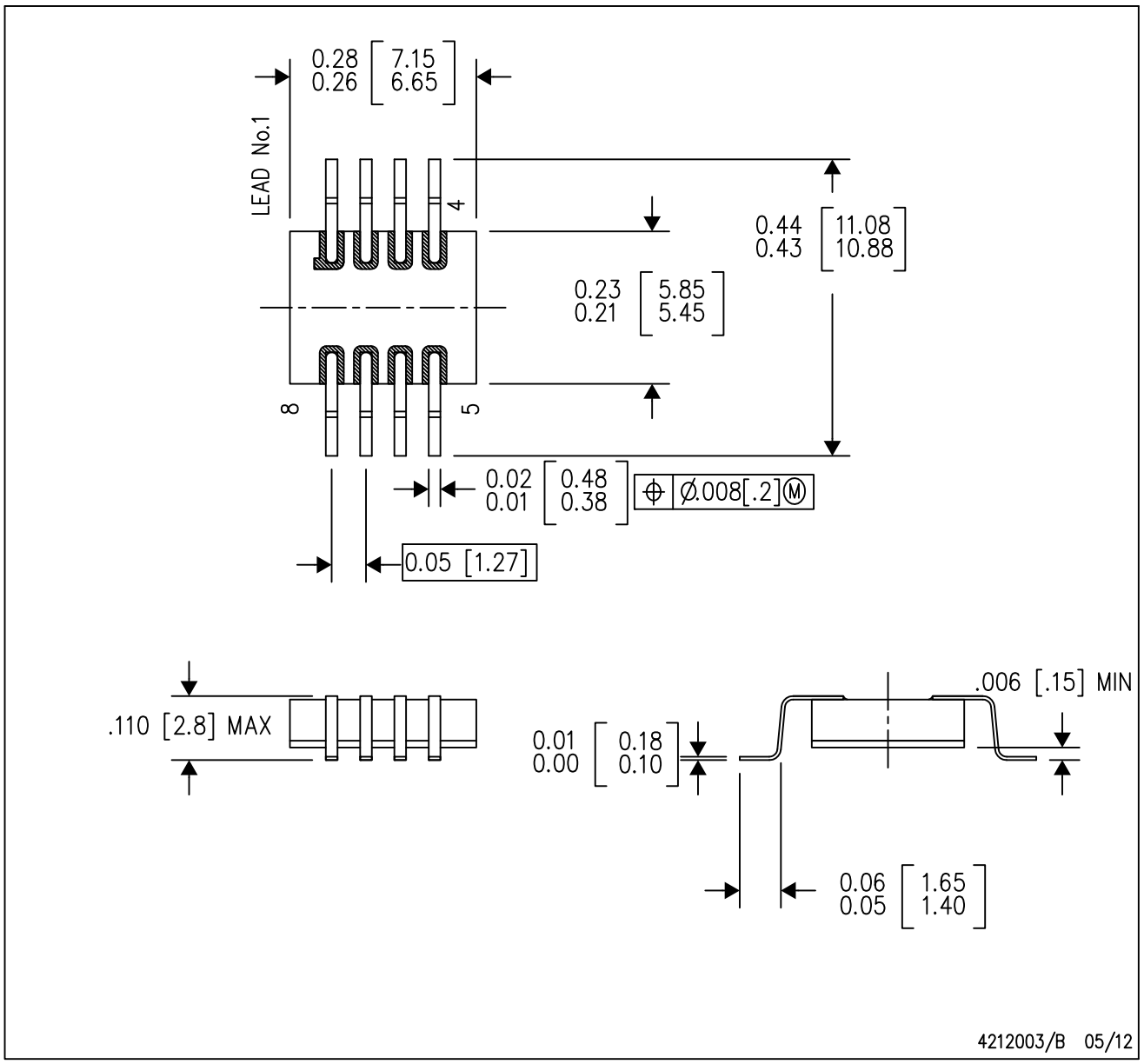
HKJ (R–CDFP–F8) CERAMIC DUAL FLATPACK



4209892/A 10/08

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals will be gold plated.

HKQ (R–CDFP–G8) CERAMIC GULL WING



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals will be gold plated.
E. Lid is not connected to any lead.

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