LM4910 Boomer® Audio Power Amplifier Series Output Capacitor-less Stereo 35mW Headphone Amplifier

Check for Samples: LM4910

FEATURES

- **Eliminates headphone amplifier output coupling capacitors**
- **Eliminates half-supply bypass capacitor**
- **Advanced pop & click circuitry eliminates noises during turn-on and turn-off**
- **Ultra-low current shutdown mode**
- **Unity-gain stable**
- **2.2V - 5.5V operation**
- **Available in space-saving MSOP, LLP, and SOIC packages**

APPLICATIONS

- **Mobile Phones**
- **PDAs**
- **Portable electronics devices**
- **Portable MP3 players**

DESCRIPTION

The LM4910 is an audio power amplifier primarily designed for headphone applications in portable device applications. It is capable of delivering 35mW of continuous average power to a 32Ω load with less than 1% distortion (THD+N) from a 3.3V_{DC} power supply.

The LM4910 utilizes a new circuit topology that eliminates output coupling capacitors and half-supply bypass capacitors. The LM4910 contains advanced pop & click circuitry which eliminates noises caused by transients that would otherwise occur during turn-on and turn-off.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. Since the LM4910 does not require any output coupling capacitors, half-supply bypass capacitors, or bootstrap capacitors, it is ideally suited for low-power portable applications where minimal space and power consumption are primary requirements.

The LM4910 features a low-power consumption shutdown mode, activated by driving the shutdown pin with logic low. Additionally, the LM4910 features an internal thermal shutdown protection mechanism. The LM4910 is also unity-gain stable and can be configured by external gain-setting resistors.

Table 1. Key Specifications

	VALUE	UNIT
PSRR at f = 217Hz	65	dB (typ)
Power Output at V_{DD} = 3.3V, R_L = 32Ω, and THD ≤ 1%	35	mW (typ)
Shutdown Current	0.1	µA (typ)

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Typical Application

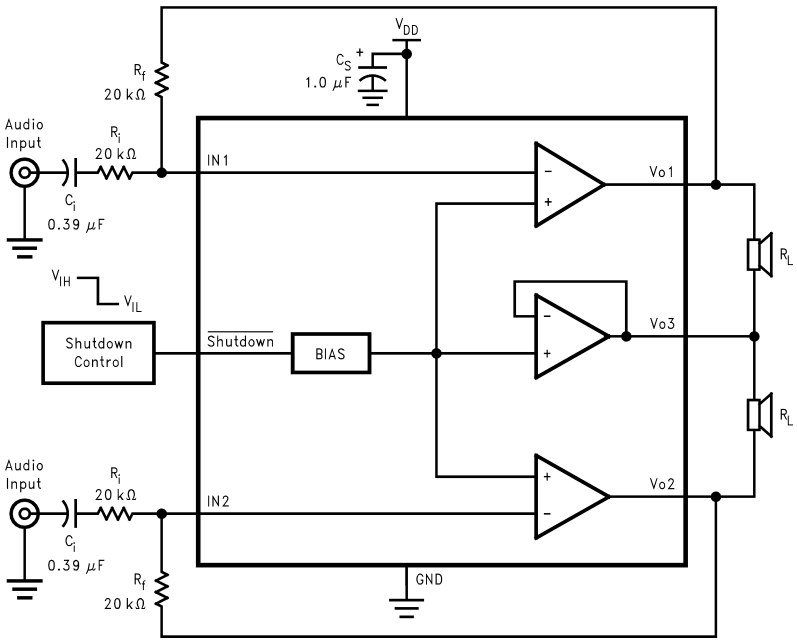

Figure 1. Typical Audio Amplifier Application Circuit

Connection Diagram

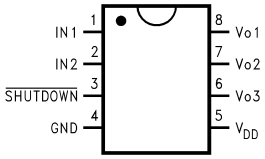

Figure 2. MSOP/SO Package Top View

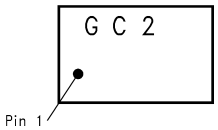

Figure 3. MSOP Marking Top View
G - Boomer Family
C2 - LM4910MM

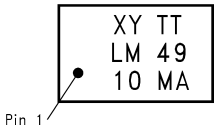

Figure 4. SO Marking Top View
TT - Die Traceability
Bottom 2 lines - Part Number

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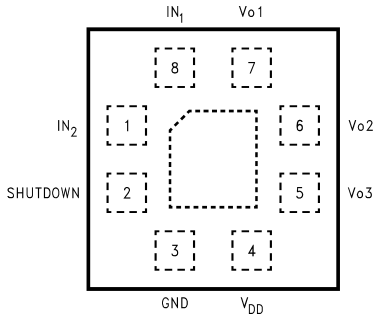

Figure 5. LLP Package Top View

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings [1]

Supply Voltage [2]	6.0V
Storage Temperature	−65°C to +150°C
Input Voltage	-0.3V to V_{DD} + 0.3V
Power Dissipation [3]	Internally Limited
ESD Susceptibility Pin 6 [4]	10kV
ESD Susceptibility [5]	2000V
ESD Susceptibility [6]	200V
Junction Temperature	150°C
Thermal Resistance	
θ_{JC} (MSOP)	56°C/W
θ_{JA} (MSOP)	190°C/W
θ_{JC} (SOP)	35°C/W
θ_{JA} (SOP)	150°C/W
θ_{JC} (LQ)	57°C/W
θ_{JA} (LQ)	140°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) If the product is in shutdown mode and V_{DD} exceeds 6V (to a max of 8V V_{DD}) then most of the excess current will flow through the ESD protection circuits. If the source impedance limits the current to a max of 10ma then the part will be protected. If the part is enabled when V_{DD} is above 6V circuit performance will be curtailed or the part may be permanently damaged.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/ \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4910, see power derating currents for more information.
(4) Human body model, 100pF discharged through a 1.5kΩ resistor, Pin 6 to ground.
(5) Human body model, 100pF discharged through a 1.5kΩ resistor.
(6) Machine Model, 220pF-240pF discharged through all pins.

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le 85°C$
Supply Voltage (V_{DD})	$2.2V \le V_{CC} \le 5.5V$

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Electrical Characteristics V_{DD} = 3.3V (1) (2)

The following specifications apply for V_{DD} = 3.3V, A_V = 1, and 32Ω load unless otherwise specified. Limits apply to T_A = 25°C.

Symbol	Parameter	Conditions	LM4910		Units (Limits)
			Typ (3)	Limit (4) (5)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, 32Ω Load	3.5	6	mA (max)
I_{SD}	Standby Current	$V_{SHUTDOWN}$ = GND	0.1	1.0	µA (max)
V_{OS}	Output Offset Voltage		5	30	mV (max)
P_O	Output Power	THD = 1% (max); f = 1kHz	35	30	mW (min)
THD+N	Total Harmonic Distortion + Noise	P_O = 30mW$_{rms}$; f = 1kHz	0.3		%
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV$_{p-p}$ sinewave Input terminated with 10Ω to ground	65 (f = 217Hz) 65 (f = 1kHz)		dB
V_{IH}	Shutdown Input Voltage High			1.5	V (min)
V_{IL}	Shutdown Input Voltage Low			0.4	V (max)

(1) All voltages are measured with respect to the GND pin unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

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Electrical Characteristics V_{DD} = 3V (1) (2)

The following specifications apply for V_{DD} = 3V, A_V = 1, and 32Ω load unless otherwise specified. Limits apply to T_A = 25°C.

Symbol	Parameter	Conditions	LM4910		Units (Limits)
			Typ (3)	Limit (4) (5)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, 32Ω Load	3.3	6	mA (max)
I_{SD}	Standby Current	$V_{SHUTDOWN}$ = GND	0.1	1.0	µA (max)
V_{OS}	Output Offset Voltage		5	30	mV (max)
P_O	Output Power	THD = 1% (max); f = 1kHz	30	25	mW (min)
THD+N	Total Harmonic Distortion + Noise	P_O = 25mW$_{rms}$; f = 1kHz	0.3		%
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV$_{p-p}$ sinewave Input terminated with 10Ω to ground	65 (f = 217 Hz) 65 (f = 1kHz)		dB
V_{IH}	Shutdown Input Voltage High			1.5	V (min)
V_{IL}	Shutdown Input Voltage Low			0.4	V (max)

(1) All voltages are measured with respect to the GND pin unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.
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Electrical Characteristics V_{DD} = 2.6V (1) (2)

The following specifications apply for V_{DD} = 2.6V, A_V = 1, and 32Ω load unless otherwise specified. Limits apply to T_A = 25°C.

Symbol	Parameter	Conditions	LM4910		Units (Limits)
			Typ (3)	Limit (4) (5)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, 32Ω Load	3.0		mA (max)
I_{SD}	Standby Current	$V_{SHUTDOWN}$ = GND	0.1		µA (max)
V_{OS}	Output Offset Voltage		5		mV (max)
P_O	Output Power	THD = 1% (max); f = 1kHz	13		mW
THD+N	Total Harmonic Distortion + Noise	P_O = 10mW_{rms}; f = 1kHz	0.3		%
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{p-p} sinewave Input terminated with 10Ω to ground	55 (f = 217Hz) 55 (f = 1kHz)		dB

(1) All voltages are measured with respect to the GND pin unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

External Components Description

(Figure 1)

Components		Functional Description
1.	R_I	Inverting input resistance which sets the closed-loop gain in conjunction with R_f. This resistor also forms a high-pass filter with C_i at $f_c = 1/(2\pi R_i C_i)$.
2.	C_I	Input coupling capacitor which blocks the DC voltage at the amplifier's input terminals. Also creates a high-pass filter with R_i at $f_c = 1/(2\pi R_i C_i)$. Refer to the section **Proper Selection of External Components,** for an explanation of how to determine the value of C_i.
3.	R_f	Feedback resistance which sets the closed-loop gain in conjunction with R_i.
4.	C_S	Supply bypass capacitor which provides power supply filtering. Refer to the **Power Supply Bypassing** section for information concerning proper placement and selection of the supply bypass capacitor.

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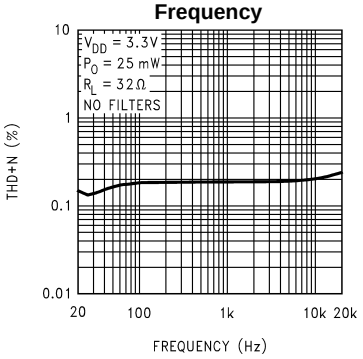
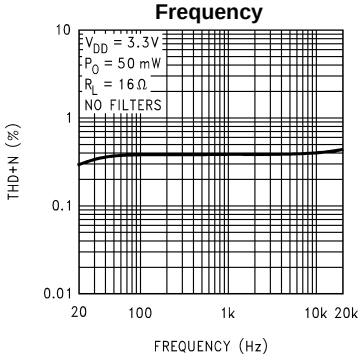
Typical Performance Characteristics

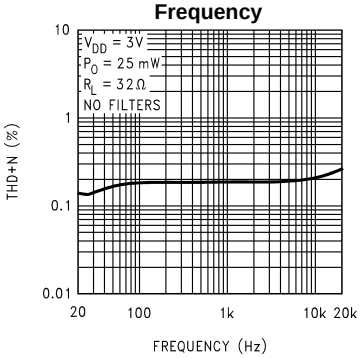
THD+N vs Frequency



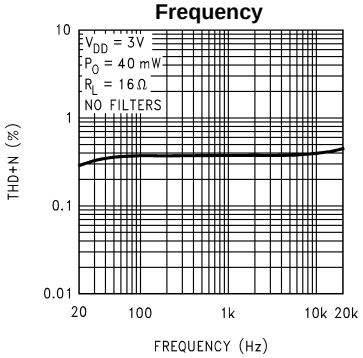
THD+N vs Frequency



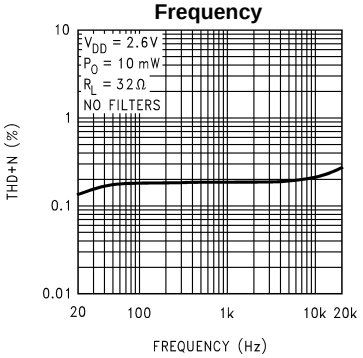
THD+N vs Frequency



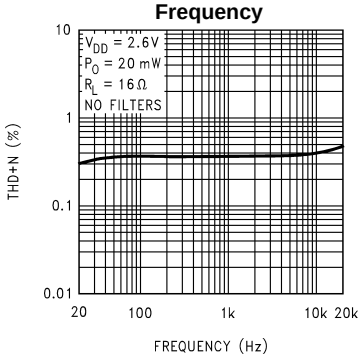
THD+N vs Frequency



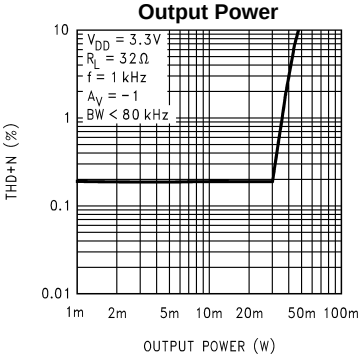
THD+N vs Frequency



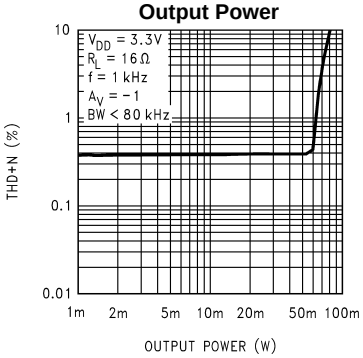
THD+N vs Frequency



THD+N vs Output Power



THD+N vs Output Power



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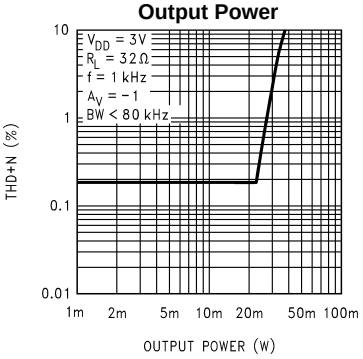
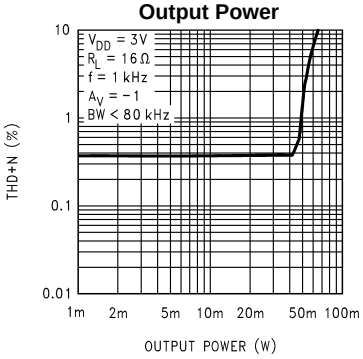
Typical Performance Characteristics (continued)

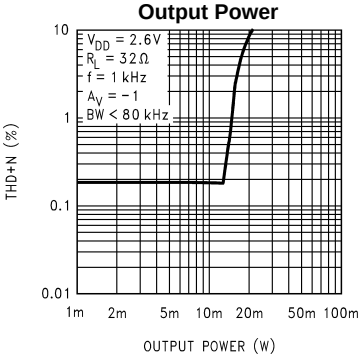
THD+N vs Output Power



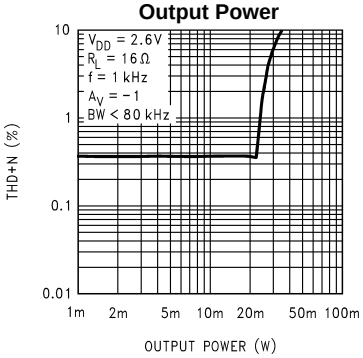
THD+N vs Output Power



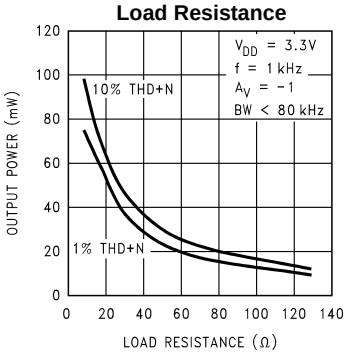
THD+N vs Output Power



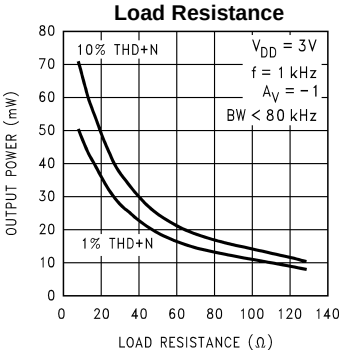
THD+N vs Output Power



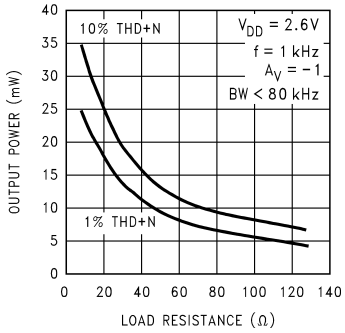
Output Power vs Load Resistance



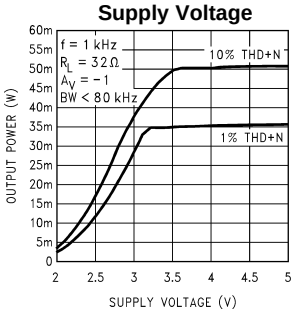
Output Power vs Load Resistance



Output Power vs Load Resistance



Output Power vs Supply Voltage



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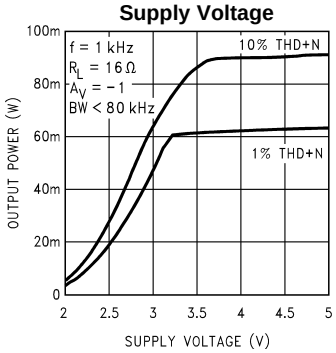
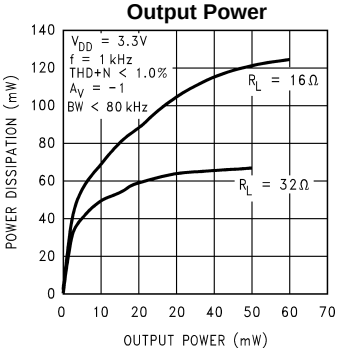
Typical Performance Characteristics (continued)

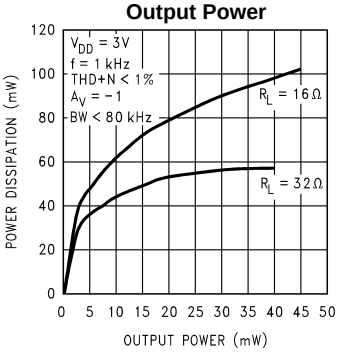
Output Power vs Supply Voltage



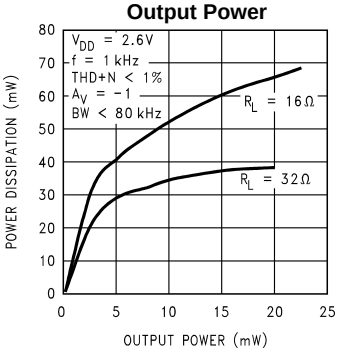
Power Dissipation vs Output Power



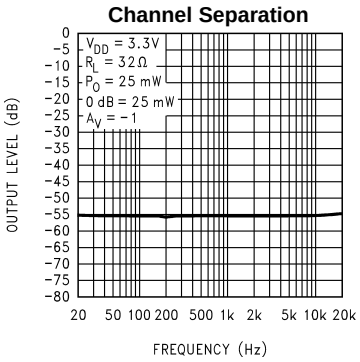
Power Dissipation vs Output Power



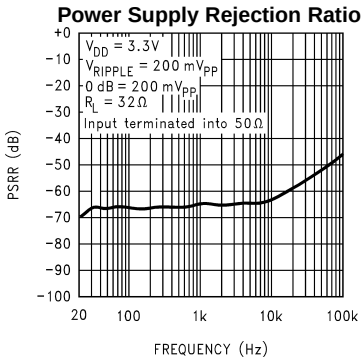
Power Dissipation vs Output Power



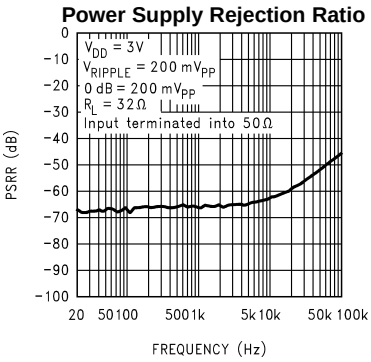
Channel Separation



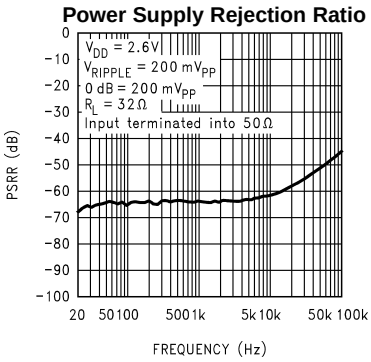
Power Supply Rejection Ratio



Power Supply Rejection Ratio



Power Supply Rejection Ratio



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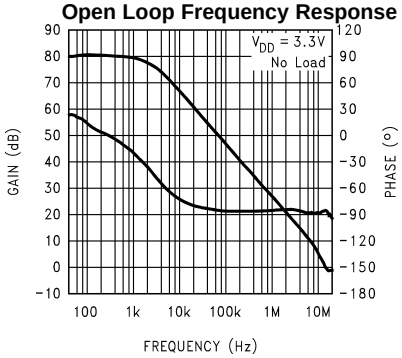
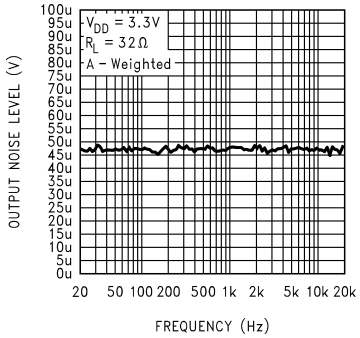
Typical Performance Characteristics (continued)

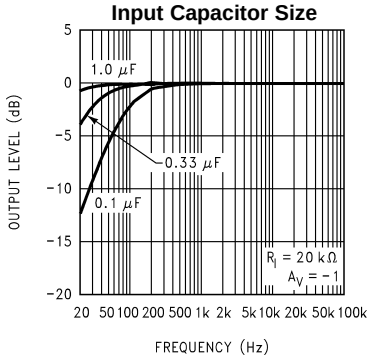
Open Loop Frequency Response



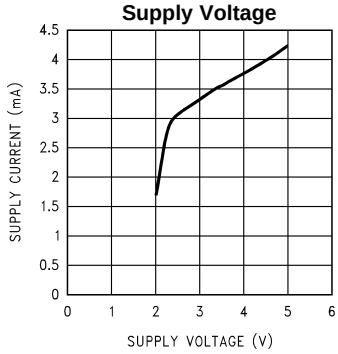
Noise Floor



Frequency Response vs Input Capacitor Size



Supply Current vs Supply Voltage



Application Information

ELIMINATING OUTPUT COUPLING CAPACITORS

Typical single-supply audio amplifiers that drive single-ended (SE) headphones use a coupling capacitor on each SE output. This output coupling capacitor blocks the half-supply voltage to which the output amplifiers are typically biased and couples the audio signal to the headphones. The signal return to circuit ground is through the headphone jack's sleeve.

The LM4910 eliminates these output coupling capacitors. Amp3 is internally configured to apply a bandgap referenced voltage (V_{REF} = 1.58V) to a stereo headphone jack's sleeve. This voltage matches the quiescent voltage present on the Amp1 and Amp2 outputs that drive the headphones. The headphones operate in a manner similar to a bridge-tied-load (BTL). The same DC voltage is applied to both headphone speaker terminals. This results in no net DC current flow through the speaker. AC current flows through a headphone speaker as an audio signal's output amplitude increases on the speaker's terminal.

The headphone jack's sleeve is not connected to circuit ground. Using the headphone output jack as a line-level output will place the LM4910's bandgap referenced voltage on a plug's sleeve connection. This presents no difficulty when the external equipment uses capacitively coupled inputs. For the very small minority of equipment that is DC-coupled, the LM4910 monitors the current supplied by the amplifier that drives the headphone jack's sleeve. If this current exceeds 500mA_{PK}, the amplifier is shutdown, protecting the LM4910 and the external equipment.

ELIMINATING THE HALF-SUPPLY BYPASS CAPACITOR

Typical single-supply audio amplifers are normally biased to 1/2V_{DD} in order to maximize the output swing of the audio signal. This is usually achieved with a simple resistor divider network from V_{DD} to ground that provides the proper bias voltage to the amplifier. However, this scheme requires the use of a half-supply bypass capacitor to improve the bias voltage's stability and the amplifier's PSRR performance.

The LM4910 utilizes an internally generated, buffered bandgap reference voltage as the amplifier's bias voltage. This bandgap reference voltage is not a direct function of V_{DD} and therefore is less susceptible to noise or ripple on the power supply line. This allows for the LM4910 to have a stable bias voltage and excellent PSRR performance even without a half-supply bypass capacitor.

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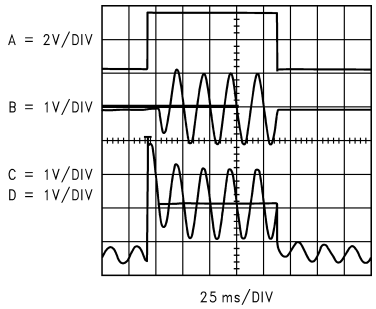
OUTPUT TRANSIENT ('CLICK AND POPS') ELIMINATED

The LM4910 contains advanced circuitry that virtually eliminates output transients ('clicks and pops'). This circuitry prevents all traces of transients when the supply voltage is first applied or when the part resumes operation after coming out of shutdown mode. The LM4910 remains in a muted condition until there is sufficient input signal magnitude (>5mV_{RMS}, typ) to mask any remaining transient that may occur. Figure 2 shows the LM4910's lack of transients in the differential signal (Trace B) across a 320 load. The LM4910's active-low $\overline{\text{SHUTDOWN}}$ pin is driven by the logic signal shown in Trace A. Trace C is the V_{O1} output signal and Trace D is the V_{O3} output signal.

To ensure optimal click and pop performance under low gain configurations (less than 0dB), it is critical to minimize the RC combination of the feedback resistor R_F and stray input capacitance at the amplifier inputs. A more reliable way to lower gain or reduce power delivered to the load is to place a current limiting resistor in series with the load as explained in the **Minimizing Output Noise / Reducing Output Power** section.



AMPLIFIER CONFIGURATION EXPLANATION

As shown in Figure 1, the LM4910 has three operational amplifiers internally. Two of the amplifier's have externally configurable gain while the other amplifier is internally fixed at the bias point acting as a unity-gain buffer. The closed-loop gain of the two configurable amplifiers is set by selecting the ratio of R_f to R_i. Consequently, the gain for each channel of the IC is

$$A_V = -(R_f/R_i) \quad (1)$$

By driving the loads through outputs V_{O1} and V_{O2} with V_{O3} acting as a buffered bias voltage the LM4910 does not require output coupling capacitors. The typical single-ended amplifier configuration where one side of the load is connected to ground requires large, expensive output coupling capacitors.

A configuration such as the one used in the LM4910 has a major advantage over single supply, single-ended amplifiers. Since the outputs V_{O1}, V_{O2}, and V_{O3} are all biased at V_{REF} = 1.58V, no net DC voltage exists across each load. This eliminates the need for output coupling capacitors that are required in a single-supply, single-ended amplifier configuration. Without output coupling capacitors in a typical single-supply, single-ended amplifier, the bias voltage is placed across the load resulting in both increased internal IC power dissipation and possible loudspeaker damage.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. The maximum power dissipation for a given application can be derived from the power dissipation graphs or from Equation 1.

$$P_{DMAX} = 4(V_{DD})^2 / (\pi^2 R_L) \quad (2)$$

It is critical that the maximum junction temperature T_{JMAX} of 150°C is not exceeded. Since the typical application is for headphone operation (32Ω impedance) using a 3.3V supply the maximum power dissipation is only 138mW. Therefore, power dissipation is not a major concern.

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POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is important for low noise performance and high power supply rejection. The capacitor location on the power supply pins should be as close to the device as possible.

Typical applications employ a 3.3V regulator with 10µF tantalum or electrolytic capacitor and a ceramic bypass capacitor which aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the LM4910. A bypass capacitor value in the range of 0.1µF to 1µF is recommended for C_S.

MICRO POWER SHUTDOWN

The voltage applied to the $\overline{\text{SHUTDOWN}}$ pin controls the LM4910's shutdown function. Activate micro-power shutdown by applying a logic-low voltage to the $\overline{\text{SHUTDOWN}}$ pin. When active, the LM4910's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. The trigger point is 0.4V(max) for a logic-low level, and 1.5V(min) for a logic-high level. The low 0.1µA(typ) shutdown current is achieved by applying a voltage that is as near as ground as possible to the $\overline{\text{SHUTDOWN}}$ pin. A voltage that is higher than ground may increase the shutdown current.

There are a few ways to control the micro-power shutdown. These include using a single-pole, single-throw switch, a microprocessor, or a microcontroller. When using a switch, connect an external 100kΩ pull-up resistor between the $\overline{\text{SHUTDOWN}}$ pin and V_{DD}. Connect the switch between the $\overline{\text{SHUTDOWN}}$ pin and ground. Select normal amplifier operation by opening the switch. Closing the switch connects the $\overline{\text{SHUTDOWN}}$ pin to ground, activating micro-power shutdown. The switch and resistor guarantee that the $\overline{\text{SHUTDOWN}}$ pin will not float. This prevents unwanted state changes. In a system with a microprocessor or microcontroller, use a digital output to apply the control voltage to the $\overline{\text{SHUTDOWN}}$ pin. Driving the $\overline{\text{SHUTDOWN}}$ pin with active circuitry eliminates the pull-up resistor.

SELECTING EXTERNAL COMPONENTS

Selecting proper external components in applications using integrated power amplifiers is critical to optimize device and system performance. While the LM4910 is tolerant of external component combinations, consideration to component values must be used to maximize overall system quality.

The LM4910 is unity-gain stable which gives the designer maximum system flexibility. The LM4910 should be used in low gain configurations to minimize THD+N values, and maximize the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than $1V_{rms}$ are available from sources such as audio codecs. Very large values should not be used for the gain-setting resistors. Values for R_i and R_f should be less than 1MΩ. Please refer to the section, **Audio Power Amplifier Design**, for a more complete explanation of proper gain selection

Besides gain, one of the major considerations is the closed-loop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in Figure 1. The input coupling capacitor, C_i, forms a first order high pass filter which limits low frequency response. This value should be chosen based on needed frequency response and turn-on time.

SELECTION OF INPUT CAPACITOR SIZE

Amplifiying the lowest audio frequencies requires a high value input coupling capacitor, C_i. A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the headphones used in portable systems have little ability to reproduce signals below 60Hz. Applications using headphones with this limited frequency response reap little improvement by using a high value input capacitor.

In addition to system cost and size, turn-on time is affected by the size of the input coupling capacitor Ci. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage. This charge comes from the output via the feedback Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on time can be minimized. A small value of Ci (in the range of 0.1µF to 0.39µF), is recommended.

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USING EXTERNAL POWERED SPEAKERS

The LM4910 is designed specifically for headphone operation. Often the headphone output of a device will be used to drive external powered speakers. The LM4910 has a differential output to eliminate the output coupling capacitors. The result is a headphone jack sleeve that is connected to V_{O3} instead of GND. For powered speakers that are designed to have single-ended signals at the input, the click and pop circuitry will not be able to eliminate the turn-on/turn-off click and pop. Unless the inputs to the powered speakers are fully differential the turn-on/turn-off click and pop will be very large.

AUDIO POWER AMPLIFIER DESIGN

A 30mW/32Ω Audio Amplifier

Given:	
Power Output	30mWrms
Load Impedance	32Ω
Input Level	1Vrms
Input Impedance	20kΩ

A designer must first determine the minimum supply rail to obtain the specified output power. By extrapolating from the Output Power vs Supply Voltage graphs in the **Typical Performance Characteristics** section, the supply rail can be easily found.

Since 3.3V is a standard supply voltage in most applications, it is chosen for the supply rail in this example. Extra supply voltage creates headroom that allows the LM4910 to reproduce peaks in excess of 30mW without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does no violate the conditions explained in the **Power Dissipation** section.

Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation 2.

$$A_V \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \tag{3}$$

From Equation 2, the minimum A_V is 0.98; use A_V = 1. Since the desired input impedance is 20kΩ, and with A_V equal to 1, a ratio of 1:1 results from Equation 1 for R_f to R_i. The values are chosen with R_i = 20kΩ and R_f = 20kΩ.

The last step in this design example is setting the amplifier's −3dB frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at least one-fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well within the ±0.25dB desired limit. The results are an

$$f_L = 100Hz/5 = 20Hz \tag{4}$$

and an

$$f_H = 20kHz \times 5 = 100kHz \tag{5}$$

As mentioned in the **Selecting Proper External Components** section, R_i and C_i create a highpass filter that sets the amplifier's lower bandpass frequency limit. Find the coupling capacitor's value using Equation (3).

$$C_i \geq 1/(2\pi R_i f_L) \tag{6}$$

The result is

$$1/(2\pi*20k\Omega*20Hz) = 0.397\mu F \quad (7)$$

Use a 0.39µF capacitor, the closest standard value.

The high frequency pole is determined by the product of the desired frequency pole, f_H, and the differential gain, A_V. With an A_V = 1 and f_H = 100kHz, the resulting GBWP = 100kHz which is much smaller than the LM4910 GBWP of 11MHz. This figure displays that if a designer has a need to design an amplifier with higher differential gain, the LM4910 can still be used without running into bandwidth limitations.

MINIMIZING OUTPUT NOISE / REDUCING OUTPUT POWER

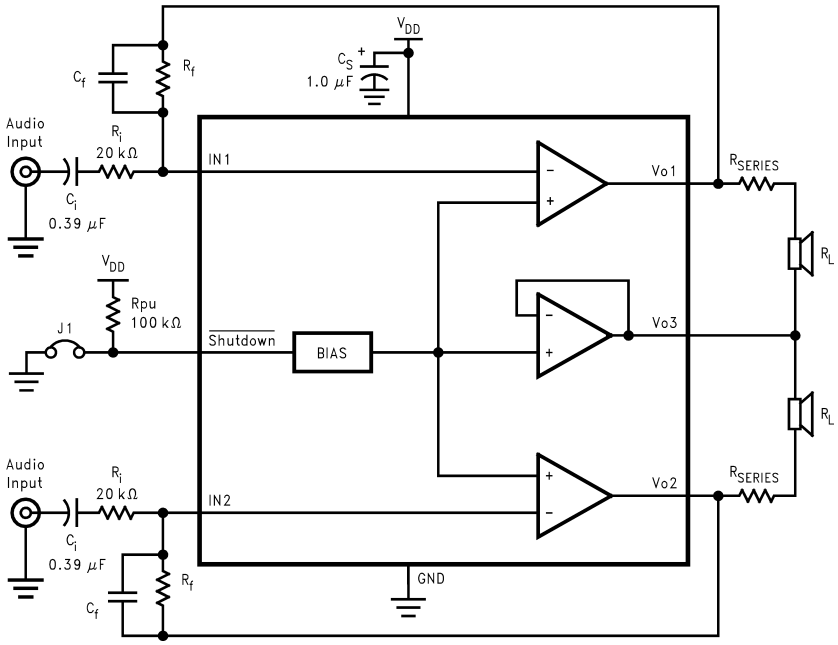

Figure 6.

Output noise delivered to the load can be minimized with the use of an external resistor, R_{SERIES}, placed in series with each load as shown in Figure 6. R_{SERIES} forms a voltage divider with the impedance of the headphone driver R_L. As a result, output noise is attenuated by the factor R_L / (R_L + R_{SERIES}). Figure 7 illustrates the relationship between output noise and R_{SERIES} for different loads. R_{SERIES} also decreases output power delivered to the load by the factor R_L / (R_L + R_{SERIES})^2. However, this may not pose a problem since most headphone applications require less than 10mW of output power. Figure 9 illustrates output power (@1% THD+N) vs R_{SERIES} for different loads.

Figure 7 shows an optional resistor connected between the amplifier output that drives the headphone jack sleeve and ground. This resistor provides a ground path that supressed power supply hum. This hum may occur in applications such as notebook computers in a shutdown condition and connected to an external powered speaker. The resistor's 100Ω value is a suggested starting point. Its final value must be determined based on the tradeoff between the amount of noise suppression that may be needed and minimizing the additional current drawn by the resistor (25mA for a 100Ω resistor and a 5V supply).

ESD PROTECTION

As stated in the Absolute Maximum Ratings, pin 6 (V_o3) on the LM4910 has a maximum ESD susceptibility rating of 10kV. For higher ESD voltages, the addition of a PCDN042 dual transil (from California Micro Devices), as shown in Figure 7, will provide additional protection.

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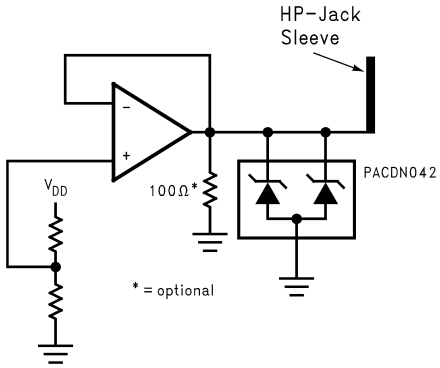


Figure 7. The PCDN042 provides additional ESD protection beyond the 10kV shown in the Absolute Maximum Ratings for the V_o3 output

Figure 8. Output Noise vs R_{SERIES}

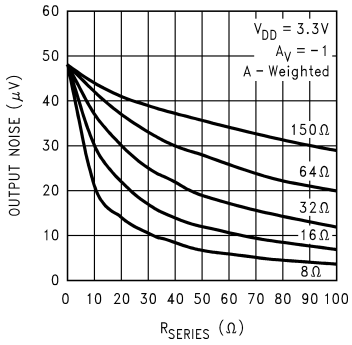


Figure 9.

Figure 10. Output Power vs R_{SERIES}

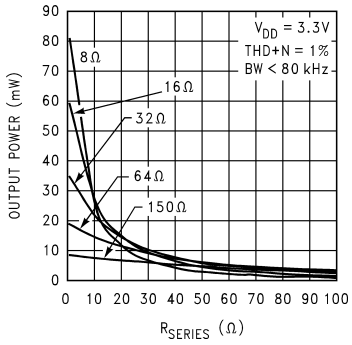
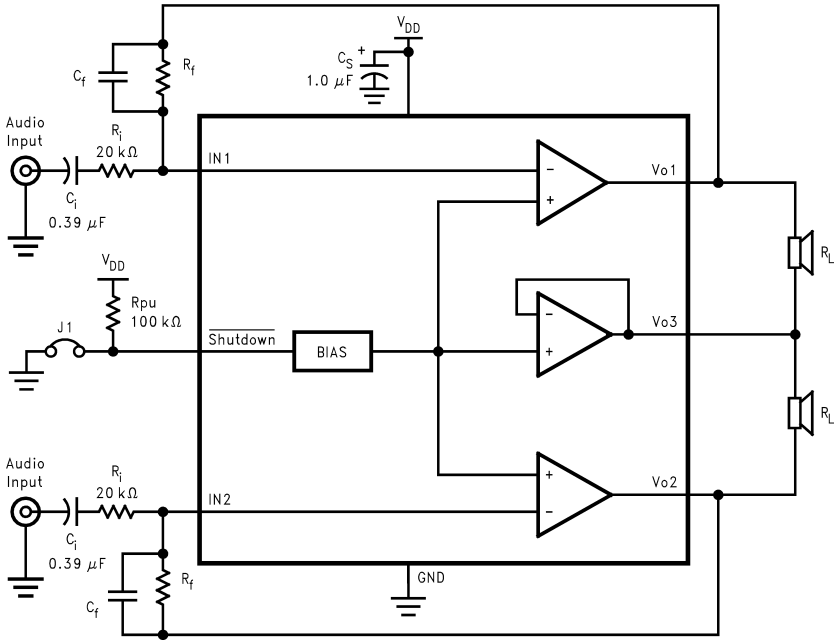


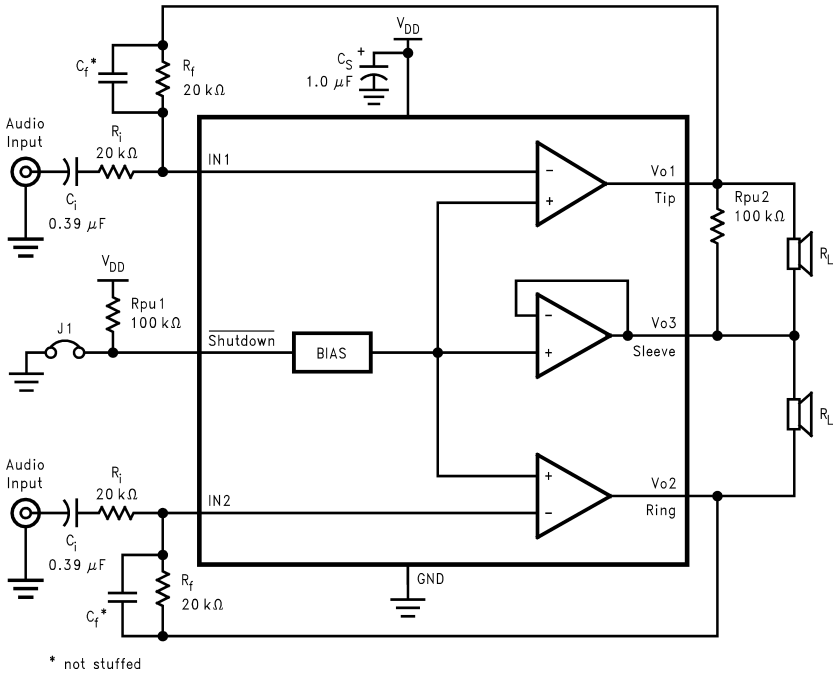
Figure 11.

HIGHER GAIN AUDIO AMPLIFIER



The LM4910 is unity-gain stable and requires no external components besides gain-setting resistors, input coupling capacitors, and proper supply bypassing in the typical application. However, if a very large closed-loop differential gain is required, a feedback capacitor (C_f) may be needed as shown in Figure 11 to bandwidth limit the amplifier. This feedback capacitor creates a low pass filter that eliminates possible high frequency oscillations. Care should be taken when calculating the -3dB frequency in that an incorrect combination of R_f and C_f will cause frequency response roll off before 20kHz. A typical combination of feedback resistor and capacitor that will not produce audio band high frequency roll off is Rf = 20kΩ and C_f = 25pF. These components result in a -3dB point of approximately 320kHz.

REFERENCE DESIGN BOARD and LAYOUT GUIDELINES MSOP & SO BOARDS



(Note: $R_{PU}2$ is not required. It is used for test measurement purposes only.)

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LM4910 SO DEMO BOARD ARTWORK

Figure 12. Composite View

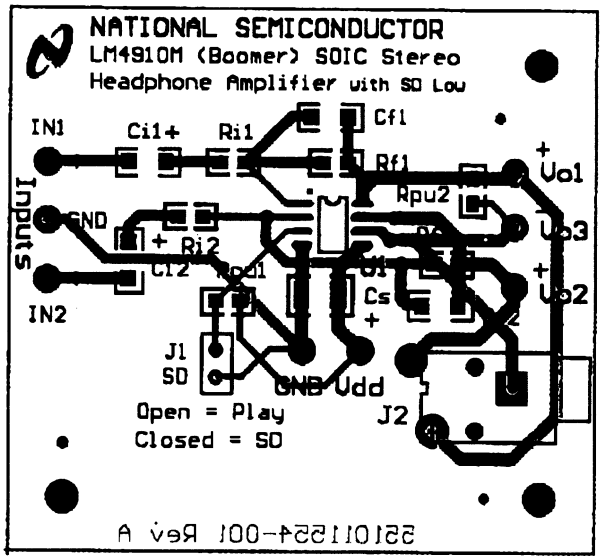


Figure 13. Silk Screen

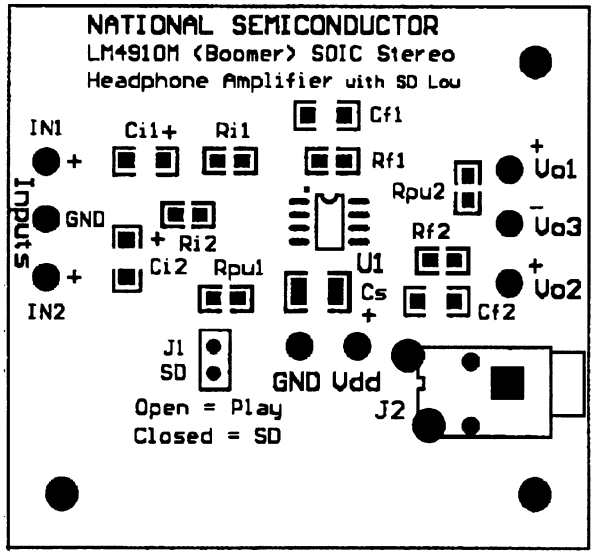


Figure 14. Top Layer

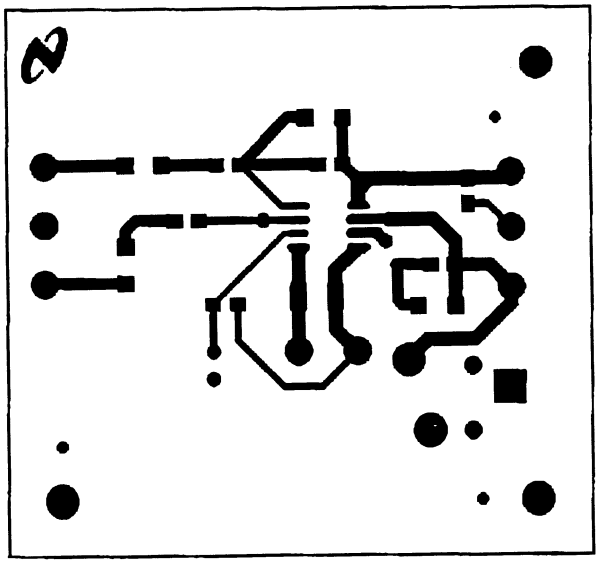
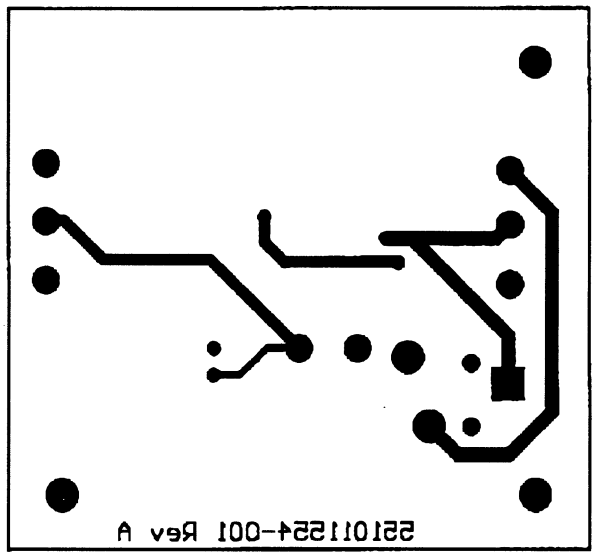


Figure 15. Bottom Layer



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LM4910 MSOP DEMO BOARD ARTWORK

Figure 16. Composite View

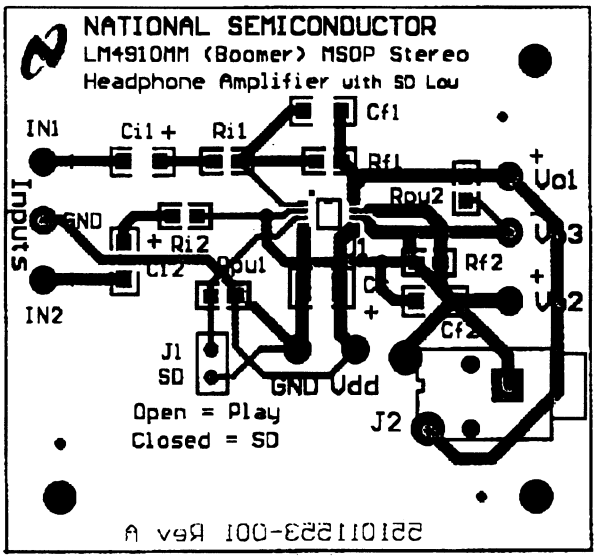


Figure 17. Silk Screen

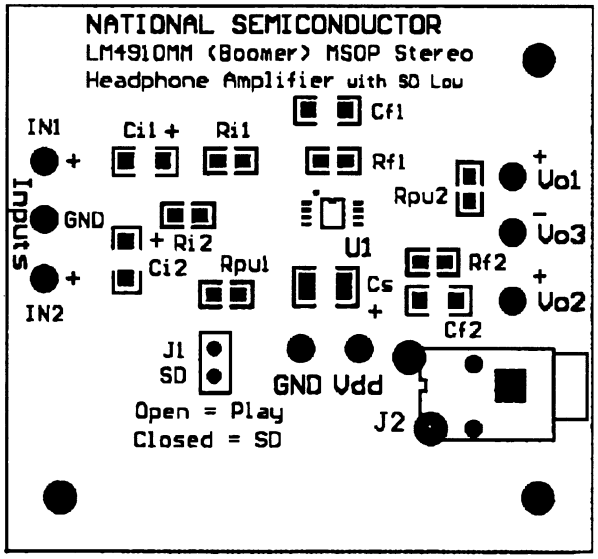


Figure 18. Top Layer

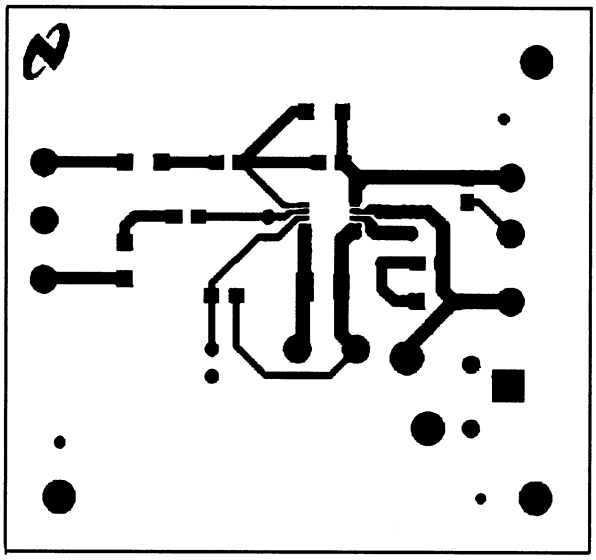
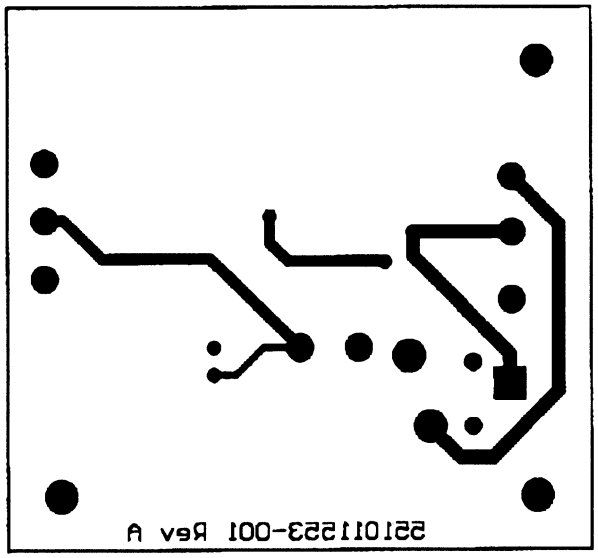


Figure 19. Bottom Layer



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LM4910 LLP DEMO BOARD ARTWORK

Figure 20. Composite View

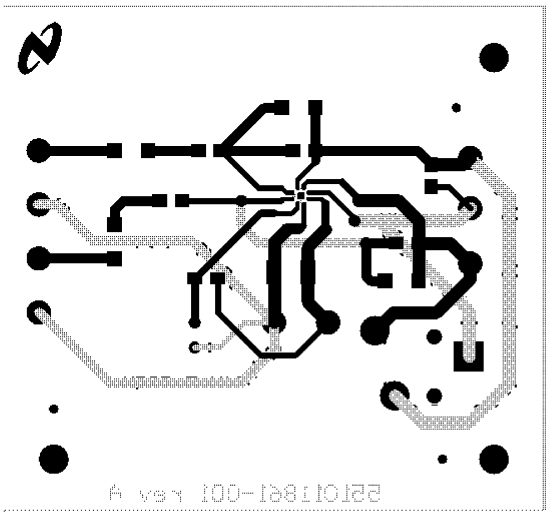


Figure 21. Silk Screen

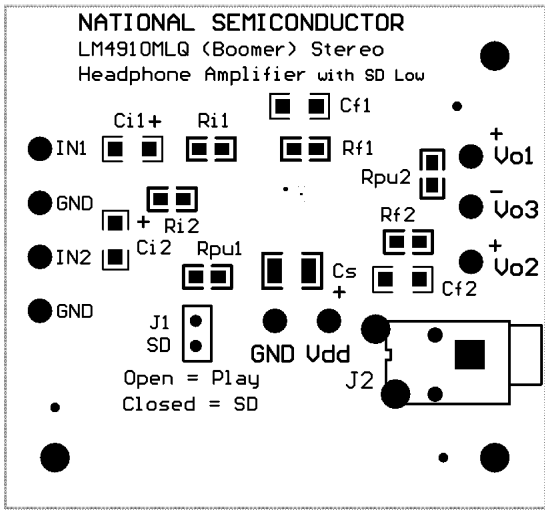


Figure 22. Top Layer

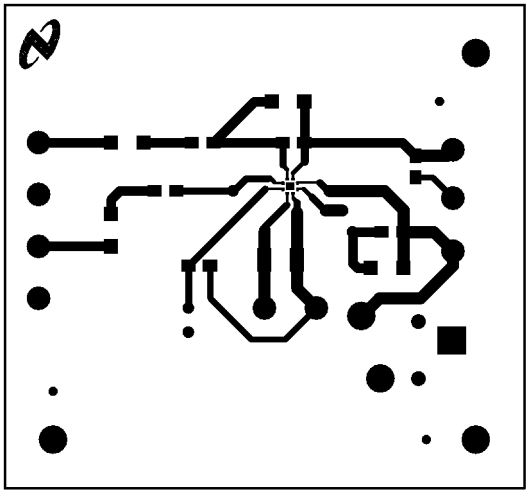
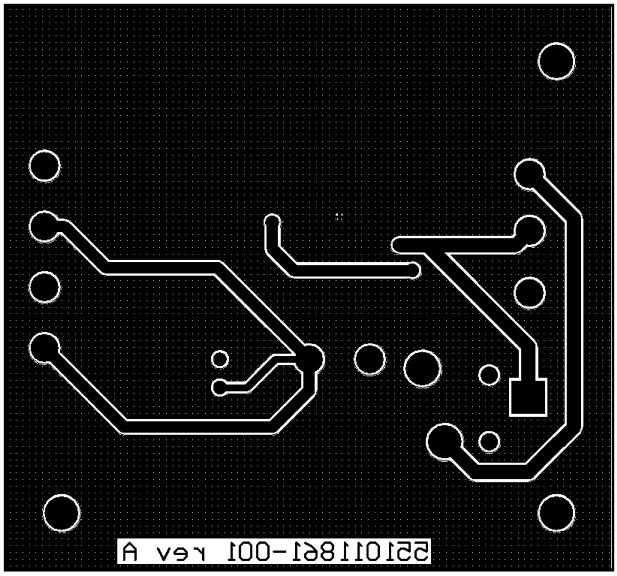


Figure 23. Bottom Layer



LM4910 Reference Design Boards Bill of Materials

Part Description	Qty	Ref Designator
LM4910 Mono Reference Design Board	1	
LM4910 Audio AMP	1	U1
Tantalum Cap 1µF 16V 10	1	Cs
Ceramic Cap 0.39µF 50V Z50 20	2	Ci
Resistor 20kΩ 1/10W 5	4	Ri, Rf
Resistor 100kΩ 1/10W 5	1	Rpu
Jumper Header Vertical Mount 2X1, 0.100	1	J1

PCB LAYOUT GUIDELINES

This section provides practical guidelines for mixed signal PCB layout that involves various digital/analog power and ground traces. Designers should note that these are only "rule-of-thumb" recommendations and the actual results will depend heavily on the final layout.

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Minimization of THD

PCB trace impedance on the power, ground, and all output traces should be minimized to achieve optimal THD performance. Therefore, use PCB traces that are as wide as possible for these connections. As the gain of the amplifier is increased, the trace impedance will have an ever increasing adverse affect on THD performance. At unity-gain (0dB) the parasitic trace impedance effect on THD performance is reduced but still a negative factor in the THD performance of the LM4910 in a given application.

GENERAL MIXED SIGNAL LAYOUT RECOMMENDATION

Power and Ground Circuits

For two layer mixed signal design, it is important to isolate the digital power and ground trace paths from the analog power and ground trace paths. Star trace routing techniques (bringing individual traces back to a central point rather than daisy chaining traces together in a serial manner) can greatly enhance low level signal performance. Star trace routing refers to using individual traces to feed power and ground to each circuit or even device. This technique will require a greater amount of design time but will not increase the final price of the board. The only extra parts required may be some jumpers.

Single-Point Power / Ground Connections

The analog power traces should be connected to the digital traces through a single point (link). A "PI-filter" can be helpful in minimizing high frequency noise coupling between the analog and digital sections. Further, place digital and analog power traces over the corresponding digital and analog ground traces to minimize noise coupling.

Placement of Digital and Analog Components

All digital components and high-speed digital signal traces should be located as far away as possible from analog components and circuit traces.

Avoiding Typical Design / Layout Problems

Avoid ground loops or running digital and analog traces parallel to each other (side-by-side) on the same PCB layer. When traces must cross over each other do it at 90 degrees. Running digital and analog traces at 90 degrees to each other from the top to the bottom side as much as possible will minimize capacitive noise coupling and cross talk.

Revision History

Rev	Date	Description
1.0	7/12/05	Released to the WEB.
1.1	01/16/07	Deleted the phrase “patent pending” on page 1.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM4910LQ/NOPB	ACTIVE	WQFN	NGP	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	GA4	Samples
LM4910MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	GC2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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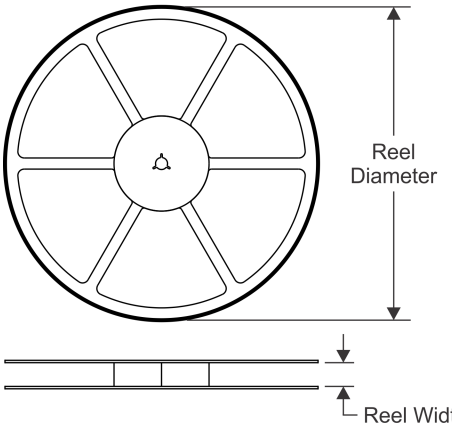
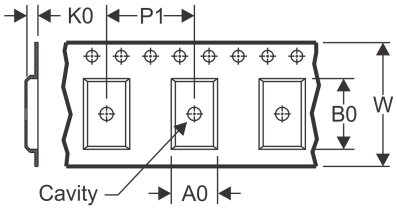
TAPE AND REEL INFORMATION

REEL DIMENSIONS

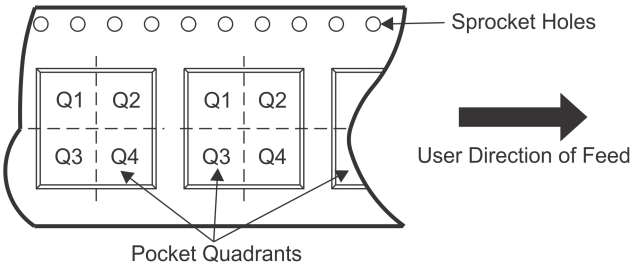


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

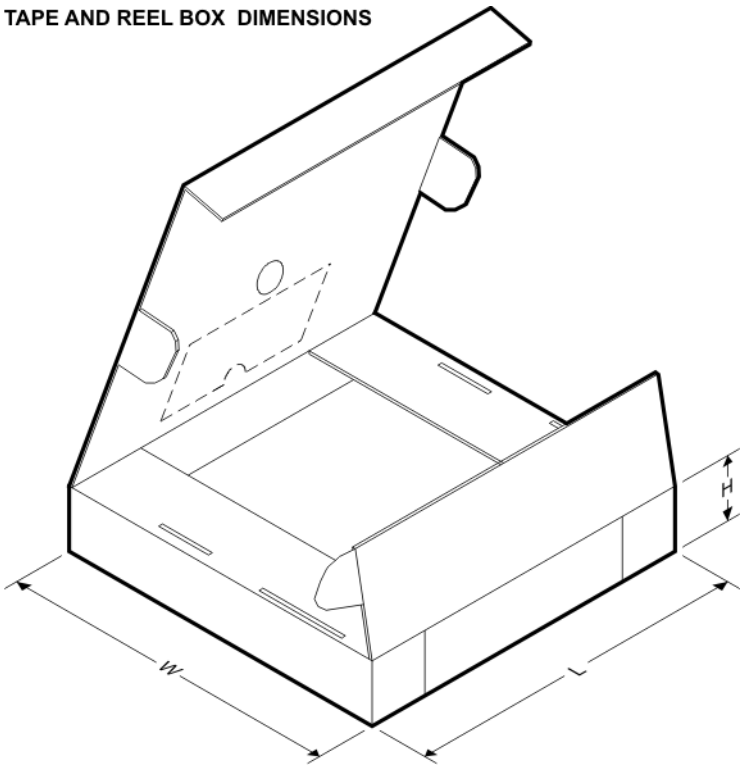
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4910LQ/NOPB	WQFN	NGP	8	1000	178.0	12.4	2.2	2.2	1.0	8.0	12.0	Q1
LM4910MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

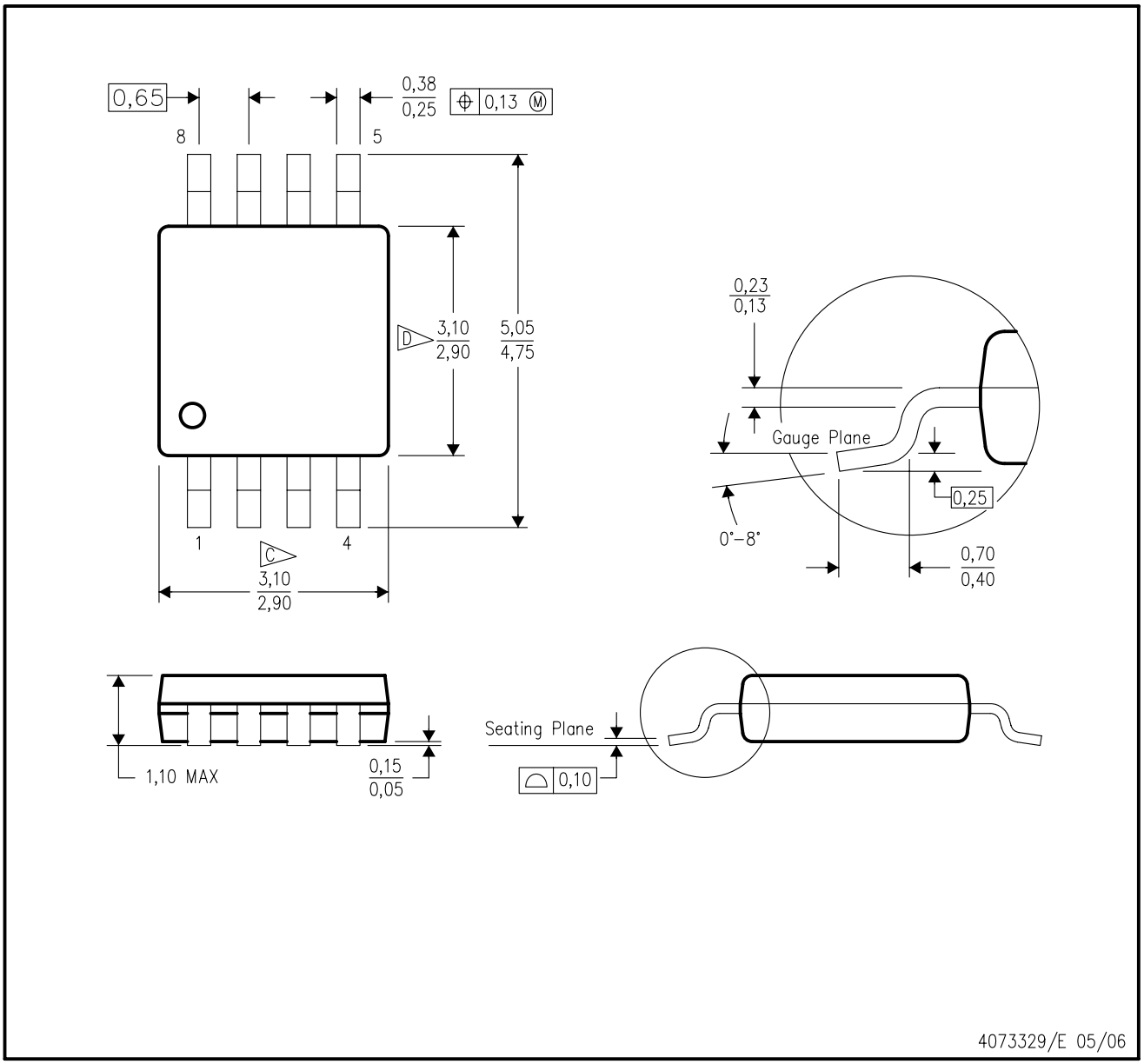
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

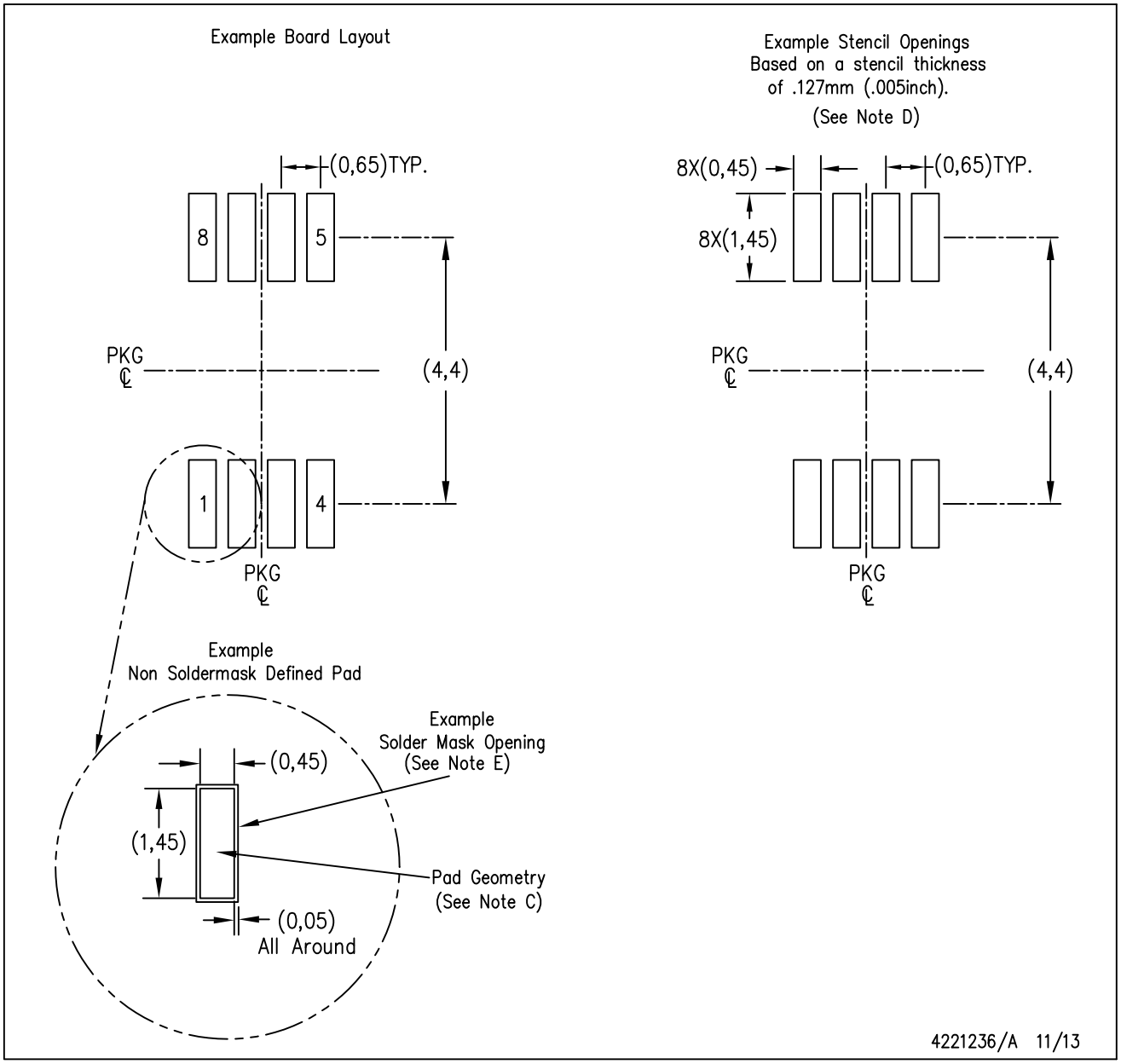
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4910LQ/NOPB	WQFN	NGP	8	1000	210.0	185.0	35.0
LM4910MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE

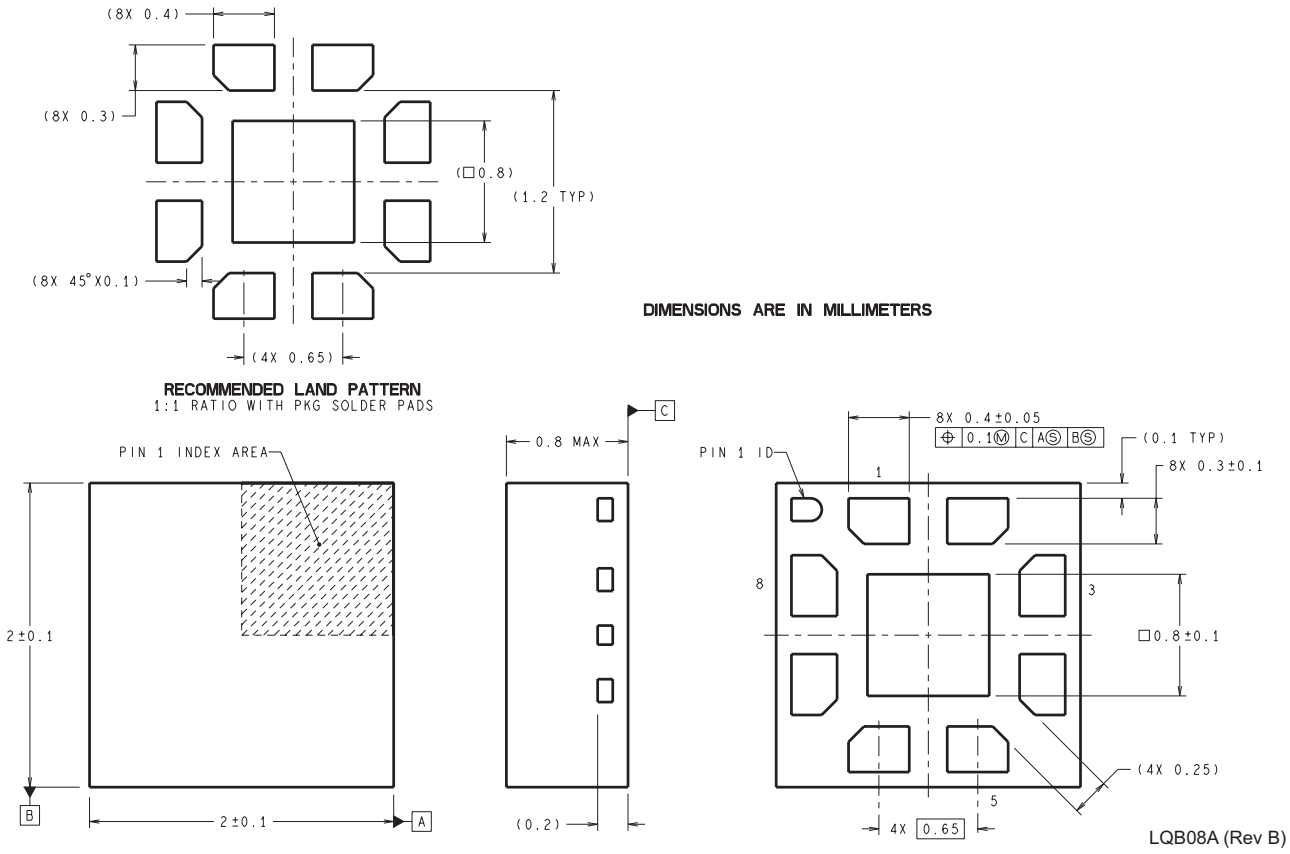


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.


(8X 0.4)
(8X 0.3)
(□0.8)
(1.2 TYP)
(8X 45°X0.1)
(4X 0.65)
RECOMMENDED LAND PATTERN
1:1 RATIO WITH PKG SOLDER PADS
DIMENSIONS ARE IN MILLIMETERS
PIN 1 INDEX AREA
2±0.1
2±0.1
B
A
0.8 MAX
C
(0.2)
PIN 1 ID
8X 0.4±0.05
0.1 M C A S B S
(0.1 TYP)
8X 0.3±0.1
1
8
3
□0.8±0.1
(4X 0.25)
5
4X 0.65
LQB08A (Rev B)

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