

SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT

Check for Samples: [SN74AHC1G126-EP](#)

FEATURES

- Operating Range of 2 V to 5.5 V
- Max t_{pd} of 6 ns at 5 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 8 -mA Output Drive at 5 V
- Latch-Up Performance Exceeds 250 mA Per JESD 17

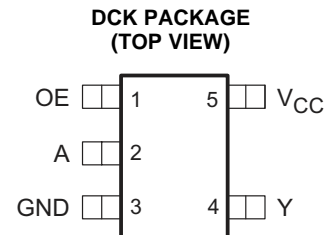
SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly and Test Site
- One Fabrication Site
- Available in Military (-55°C to 125°C) Temperature Range
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

DESCRIPTION

The SN74AHC1G126 is a single bus buffer gate and line driver with 3-state output. The output is disabled when the output-enable (OE) input is low. When OE is high, true data is passed from the A input to the Y output.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.



ORDERING INFORMATION⁽¹⁾

T_J	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
-55°C to 125°C	SOT (SC-70) – DCK	Reel of 250	74AHC1G126MDCKTEP	SLI	V62/14605-01XE

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

Table 1. FUNCTION TABLE

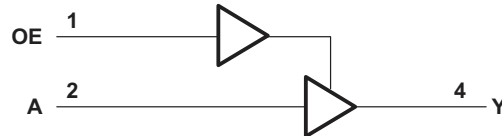
INPUTS		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Z



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LOGIC DIAGRAM (POSITIVE LOGIC)**ABSOLUTE MAXIMUM RATINGS⁽¹⁾**

over operating junction temperature range (unless otherwise noted)

V_{CC}	Supply voltage range		-0.5 V to 7 V
V_I	Input voltage range ⁽²⁾		-0.5 V to 7 V
V_O	Output voltage range ⁽²⁾		-0.5 V to $V_{CC} + 0.5$ V
I_{IK}	Input clamp current	$V_I < 0$	-20 mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$	± 20 mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}	± 25 mA
	Continuous current through V_{CC} or GND		± 50 mA
T_J	Junction temperature range		-55°C to 150°C
T_{stg}	Storage temperature range		-65°C to 150°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		SN74AHC1G126-EP	UNITS
		DCK	
		5 PINS	
θ_{JA}	Junction-to-ambient thermal resistance ⁽²⁾	282.8	°C/W
θ_{JCTop}	Junction-to-case (top) thermal resistance ⁽³⁾	91.1	
θ_{JB}	Junction-to-board thermal resistance ⁽⁴⁾	60.1	
ψ_{JT}	Junction-to-top characterization parameter ⁽⁵⁾	1.6	
ψ_{JB}	Junction-to-board characterization parameter ⁽⁶⁾	59.2	
θ_{JCbott}	Junction-to-case (bottom) thermal resistance ⁽⁷⁾	N/A	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		V
		V _{CC} = 3 V	2.1		
		V _{CC} = 5.5 V	3.85		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5	V
		V _{CC} = 3 V		0.9	
		V _{CC} = 5.5 V		1.65	
V _I	Input voltage		0	5.5	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V		-50	μA
		V _{CC} = 3.3 V ±0.3 V		-4	mA
		V _{CC} = 5 V ±0.5 V		-8	
I _{OL}	Low-level output current	V _{CC} = 2 V		-50	μA
		V _{CC} = 3.3 V ±0.3 V		4	mA
		V _{CC} = 5 V ±0.5 V		8	
Δt/Δv	Input transition rise/fall time	V _{CC} = 3.3 V ±0.3 V		100	ns/V
		V _{CC} = 5 V ±0.5 V		20	
T _J	Operating junction temperature range		-55	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
V _{OH}	I _{OH} = -50 μA	2 V	1.9		V
		3 V	2.9		
		4.5 V	4.4		
	I _{OH} = -4 mA	3 V	2.48		
	I _{OH} = -8 mA	4.5	3.8		
V _{OL}	I _{OH} = 50 μA	2 V		0.1	V
		3 V		0.1	
		4.5 V		0.1	
	I _{OH} = 4 mA	3 V		0.44	
	I _{OH} = 8 mA	4.5		0.44	
I _I	V _I = 5.5 V or GND	0 V to 5.5 V		±1	μA
I _{OZ}	V _O = V _{CC} or GND	5.5 V		±2.5	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V		10	μA
C _i	V _I = V _{CC} or GND	5 V		10	pF

SWITCHING CHARACTERISTICS

over recommended operating junction temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	MIN	MAX	UNIT
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	1	13	ns
t_{PHL}				1	13	ns
t_{PZH}	OE	Y	$C_L = 50\text{ pF}$	1	13	ns
t_{PZL}				1	13	ns
t_{PHZ}	OE	Y	$C_L = 50\text{ pF}$	1	15	ns
t_{PLZ}				1	15	ns

SWITCHING CHARACTERISTICS

over recommended operating junction temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted)

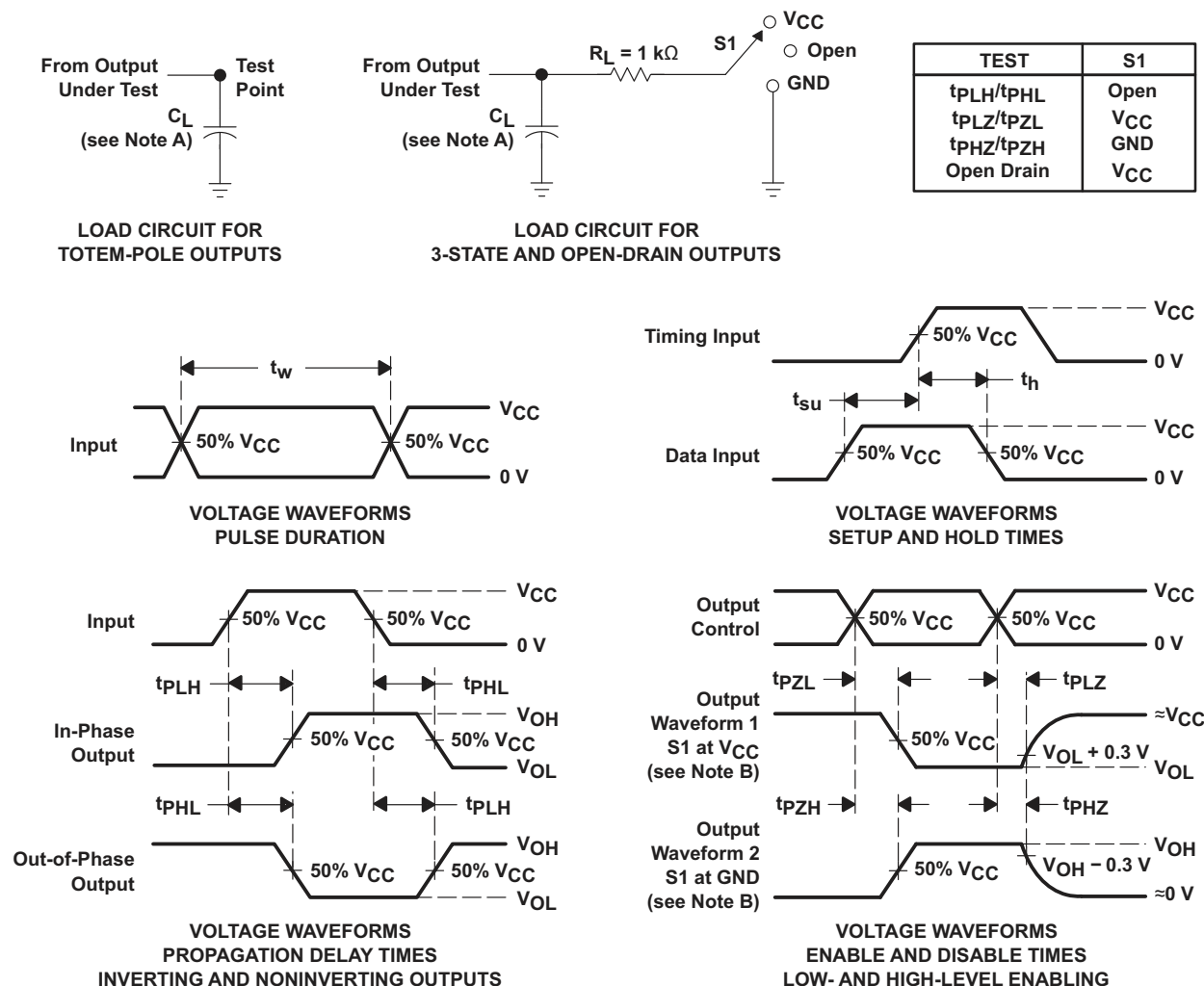
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	MIN	MAX	UNIT
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	1	8.5	ns
t_{PHL}				1	8.5	ns
t_{PZH}	OE	Y	$C_L = 50\text{ pF}$	1	8	ns
t_{PZL}				1	8	ns
t_{PHZ}	OE	Y	$C_L = 50\text{ pF}$	1	10	ns
t_{PLZ}				1	10	ns

OPERATING CHARACTERISTICS

$V_{CC} = 5\text{ V}$, $T_J = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, $f = 1\text{ MHz}$	14	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74AHC1G126MDCKTEP	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	SLI	Samples
V62/14605-01XE	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	SLI	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74AHC1G126-EP :

- Catalog: [SN74AHC1G126](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AHC1G126MDCKTEP	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AHC1G126MDCKTEP	SC70	DCK	5	250	340.0	340.0	38.0

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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