

## FEATURES

- Member of the Texas Instruments Widebus™ Family
- UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Modes
- Operates From 1.65 V to 3.6 V
- Max  $t_{pd}$  of 3.9 ns at 3.3 V
- $\pm 24$ -mA Output Drive at 3.3 V
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

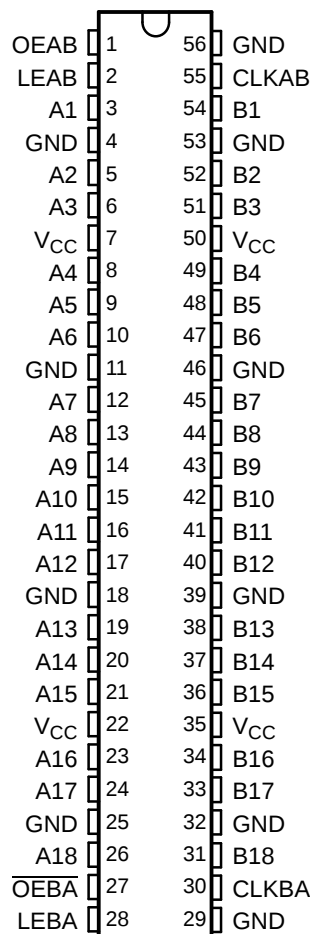
## DESCRIPTION/ORDERING INFORMATION

This 18-bit universal bus transceiver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

Data flow in each direction is controlled by output-enable (OEAB and  $\overline{OEBA}$ ), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B, but uses  $\overline{OEBA}$ , LEBA, and CLKBA. The output enables are complementary (OEAB is active high, and  $\overline{OEBA}$  is active low).

DGG OR DL PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

| $T_A$         | PACKAGE <sup>(1)</sup> |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------------------|---------------|-----------------------|------------------|
| -40°C to 85°C | SSOP - DL              | Tube          | SN74ALVCH16501DL      | ALVCH16501       |
|               |                        | Tape and reel | SN74ALVCH16501DLR     |                  |
|               | TSSOP - DGG            | Tape and reel | SN74ALVCH16501DGGR    | ALVCH16501       |
|               | VFBGA - GQL            | Tape and reel | SN74ALVCH16501KR      | VH501            |
|               | VFBGA - ZQL (Pb-free)  |               | 74ALVCH16501ZQLR      |                  |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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# SN74ALVCH16501

## 18-BIT UNIVERSAL BUS TRANSCEIVER

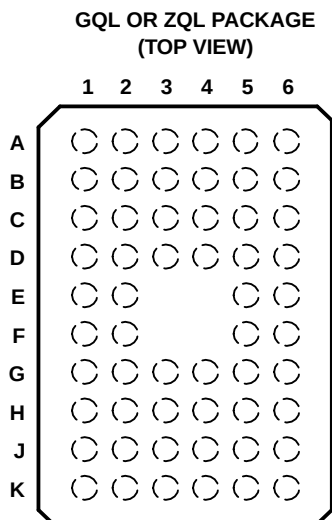
### WITH 3-STATE OUTPUTS

SCES024J–JULY 1995–REVISED OCTOBER 2004

#### DESCRIPTION/ORDERING INFORMATION (CONTINUED)

To ensure the high-impedance state during power up or power down,  $\overline{OEBA}$  should be tied to  $V_{CC}$  through a pullup resistor, and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.



#### TERMINAL ASSIGNMENTS

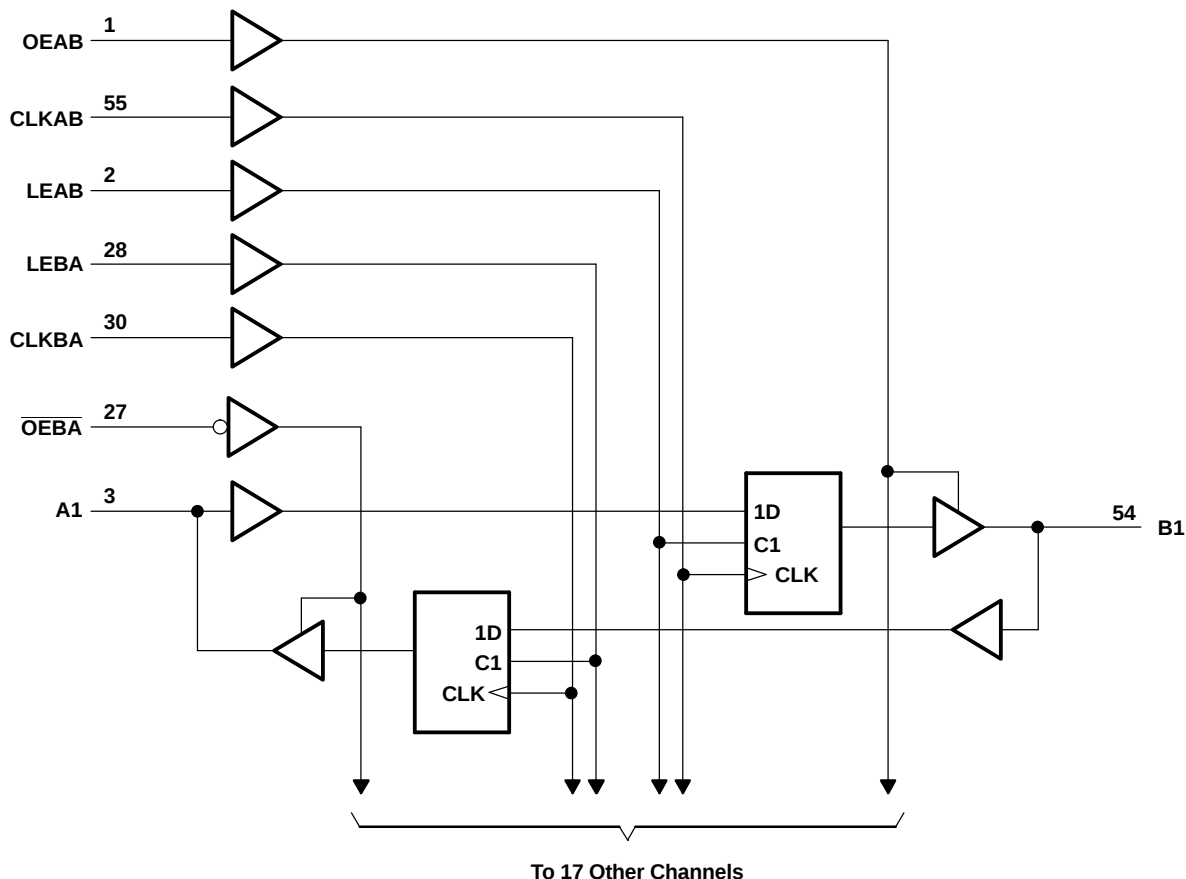
|          | 1   | 2                 | 3        | 4        | 5     | 6   |
|----------|-----|-------------------|----------|----------|-------|-----|
| <b>A</b> | A1  | LEAB              | OEAB     | GND      | CLKAB | B1  |
| <b>B</b> | A3  | A2                | GND      | GND      | B2    | B3  |
| <b>C</b> | A5  | A4                | $V_{CC}$ | $V_{CC}$ | B4    | B5  |
| <b>D</b> | A7  | A6                | GND      | GND      | B6    | B7  |
| <b>E</b> | A9  | A8                |          |          | B8    | B9  |
| <b>F</b> | A10 | A11               |          |          | B11   | B10 |
| <b>G</b> | A12 | A13               | GND      | GND      | B13   | B12 |
| <b>H</b> | A14 | A15               | $V_{CC}$ | $V_{CC}$ | B15   | B14 |
| <b>J</b> | A16 | A17               | GND      | GND      | B17   | B16 |
| <b>K</b> | A18 | $\overline{OEBA}$ | LEBA     | GND      | CLKBA | B18 |

**FUNCTION TABLE<sup>(1)</sup>**

| INPUTS |      |       |   | OUTPUT<br>B                   |
|--------|------|-------|---|-------------------------------|
| OEAB   | LEAB | CLKAB | A |                               |
| L      | X    | X     | X | Z                             |
| H      | H    | X     | L | L                             |
| H      | H    | X     | H | H                             |
| H      | L    | ↑     | L | L                             |
| H      | L    | ↑     | H | H                             |
| H      | L    | H     | X | B <sub>0</sub> <sup>(2)</sup> |
| H      | L    | L     | X | B <sub>0</sub> <sup>(3)</sup> |

- (1) A-to-B data flow is shown; B-to-A flow is similar, but uses  $\overline{\text{OEBA}}$ ,  $\text{LEBA}$ , and  $\text{CLKBA}$ .  
 (2) Output level before the indicated steady-state input conditions were established, provided that  $\text{CLKAB}$  was high before  $\text{LEAB}$  went low  
 (3) Output level before the indicated steady-state input conditions were established

**LOGIC DIAGRAM (POSITIVE LOGIC)**



Pin numbers shown are for the DGG and DL packages.

# SN74ALVCH16501

## 18-BIT UNIVERSAL BUS TRANSCEIVER

### WITH 3-STATE OUTPUTS

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#### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|                                                        |                                          |                                 | MIN  | MAX                   | UNIT |
|--------------------------------------------------------|------------------------------------------|---------------------------------|------|-----------------------|------|
| V <sub>CC</sub>                                        | Supply voltage range                     |                                 | -0.5 | 4.6                   | V    |
| V <sub>I</sub>                                         | Input voltage range                      | Except I/O ports <sup>(2)</sup> | -0.5 | 4.6                   | V    |
|                                                        |                                          | I/O ports <sup>(2)(3)</sup>     | -0.5 | V <sub>CC</sub> + 0.5 |      |
| V <sub>O</sub>                                         | Output voltage range <sup>(2)(3)</sup>   |                                 | -0.5 | V <sub>CC</sub> + 0.5 | V    |
| I <sub>IK</sub>                                        | Input clamp current                      | V <sub>I</sub> < 0              | -50  |                       | mA   |
| I <sub>OK</sub>                                        | Output clamp current                     | V <sub>O</sub> < 0              | -50  |                       | mA   |
| I <sub>O</sub>                                         | Continuous output current                |                                 | ±50  |                       | mA   |
| Continuous current through each V <sub>CC</sub> or GND |                                          |                                 | ±100 |                       | mA   |
| θ <sub>JA</sub>                                        | Package thermal impedance <sup>(4)</sup> | DGG package                     | 64   |                       | °C/W |
|                                                        |                                          | DL package                      | 56   |                       |      |
|                                                        |                                          | GQL/ZQL package                 | 42   |                       |      |
| T <sub>stg</sub>                                       | Storage temperature range                |                                 | -65  | 150                   | °C   |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

#### RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

|                     |                                    | MIN                                          | MAX                  | UNIT |
|---------------------|------------------------------------|----------------------------------------------|----------------------|------|
| $V_{CC}$            | Supply voltage                     | 1.65                                         | 3.6                  | V    |
| $V_{IH}$            | High-level input voltage           | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ | $0.65 \times V_{CC}$ | V    |
|                     |                                    | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$   | 1.7                  |      |
|                     |                                    | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$   | 2                    |      |
| $V_{IL}$            | Low-level input voltage            | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ | $0.35 \times V_{CC}$ | V    |
|                     |                                    | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$   | 0.7                  |      |
|                     |                                    | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$   | 0.8                  |      |
| $V_I$               | Input voltage                      | 0                                            | $V_{CC}$             | V    |
| $V_O$               | Output voltage                     | 0                                            | $V_{CC}$             | V    |
| $I_{OH}$            | High-level output current          | $V_{CC} = 1.65 \text{ V}$                    | -4                   | mA   |
|                     |                                    | $V_{CC} = 2.3 \text{ V}$                     | -12                  |      |
|                     |                                    | $V_{CC} = 2.7 \text{ V}$                     | -12                  |      |
|                     |                                    | $V_{CC} = 3 \text{ V}$                       | -24                  |      |
| $I_{OL}$            | Low-level output current           | $V_{CC} = 1.65 \text{ V}$                    | 4                    | mA   |
|                     |                                    | $V_{CC} = 2.3 \text{ V}$                     | 12                   |      |
|                     |                                    | $V_{CC} = 2.7 \text{ V}$                     | 12                   |      |
|                     |                                    | $V_{CC} = 3 \text{ V}$                       | 24                   |      |
| $\Delta t/\Delta v$ | Input transition rise or fall rate |                                              | 10                   | ns/V |
| $T_A$               | Operating free-air temperature     | -40                                          | 85                   | °C   |

- (1) All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                      | TEST CONDITIONS                                                              | V <sub>CC</sub> | MIN TYP <sup>(1)</sup> MAX | UNIT |
|--------------------------------|------------------------------------------------------------------------------|-----------------|----------------------------|------|
| V <sub>OH</sub>                | I <sub>OH</sub> = -100 µA                                                    | 1.65 V to 3.6 V | V <sub>CC</sub> - 0.2      | V    |
|                                | I <sub>OH</sub> = -4 mA                                                      | 1.65 V          | 1.2                        |      |
|                                | I <sub>OH</sub> = -6 mA                                                      | 2.3 V           | 2                          |      |
|                                | I <sub>OH</sub> = -12 mA                                                     | 2.3 V           | 1.7                        |      |
|                                |                                                                              | 2.7 V           | 2.2                        |      |
|                                |                                                                              | 3 V             | 2.4                        |      |
|                                | I <sub>OH</sub> = -24 mA                                                     | 3 V             | 2                          |      |
| V <sub>OL</sub>                | I <sub>OL</sub> = 100 µA                                                     | 1.65 V to 3.6 V | 0.2                        | V    |
|                                | I <sub>OL</sub> = 4 mA                                                       | 1.65 V          | 0.45                       |      |
|                                | I <sub>OL</sub> = 6 mA                                                       | 2.3 V           | 0.4                        |      |
|                                | I <sub>OL</sub> = 12 mA                                                      | 2.3 V           | 0.7                        |      |
|                                |                                                                              | 2.7 V           | 0.4                        |      |
|                                | I <sub>OL</sub> = 24 mA                                                      | 3 V             | 0.55                       |      |
| I <sub>I</sub>                 | V <sub>I</sub> = V <sub>CC</sub> or GND                                      | 3.6 V           | ±5                         | µA   |
| I <sub>I(hold)</sub>           | V <sub>I</sub> = 0.58 V                                                      | 1.65 V          | 25                         | µA   |
|                                | V <sub>I</sub> = 1.07 V                                                      | 1.65 V          | -25                        |      |
|                                | V <sub>I</sub> = 0.7 V                                                       | 2.3 V           | 45                         |      |
|                                | V <sub>I</sub> = 1.7 V                                                       | 2.3 V           | -45                        |      |
|                                | V <sub>I</sub> = 0.8 V                                                       | 3 V             | 75                         |      |
|                                | V <sub>I</sub> = 2 V                                                         | 3 V             | -75                        |      |
|                                | V <sub>I</sub> = 0 V to 3.6 V <sup>(2)</sup>                                 | 3.6 V           | ±500                       |      |
| I <sub>OZ</sub> <sup>(3)</sup> | V <sub>O</sub> = V <sub>CC</sub> or GND                                      | 3.6 V           | ±10                        | µA   |
| I <sub>CC</sub>                | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0                  | 3.6 V           | 40                         | µA   |
| ΔI <sub>CC</sub>               | One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND | 3 V to 3.6 V    | 750                        | µA   |
| C <sub>i</sub>                 | Control inputs V <sub>I</sub> = V <sub>CC</sub> or GND                       | 3.3 V           | 4                          | pF   |
| C <sub>io</sub>                | A or B ports V <sub>O</sub> = V <sub>CC</sub> or GND                         | 3.3 V           | 8                          | pF   |

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(3) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

## TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

|                    |                 |                  |                 | V <sub>CC</sub> = 2.5 V<br>± 0.2 V |     | V <sub>CC</sub> = 2.7 V |     | V <sub>CC</sub> = 3.3 V<br>± 0.3 V |     | UNIT |
|--------------------|-----------------|------------------|-----------------|------------------------------------|-----|-------------------------|-----|------------------------------------|-----|------|
|                    |                 |                  |                 | MIN                                | MAX | MIN                     | MAX | MIN                                | MAX |      |
| f <sub>clock</sub> | Clock frequency |                  |                 | 150                                |     | 150                     |     | 150                                |     | MHz  |
| t <sub>w</sub>     | Pulse duration  | LE high          |                 | 3.3                                |     | 3.3                     |     | 3.3                                |     | ns   |
|                    |                 | CLK high or low  |                 | 3.3                                |     | 3.3                     |     | 3.3                                |     |      |
| t <sub>su</sub>    | Setup time      | Data before CLK↑ |                 | 2.2                                |     | 2.1                     |     | 1.7                                |     | ns   |
|                    |                 | Data before LE↓  | CLK high        | 1.9                                |     | 1.6                     |     | 1.5                                |     |      |
|                    |                 |                  | CLK low         | 1.3                                |     | 1.1                     |     | 1                                  |     |      |
| t <sub>h</sub>     | Hold time       | Data after CLK↑  |                 | 0.6                                |     | 0.6                     |     | 0.7                                |     | ns   |
|                    |                 | Data after LE↓   | CLK high or low |                                    | 1.4 |                         | 1.7 |                                    | 1.4 |      |

# SN74ALVCH16501

## 18-BIT UNIVERSAL BUS TRANSCEIVER

### WITH 3-STATE OUTPUTS

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## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

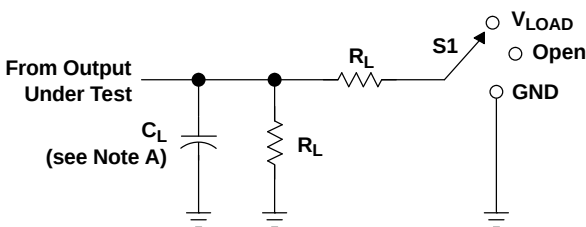
| PARAMETER  | FROM<br>(INPUT)   | TO<br>(OUTPUT) | $V_{CC} = 2.5\text{ V}$<br>$\pm 0.2\text{ V}$ |     | $V_{CC} = 2.7\text{ V}$ |     | $V_{CC} = 3.3\text{ V}$<br>$\pm 0.3\text{ V}$ |     | UNIT |
|------------|-------------------|----------------|-----------------------------------------------|-----|-------------------------|-----|-----------------------------------------------|-----|------|
|            |                   |                | MIN                                           | MAX | MIN                     | MAX | MIN                                           | MAX |      |
| $f_{\max}$ |                   |                | 150                                           |     | 150                     |     | 150                                           |     | MHz  |
| $t_{pd}$   | A or B            | B or A         | 1                                             | 4.8 |                         | 4.5 | 1                                             | 3.9 | ns   |
|            | LE                | A or B         | 1.1                                           | 5.7 |                         | 5.3 | 1.3                                           | 4.6 |      |
|            | CLK               |                | 1.2                                           | 6.1 |                         | 5.6 | 1.4                                           | 4.9 |      |
| $t_{en}$   | OEAB              | B              | 1                                             | 5.8 |                         | 5.3 | 1                                             | 4.6 | ns   |
| $t_{dis}$  | OEAB              | B              | 1.5                                           | 6.2 |                         | 5.7 | 1.4                                           | 5   | ns   |
| $t_{en}$   | $\overline{OEBA}$ | A              | 1.3                                           | 6.3 |                         | 6   | 1.1                                           | 5   | ns   |
| $t_{dis}$  | $\overline{OEBA}$ | A              | 1.3                                           | 5.3 |                         | 4.6 | 1.3                                           | 4.2 | ns   |

## OPERATING CHARACTERISTICS

$T_A = 25^\circ\text{C}$

| PARAMETER |                               |                  | TEST CONDITIONS                            | $V_{CC} = 2.5\text{ V}$ | $V_{CC} = 3.3\text{ V}$ | UNIT |
|-----------|-------------------------------|------------------|--------------------------------------------|-------------------------|-------------------------|------|
|           |                               |                  |                                            | TYP                     | TYP                     |      |
| $C_{pd}$  | Power dissipation capacitance | Outputs enabled  | $C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$ | 44                      | 54                      | pF   |
|           |                               | Outputs disabled |                                            | 6                       | 6                       |      |

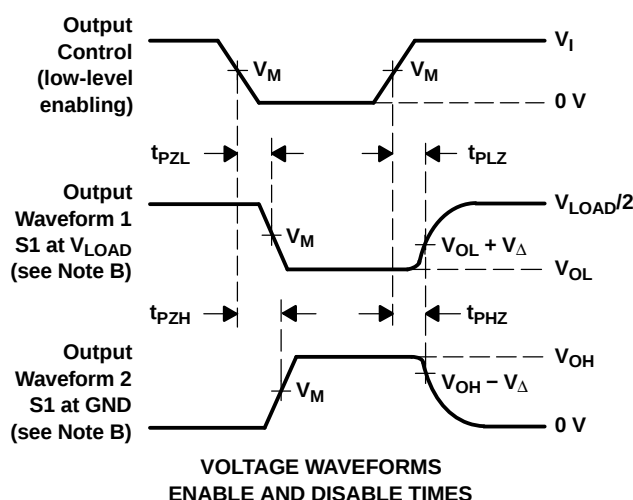
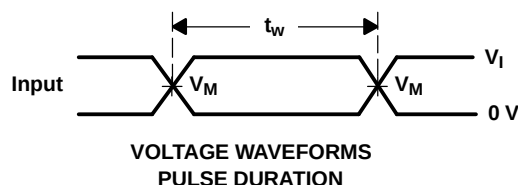
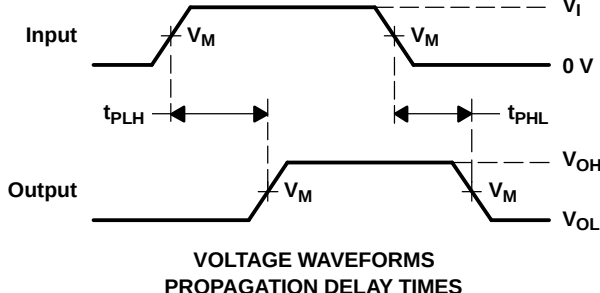
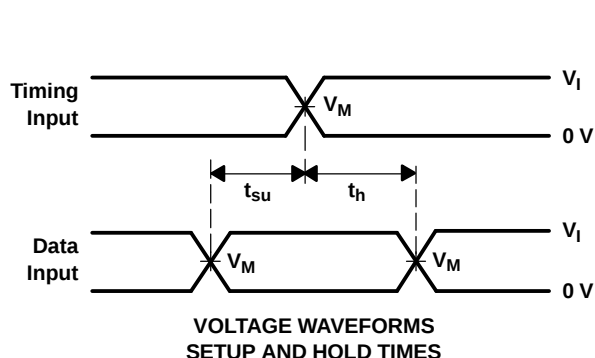
## PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

| TEST              | S1         |
|-------------------|------------|
| $t_{pd}$          | Open       |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND        |

| $V_{CC}$          | INPUT    |               | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$        | $V_{\Delta}$ |
|-------------------|----------|---------------|------------|-------------------|-------|--------------|--------------|
|                   | $V_I$    | $t_r/t_f$     |            |                   |       |              |              |
| 1.8 V             | $V_{CC}$ | $\leq 2$ ns   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k $\Omega$ | 0.15 V       |
| 2.5 V $\pm$ 0.2 V | $V_{CC}$ | $\leq 2$ ns   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 $\Omega$ | 0.15 V       |
| 2.7 V             | 2.7 V    | $\leq 2.5$ ns | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |
| 3.3 V $\pm$ 0.3 V | 2.7 V    | $\leq 2.5$ ns | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50$   $\Omega$ .  
D. The outputs are measured one at a time, with one transition per measurement.  
E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

| Orderable Device   | Status<br>(1) | Package Type               | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|--------------------|---------------|----------------------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| 74ALVCH16501DGGRG4 | ACTIVE        | TSSOP                      | DGG                | 56   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | ALVCH16501              | <a href="#">Samples</a> |
| 74ALVCH16501DLRG4  | ACTIVE        | SSOP                       | DL                 | 56   |                | TBD                        | Call TI                 | Call TI              | -40 to 85    |                         | <a href="#">Samples</a> |
| 74ALVCH16501ZQLR   | ACTIVE        | BGA<br>MICROSTAR<br>JUNIOR | ZQL                | 56   | 1000           | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 85    | VH501                   | <a href="#">Samples</a> |
| SN74ALVCH16501DGGR | ACTIVE        | TSSOP                      | DGG                | 56   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | ALVCH16501              | <a href="#">Samples</a> |
| SN74ALVCH16501DL   | ACTIVE        | SSOP                       | DL                 | 56   | 20             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | ALVCH16501              | <a href="#">Samples</a> |
| SN74ALVCH16501DLR  | OBSOLETE      | SSOP                       | DL                 | 56   |                | TBD                        | Call TI                 | Call TI              | -40 to 85    |                         |                         |
| SN74ALVCH16501KR   | OBSOLETE      | BGA<br>MICROSTAR<br>JUNIOR | GQL                | 56   |                | TBD                        | Call TI                 | Call TI              | -40 to 85    |                         |                         |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device             | Package Type         | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|----------------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| 74ALVCH16501ZQLR   | BGA MICROSTAR JUNIOR | ZQL             | 56   | 1000 | 330.0              | 16.4               | 4.8     | 7.3     | 1.5     | 8.0     | 16.0   | Q1            |
| SN74ALVCH16501DGGR | TSSOP                | DGG             | 56   | 2000 | 330.0              | 24.4               | 8.6     | 15.6    | 1.8     | 12.0    | 24.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS

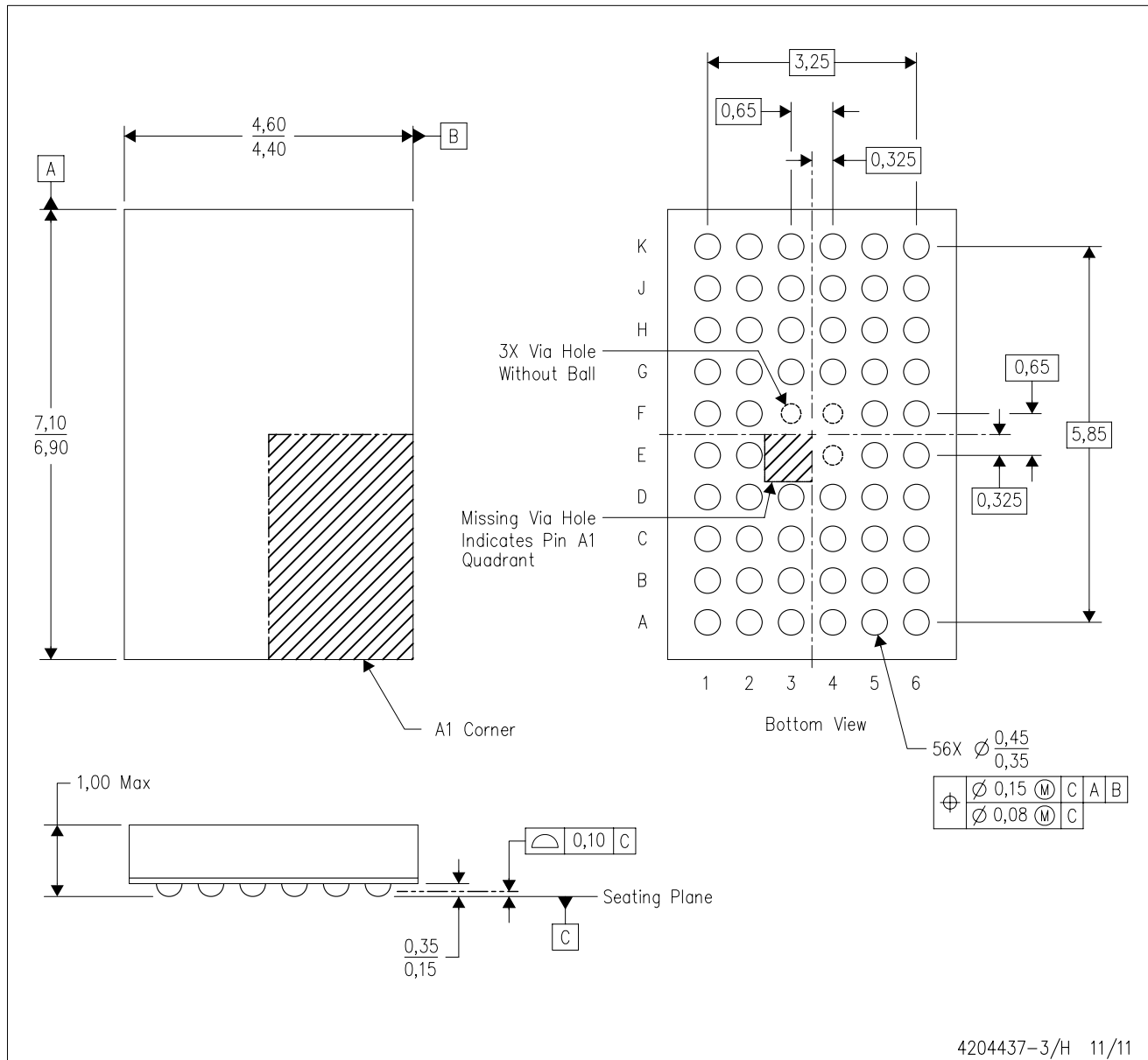


\*All dimensions are nominal

| Device             | Package Type         | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|----------------------|-----------------|------|------|-------------|------------|-------------|
| 74ALVCH16501ZQLR   | BGA MICROSTAR JUNIOR | ZQL             | 56   | 1000 | 333.2       | 345.9      | 28.6        |
| SN74ALVCH16501DGGR | TSSOP                | DGG             | 56   | 2000 | 367.0       | 367.0      | 45.0        |

ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY

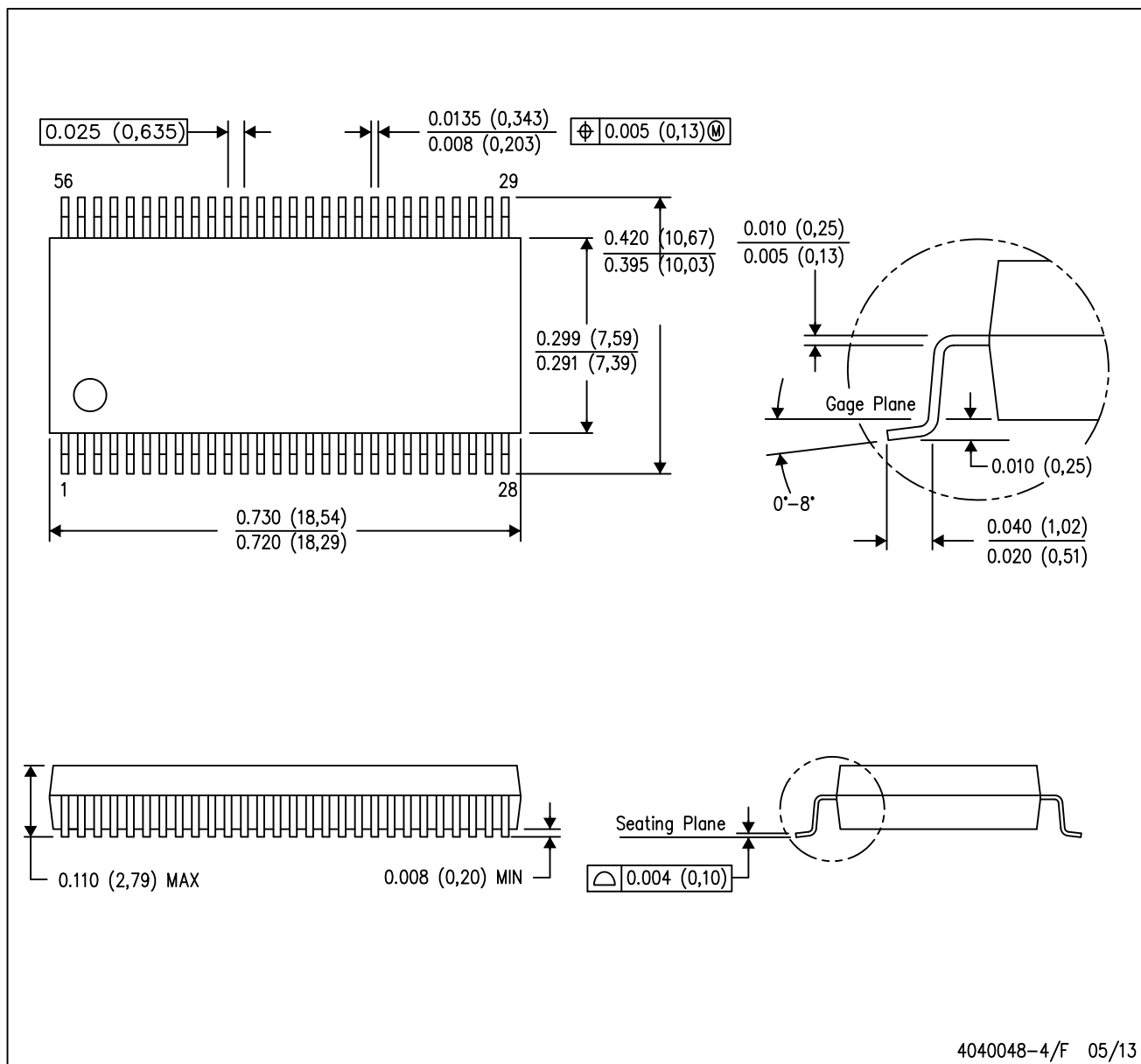


4204437-3/H 11/11

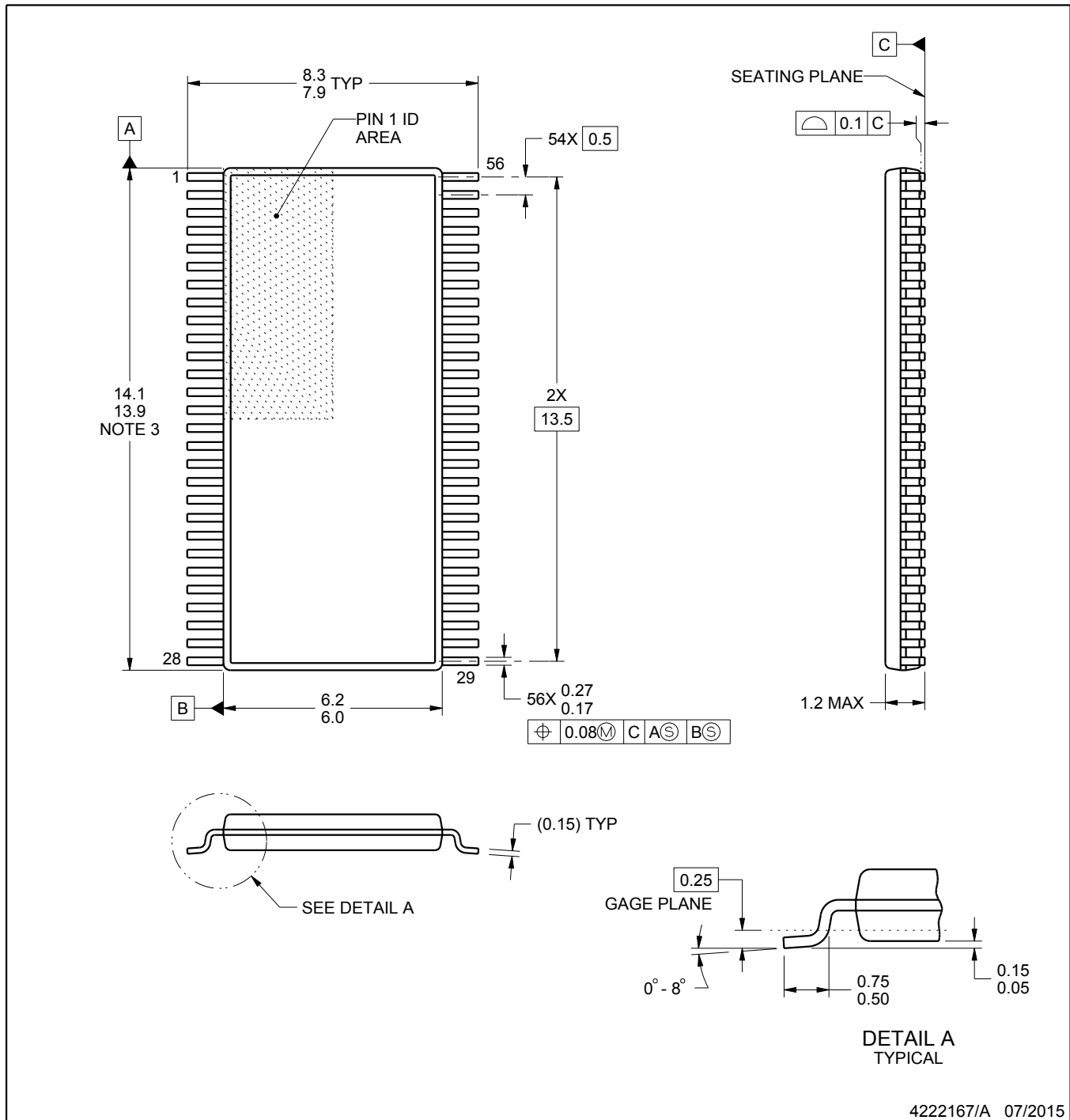
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-285 variation BA-2.
  - D. This package is Pb-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed  $0.006$  (0,15).
  - D. Falls within JEDEC MO-118



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## NOTES:

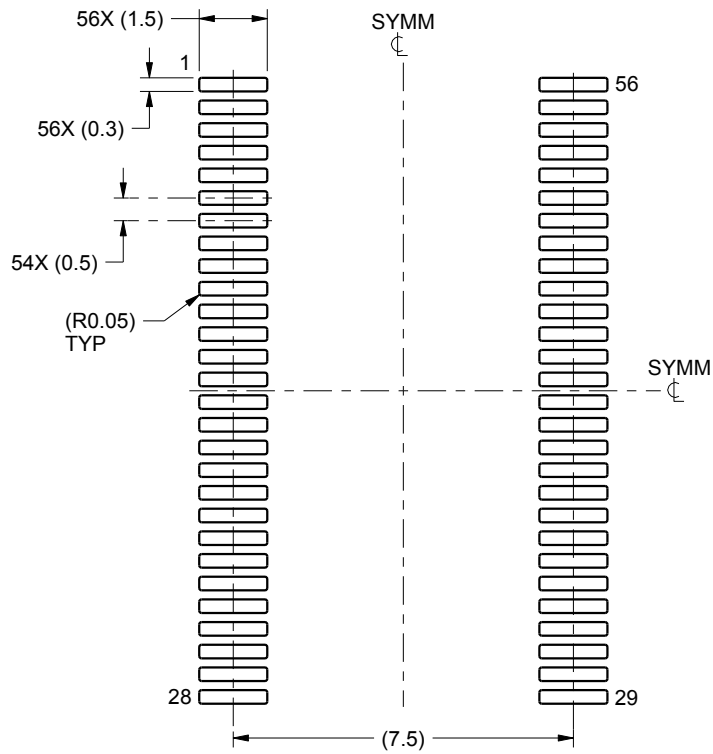
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

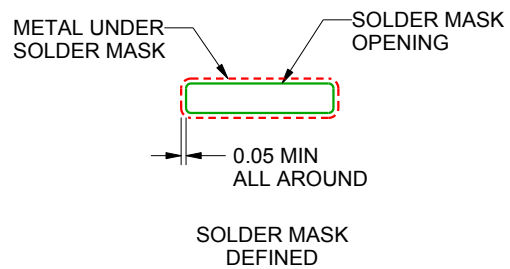
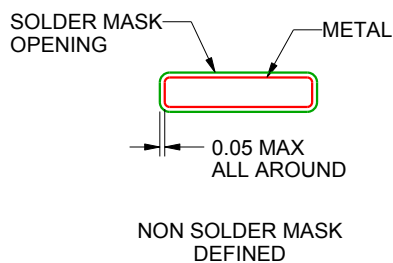
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

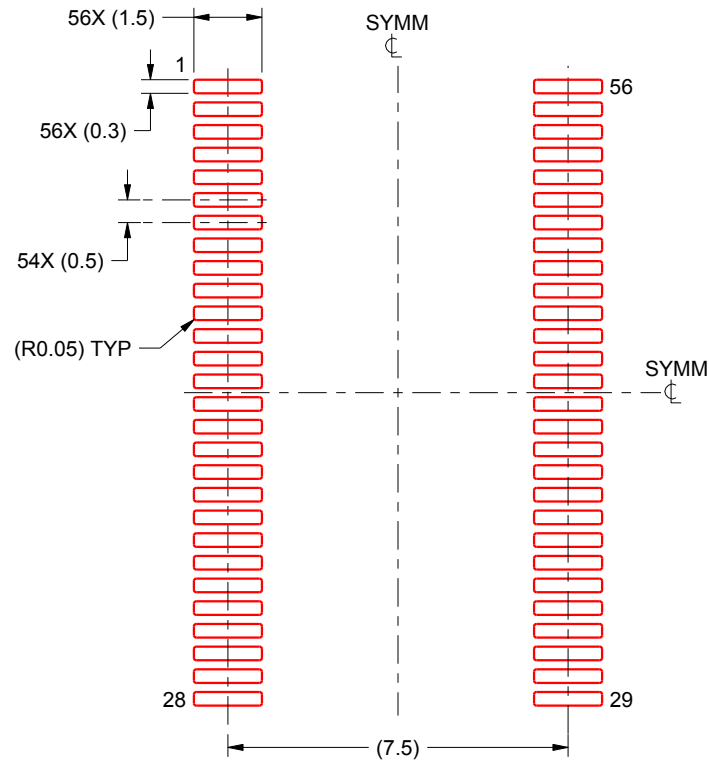
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

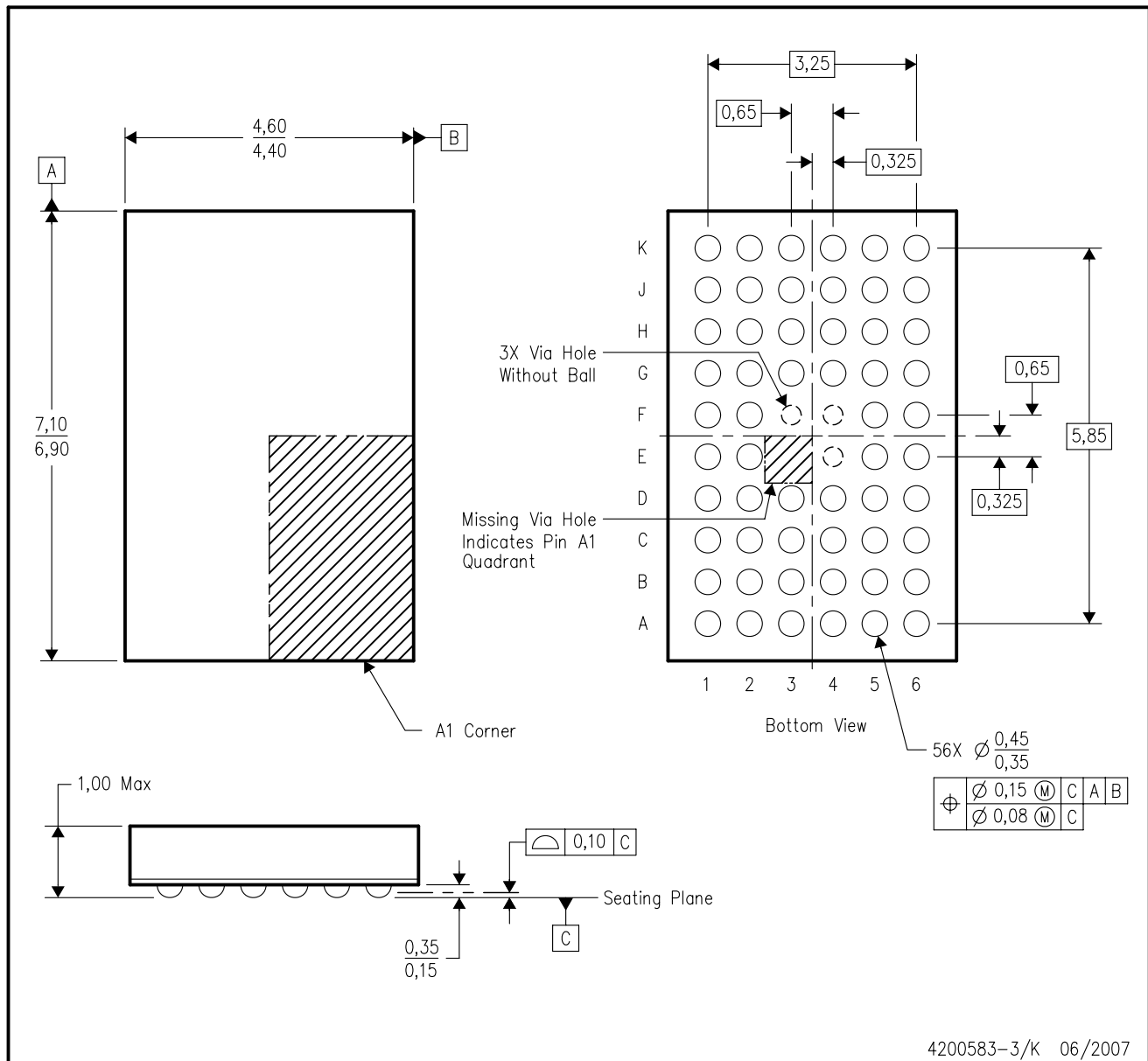
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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## GQL (R-PBGA-N56)

## PLASTIC BALL GRID ARRAY



4200583-3/K 06/2007

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-285 variation BA-2.
  - D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

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