PARALLEL-LOAD 8-BIT SHIFT REGISTERS

Check for Samples: SN54LV165A, SN74LV165A

FEATURES

- **2-V to 5.5-V V_{CC} Operation**
- **Max t_{pd} of 10.5 ns at 5 V**
- **Support Mixed-Mode Voltage Operation on All Ports**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DESCRIPTION

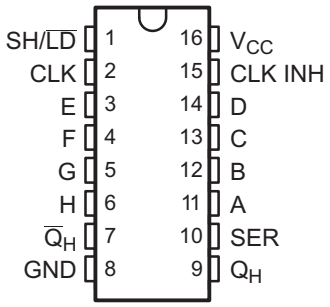
The ’LV165A devices are parallel-load, 8-bit shift registers designed for 2-V to 5.5-V V_{CC} operation.

When the devices are clocked, data is shifted toward the serial output Q_H. Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the shift/load ($\overline{SH}/LD$) input. The ’LV165A devices feature a clock-inhibit function and a complemented serial output, $\overline{Q}_H$.

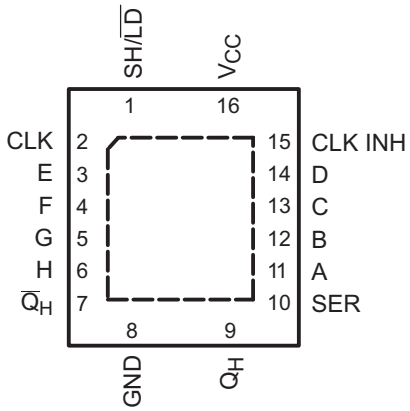
Clocking is accomplished by a low-to-high transition of the clock (CLK) input while $\overline{SH}/LD$ is held high and clock inhibit (CLK INH) is held low. The functions of CLK and CLK INH are interchangeable. Since a low CLK and a low-to-high transition of CLK INH accomplishes clocking, CLK INH should be changed to the high level only while CLK is high. Parallel loading is inhibited when $\overline{SH}/LD$ is held high. The parallel inputs to the register are enabled while $\overline{SH}/LD$ is held low, independently of the levels of CLK, CLK INH, or SER.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

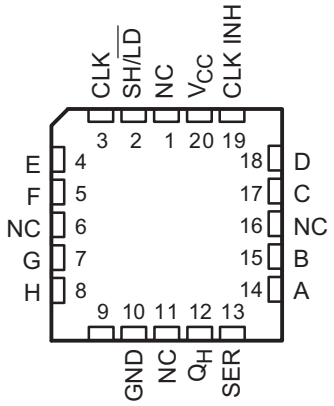
SN54LV165A . . . JO R W PACKAGE
SN74LV165A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN74LV165A . . . RGY PACKAGE
(TOP VIEW)



SN54LV165A . . . FK PACKAGE
(TOP VIEW)

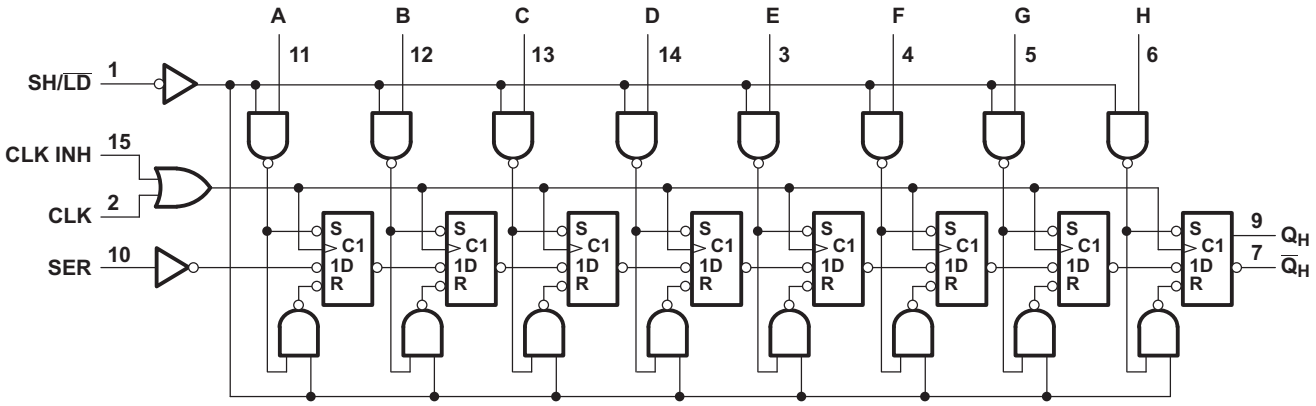


NC − No internal connection

FUNCTION TABLE

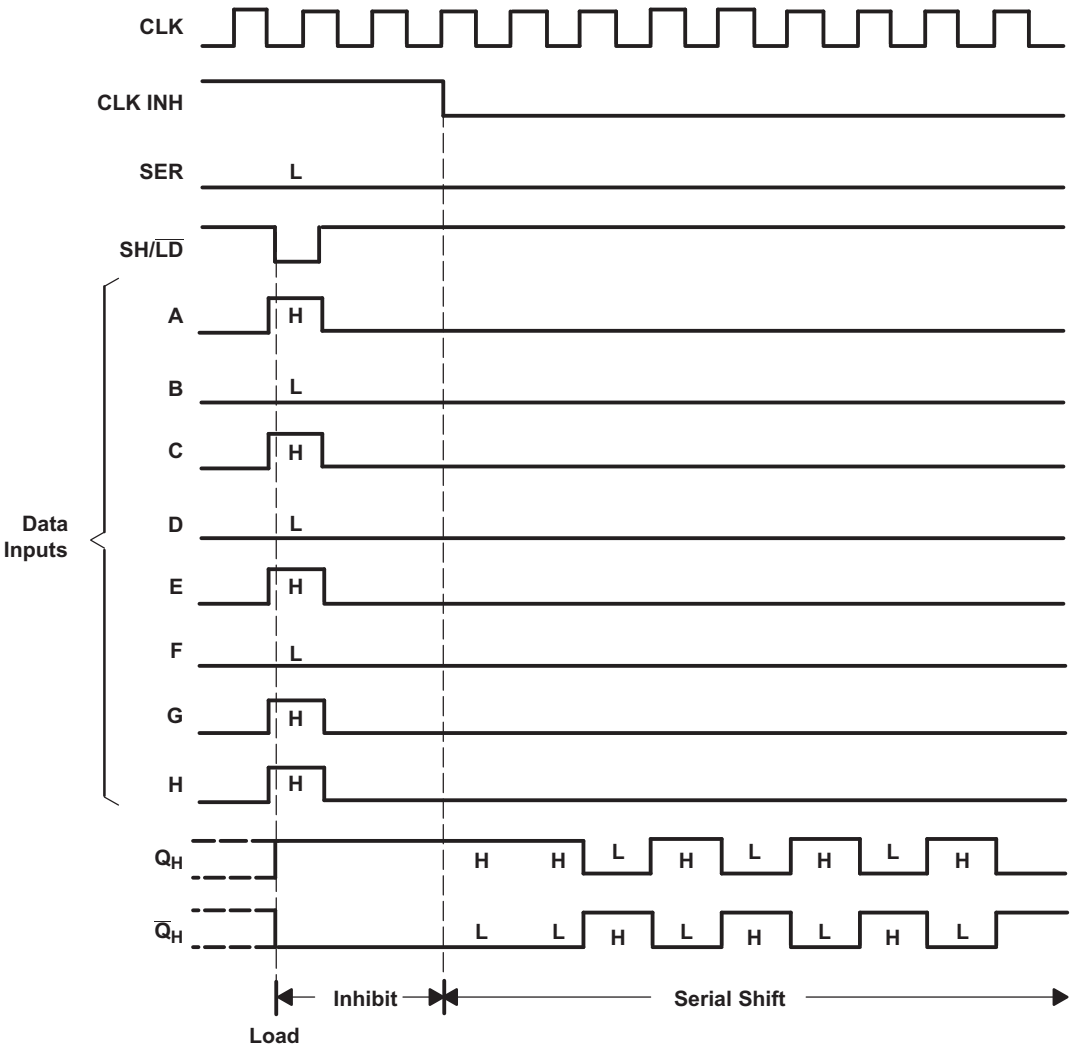
INPUTS			OPERATION
SH/LD	CLK	CLK INH	
L	X	X	Parallel load
H	H	X	Q_0
H	X	H	Q_0
H	L	↑	Shift
H	↑	L	Shift

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the D, DB, DGV, J, NS, PW, RGY, and W packages.

TYPICAL SHIFT, LOAD, AND INHIBIT SEQUENCES



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
Supply voltage range, V_{CC}		–0.5 to 7	V
Input voltage range, V_I(2)		–0.5 to 7	V
Voltage range applied to any output in the high-impedance or power-off state, V_O(2)		–0.5 to 7	V
Output voltage range, V_O(2)(3)		–0.5 to V_{CC} + 0.5	V
Input clamp current, I_{IK} (V_I < 0)		–20	mA
Output clamp current, I_{OK} (V_O < 0)		–50	mA
Continuous output current, I_O (V_O = 0 to V_{CC})		±25	mA
Continuous current through V_{CC} or GND		±50	mA
Package thermal impedance, θ_{JA}	D package(4)	73	°C/W
	DB package(4)	82	
	DGV package(4)	120	
	NS package(4)	67	
	PW package(4)	108	
	RGY package(5)	39	
Storage temperature range, T_{stg}		–65 to 150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.
(5) The package thermal impedance is calculated in accordance with JESD 51-5.

RECOMMENDED OPERATING CONDITIONS(1)

			SN54LV165A		SN74LV165A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2		V
V_{IH}	High level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		V_{CC} × 0.7		
V_{IL}	Low level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High level output current	V_{CC} = 2 V		–50		–50	µA
		V_{CC} = 2.3 V to 2.7 V		–2		–2	mA
		V_{CC} = 3 V to 3.6 V		–6		–6	
		V_{CC} = 4.5 V to 5.5 V		–12		–12	
I_{OL}	Low level output current	V_{CC} = 2 V		50		50	µA
		V_{CC} = 2.3 V to 2.7 V		2		2	mA
		V_{CC} = 3 V to 3.6 V		6		6	
		V_{CC} = 4.5 V to 5.5 V		12		12	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200		200	ns/V
		V_{CC} = 3 V to 3.6 V		100		100	
		V_{CC} = 4.5 V to 5.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	-55°C TO 125°C			-40°C TO 85°C			-40°C TO 125°C Recommended			UNIT
				SN54LV165A/ SN74LV165A-EP			SN74LV165A			SN74LV165A			
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = –50 µA		2 V to 5.5 V	V_{CC} – 0.1			V_{CC} – 0.1			V_{CC} – 0.1			V
	I_{OH} = –2 mA		2.3 V	2			2			2			
	I_{OH} = –6 mA		3 V	2.48			2.48			2.48			
	I_{OH} = –12 mA		4.5 V	3.8			3.8			3.8			
V_{OL}	I_{OL} = 50 µA		2 V to 5.5 V			0.1			0.1			0.1	V
	I_{OL} = 2 mA		2.3 V			0.4			0.4			0.4	
	I_{OL} = 6 mA		3 V			0.44			0.44			0.44	
	I_{OL} = 12 mA		4.5 V			0.55			0.55			0.55	
I_I	V_I = 5.5 V or GND		0 to 5.5 V			±1			±1			±1	µA
I_{CC}	V_I = V_{CC} or GND,	IO = 0	5.5 V			20			20			20	µA
I_{off}	V_I or V_O = 0 to 5.5 V		0			5			5			5	µA
C_i	V_I = V_{CC} or GND		3.3 V		1.7			1.7			1.7		pF

TIMING REQUIREMENTS

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER		TEST CONDITION	T_A = 25°C		-55°C TO 125°C		-40°C TO 85°C		-40°C TO 125°C		UNIT
					SN54LV165A/ SN74LV165A-EP		SN74LV165A		SN74LV165A		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	8.5		9		9		9		ns
		SH/$\overline{LD}$ low	11		13		13		13		
t_{su}	Setup time	SH/$\overline{LD}$ high before CLK↑	7		8.5		8.5		8.5		ns
		SER before CLK↑	8.5		9.5		9.5		9.5		
		CLK INH before CLK↑	7		7		7		7		
		Data before SH/$\overline{LD}$↑	11.5		12		12		12		
t_h	Hold time	SER data after CLK↑	−1		0		0		0		ns
		Parallel data after SH/$\overline{LD}$↑	0		0.5		0.5		0.5		
		SH/$\overline{LD}$ high after CLK↑	0		0		0		0		

TIMING REQUIREMENTS

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER		TEST CONDITION	T_A = 25°C		-55°C TO 125°C		-40°C TO 85°C		-40°C TO 125°C		UNIT
					SN54LV165A/ SN74LV165A-EP		SN74LV165A		SN74LV165A		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	6		7		7		7		ns
		SH/$\overline{LD}$ low	7.5		9		9		9		
t_{su}	Setup time	SH/$\overline{LD}$ high before CLK↑	5		6		6		6		ns
		SER before CLK↑	5		6		6		6		
		CLK INH before CLK↑	5		5		5		5		
		Data before SH/$\overline{LD}$↑	7.5		8.5		8.5		8.5		
t_h	Hold time	SER data after CLK↑	0		0		0		0		ns
		Parallel data after SH/$\overline{LD}$↑	0.5		0.5		0.5		0.5		
		SH/$\overline{LD}$ high after CLK↑	0		0		0		0		

TIMING REQUIREMENTS

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER		TEST CONDITION	T_A = 25°C		-55°C TO 125°C		-40°C TO 85°C		-40°C TO 125°C		UNIT
					SN54LV165A		SN74LV165A		SN74LV165A		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	4		4		4		4		ns
		SH/$\overline{LD}$ low	5		5		6		6		
t_{su}	Setup time	SH/$\overline{LD}$ high before CLK↑	4		4		4		4		ns
		SER before CLK↑	4		4		4		4		
		CLK INH before CLK↑	3.5		3.5		3.5		3.5		
		Data before SH/$\overline{LD}$↑	5		5		5		5		
t_h	Hold time	SER data after CLK↑	0.5		0.5		0.5		0.5		ns
		Parallel data after SH/$\overline{LD}$↑	1		1		1		1		
		SH/$\overline{LD}$ high after CLK↑	0.5		0.5		0.5		0.5		

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAP	T_A = 25°C			-55°C TO 125°C		-40°C TO 85°C		-40°C TO 125°C		UNIT
							SN54LV165A/ SN74LV165A-EP		SN74LV165A		SN74LV165A Recommended		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	50(1)	80(1)		45(1)		45		45		MHz
			C_L = 50 pF	40	65		35		35		35		
t_{pd}	CLK	Q_H or $\overline{Q}_H$	C_L = 15 pF		12.2(1)	19.8(1)	1(1)	22(1)	1	22	1	22	ns
	SH/$\overline{LD}$				13.1(1)	21.5(1)	1(1)	23.5(1)	1	23.5	1	23.5	
	H				12.9(1)	21.7(1)	1(1)	24(1)	1	24	1	24	
t_{pd}	CLK	Q_H or $\overline{Q}_H$	C_L = 50 pF		15.3	23.3	1	26	1	26	1	26	ns
	SH/$\overline{LD}$				16.1	25.1	1	28	1	28	1	28	
	H				15.9	25.3	1	28	1	28	1	28	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAP	T_A = 25°C			-55°C TO 125°C		-40°C TO 85°C		-40°C TO 125°C		UNIT
							SN54LV165A/ SN74LV165A-EP		SN74LV165A		SN74LV165A Recommended		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	65(1)	115(1)		55(1)		55		55		MHz
			C_L = 50 pF	60	90		50		50		50		
t_{pd}	CLK	Q_H or $\overline{Q}_H$	C_L = 15 pF		8.6(1)	15.4(1)	1(1)	18(1)	1	18	1	18	ns
	SH/$\overline{LD}$				9.1(1)	15.8(1)	1(1)	18.5(1)	1	18.5	1	18.5	
	H				8.9(1)	14.1(1)	1(1)	16.5(1)	1	16.5	1	16.5	
t_{pd}	CLK	Q_H or $\overline{Q}_H$	C_L = 50 pF		10.9	14.9	1	16.9	1	16.9	1	16.9	ns
	SH/$\overline{LD}$				11.3	19.3	1	22	1	22	1	22	
	H				11.1	17.6	1	20	1	20	1	20	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAP	T_A = 25°C			-55°C TO 125°C		-40°C TO 85°C		-40°C TO 125°C		UNIT
							SN54LV165A		SN74LV165A		SN74LV165A Recommended		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	110(1)	165(1)		90(1)		90		90		MHz
			C_L = 50 pF	95	125		85		85		85		
t_{pd}	CLK	Q_H or $\overline{Q}_H$	C_L = 15 pF		6(1)	9.9(1)	1(1)	11.5(1)	1	11.5	1	11.5	ns
	SH/$\overline{LD}$				6(1)	9.9(1)	1(1)	11.5(1)	1	11.5	1	11.5	
	H				6(1)	9(1)	1(1)	10.5(1)	1	10.5	1	10.5	
t_{pd}	CLK	Q_H or $\overline{Q}_H$	C_L = 50 pF		7.7	11.9	1	13.5	1	13.5	1	13.5	ns
	SH/$\overline{LD}$				7.7	11.9	1	13.5	1	13.5	1	13.5	
	H				7.6	11	1	12.5	1	12.5	1	12.5	

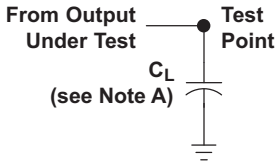
(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

OPERATING CHARACTERISTICS

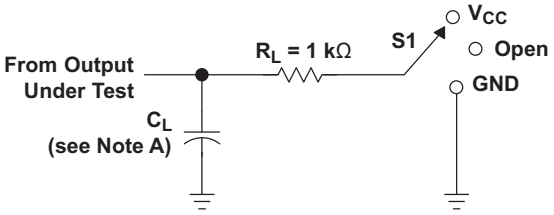
T_A = 25°C

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF	f = 10 MHz	3.3 V	36.1	pF
				5 V	37.5	

PARAMETER MEASUREMENT INFORMATION

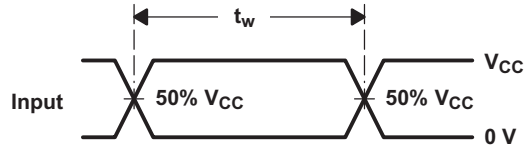


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

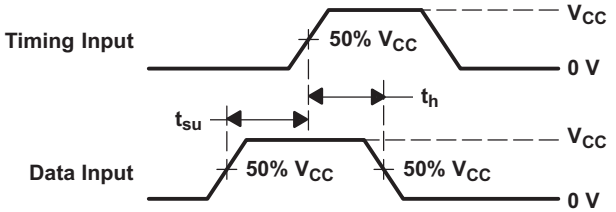


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

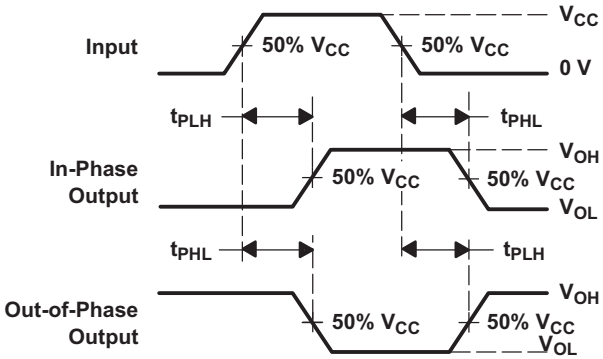
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



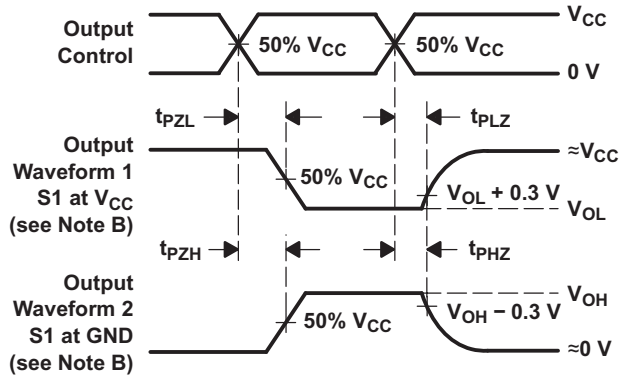
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.

D. The outputs are measured one at a time, with one input transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{en}.

G. t_{PHL} and t_{PLH} are the same as t_{pd}.

H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

REVISION HISTORY

Changes from Revision M (December 2010) to Revision N	Page
• Extended maximum temperature operating range from 85°C to 125°C.	5

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV165AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165ADBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165ADGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165ADRG3	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV165A	Samples
SN74LV165APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165APWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165APWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165APWRG3	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165APWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV165ARGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV165A	Samples
SN74LV165ARGYRG4	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV165A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74LV165A :

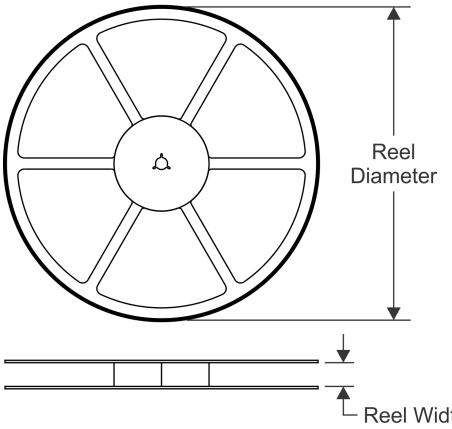
- Enhanced Product: SN74LV165A-EP

NOTE: Qualified Version Definitions:

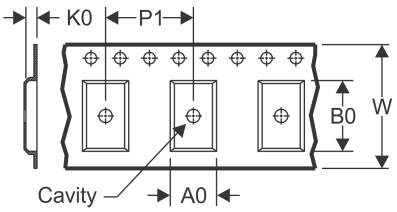
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

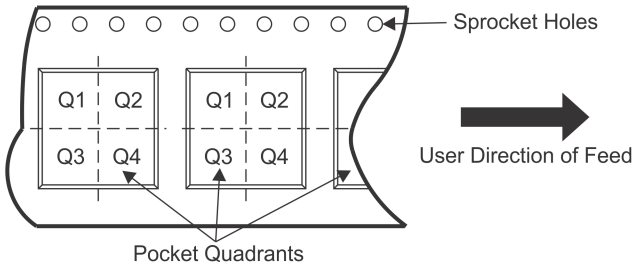


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

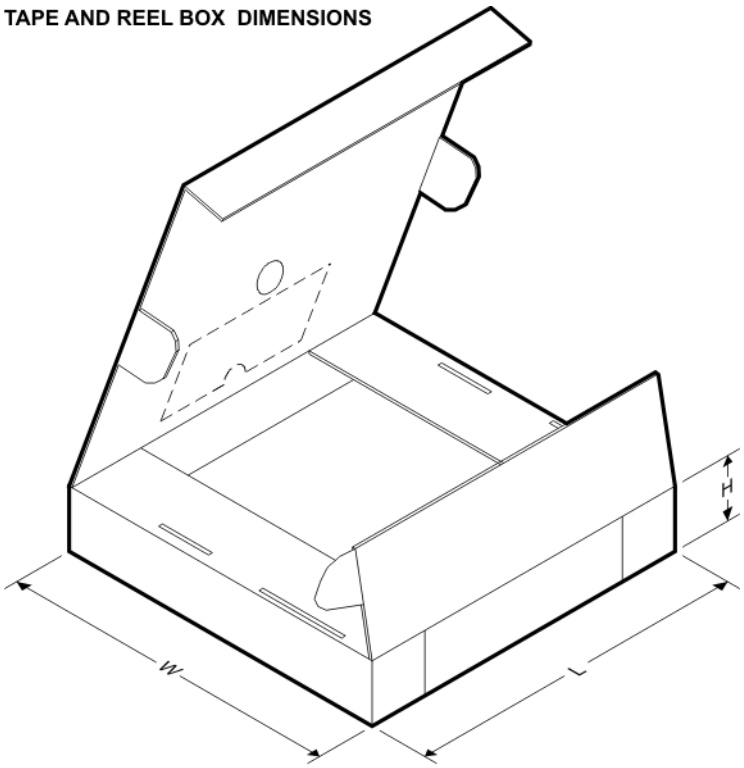
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV165ADBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LV165ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV165ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV165ADR	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV165ADRG3	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV165ADRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV165ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV165APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV165APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV165APWRG3	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV165APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV165APWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV165ARGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

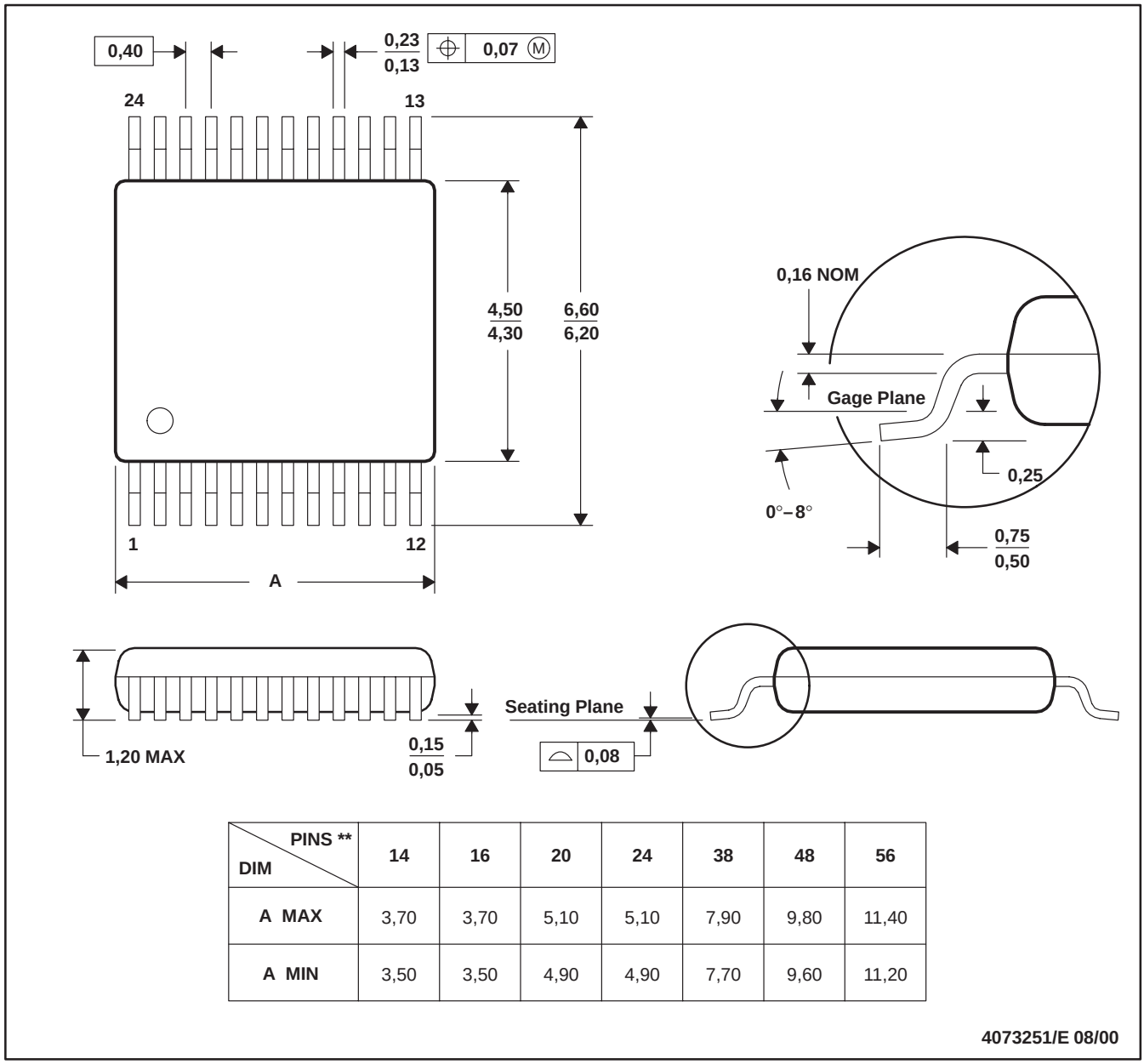


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV165ADBR	SSOP	DB	16	2000	367.0	367.0	38.0
SN74LV165ADGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
SN74LV165ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LV165ADR	SOIC	D	16	2500	364.0	364.0	27.0
SN74LV165ADRG3	SOIC	D	16	2500	364.0	364.0	27.0
SN74LV165ADRG4	SOIC	D	16	2500	333.2	345.9	28.6
SN74LV165ANSR	SO	NS	16	2000	367.0	367.0	38.0
SN74LV165APWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV165APWR	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74LV165APWRG3	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74LV165APWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV165APWT	TSSOP	PW	16	250	367.0	367.0	35.0
SN74LV165ARGYR	VQFN	RGY	16	3000	367.0	367.0	35.0

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

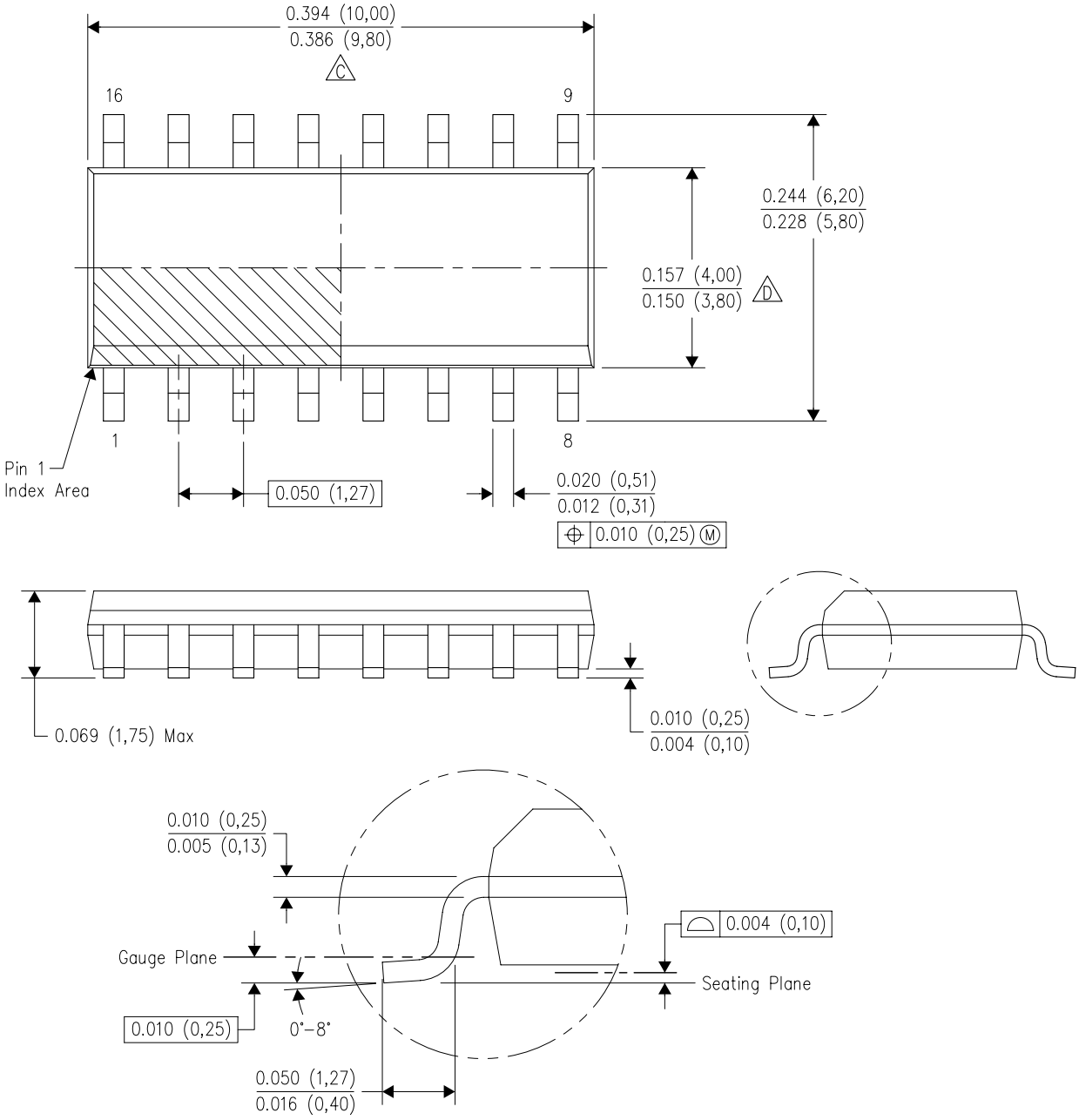


DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

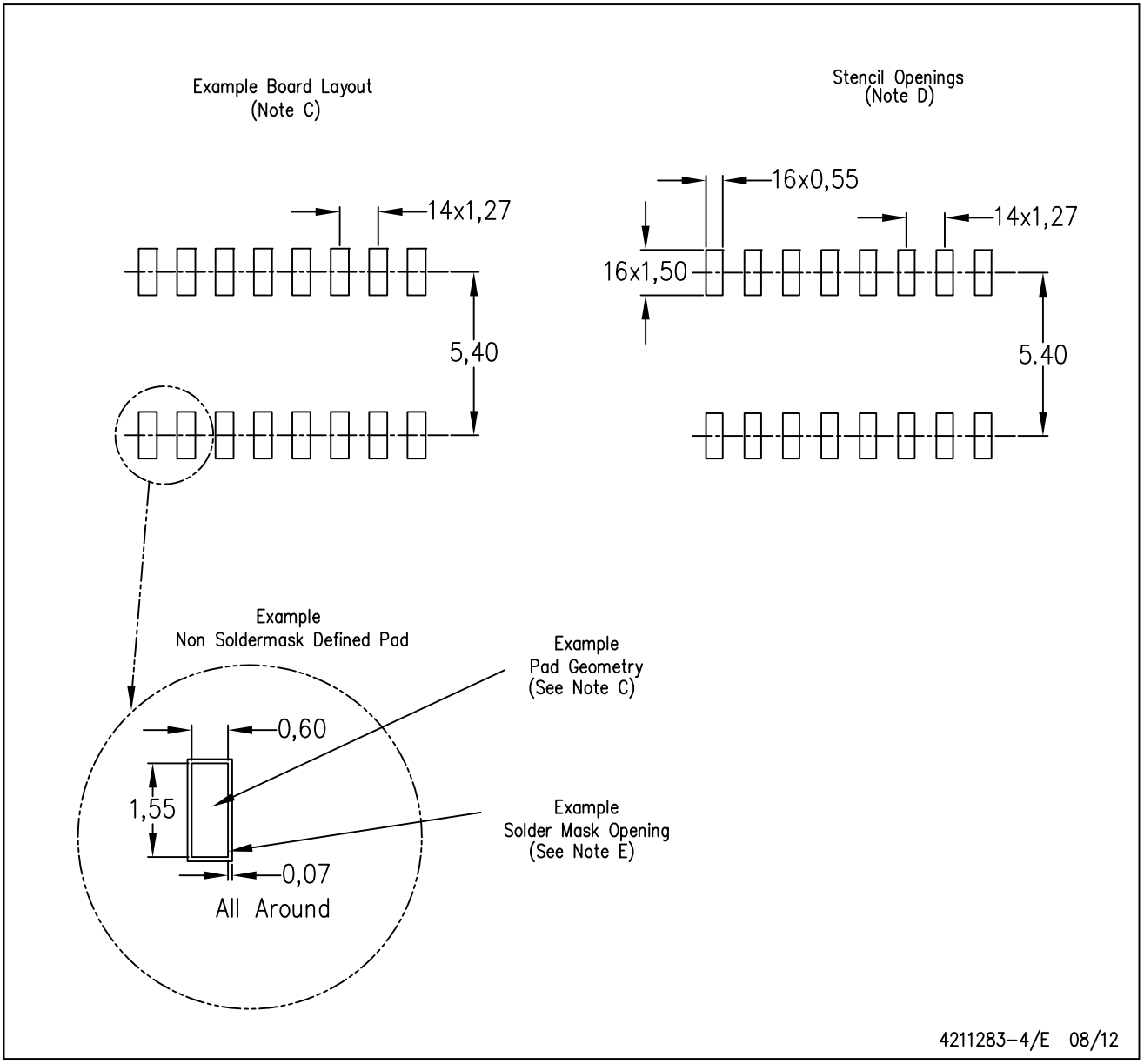
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



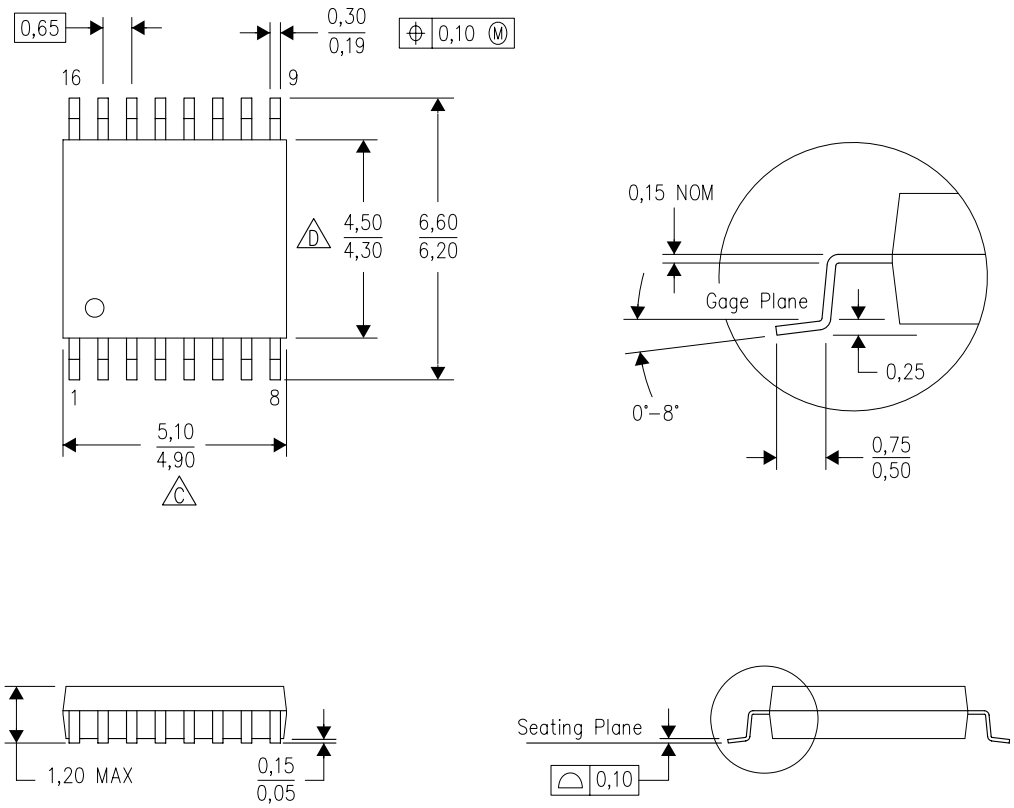
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

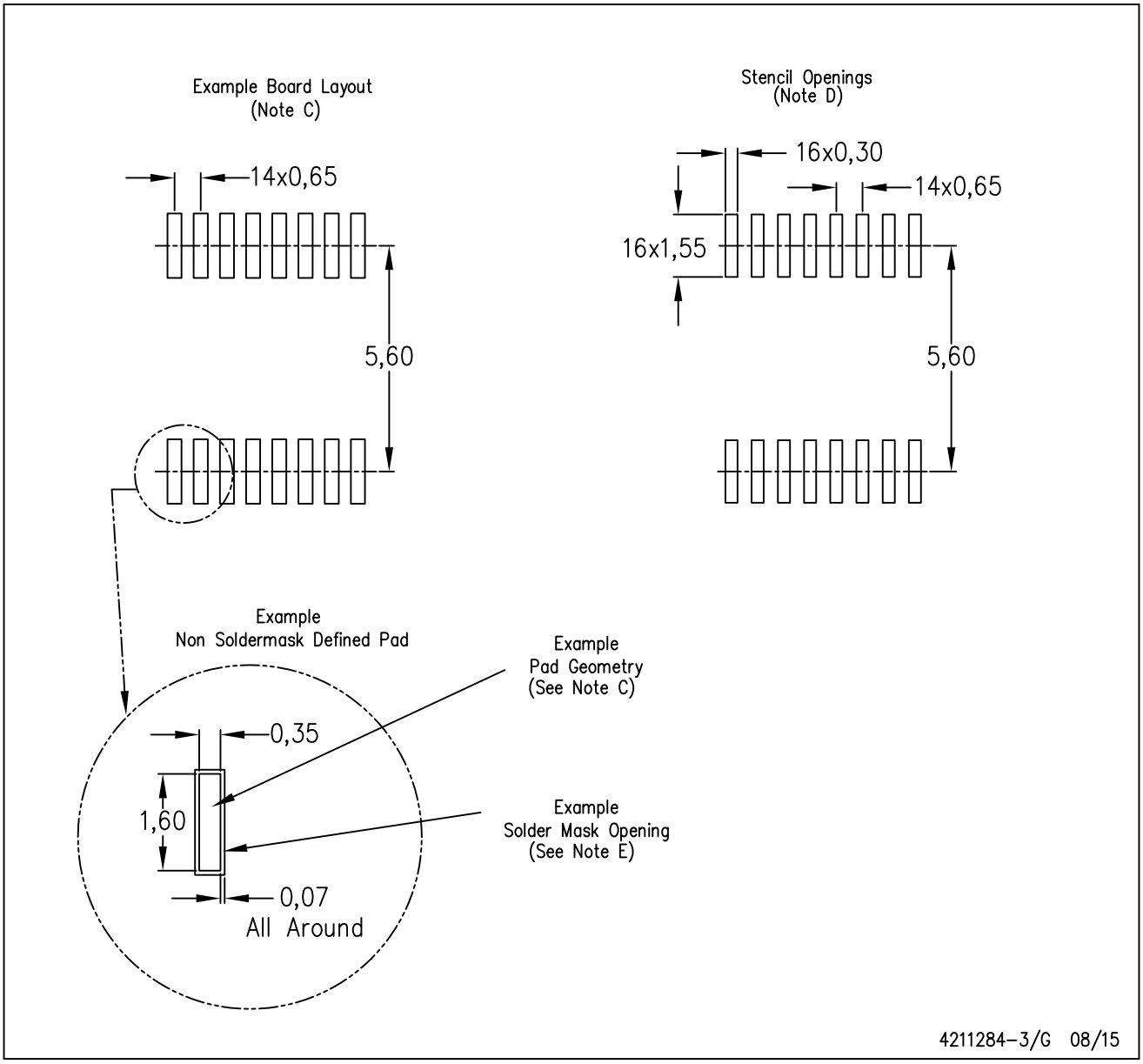
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE

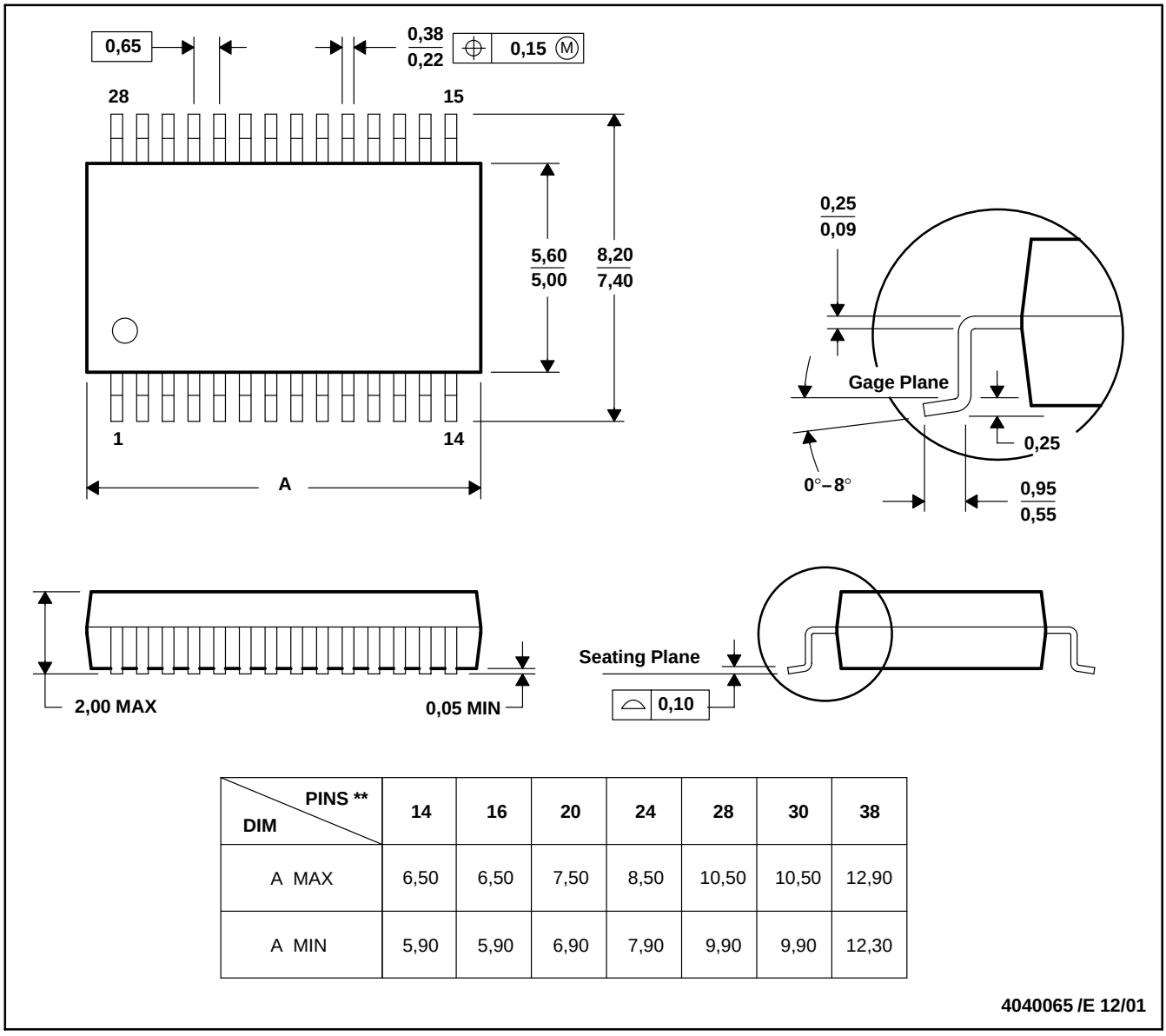


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

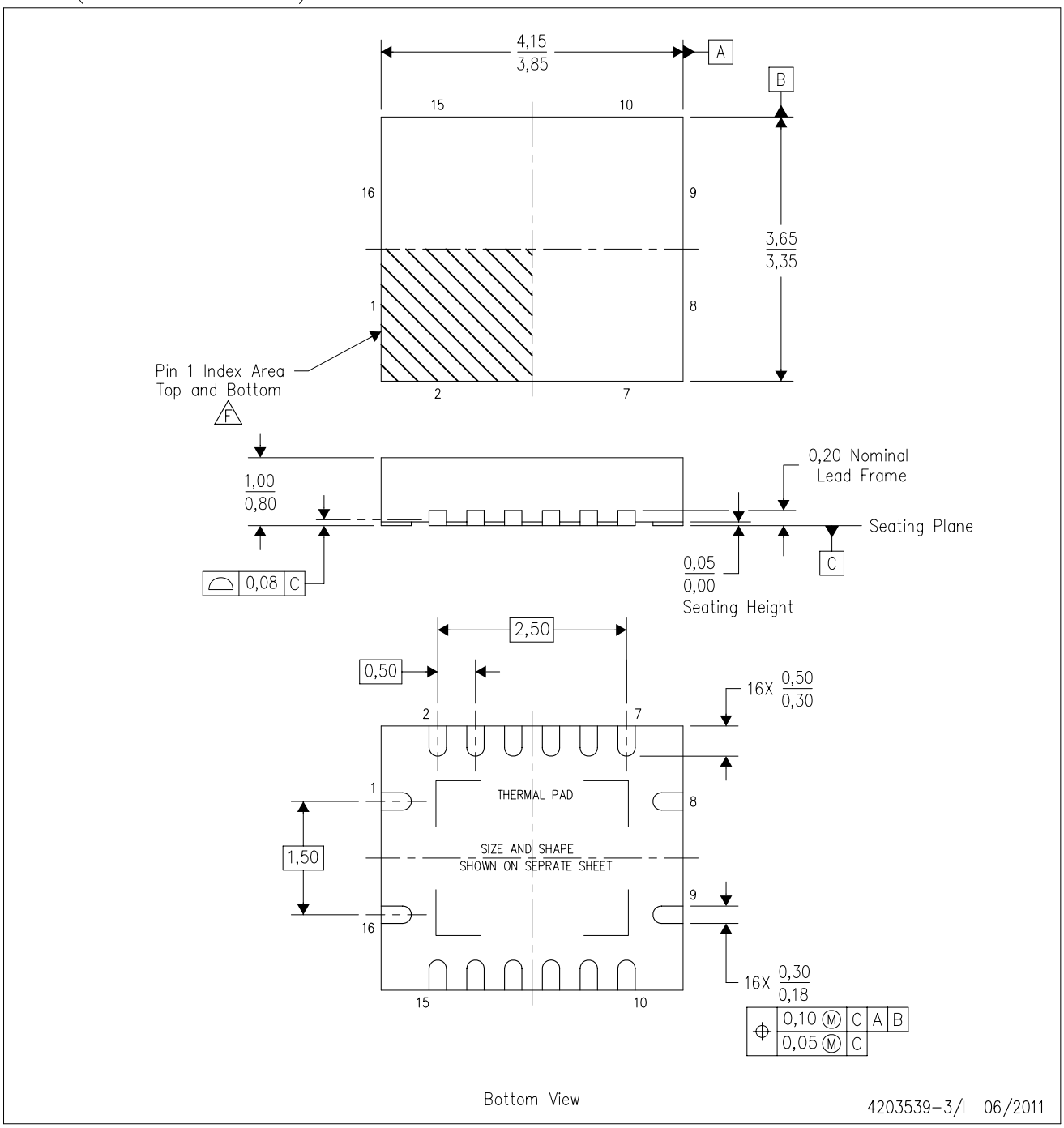


DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

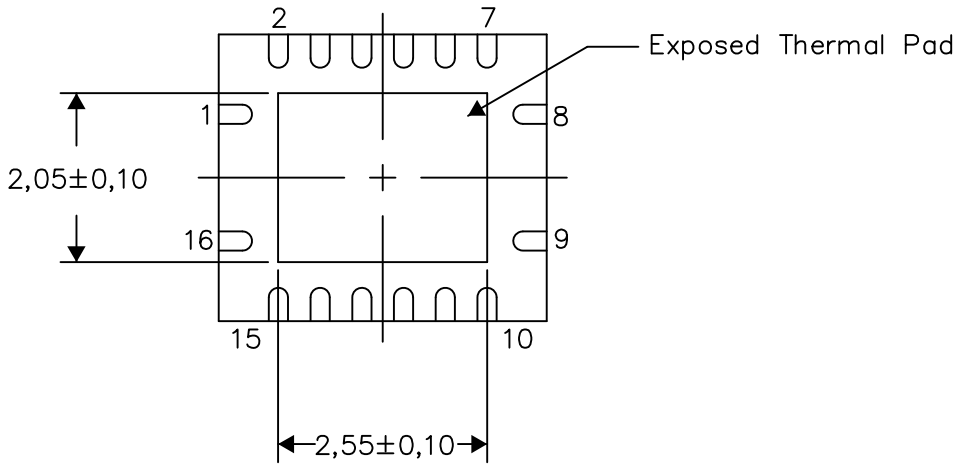
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



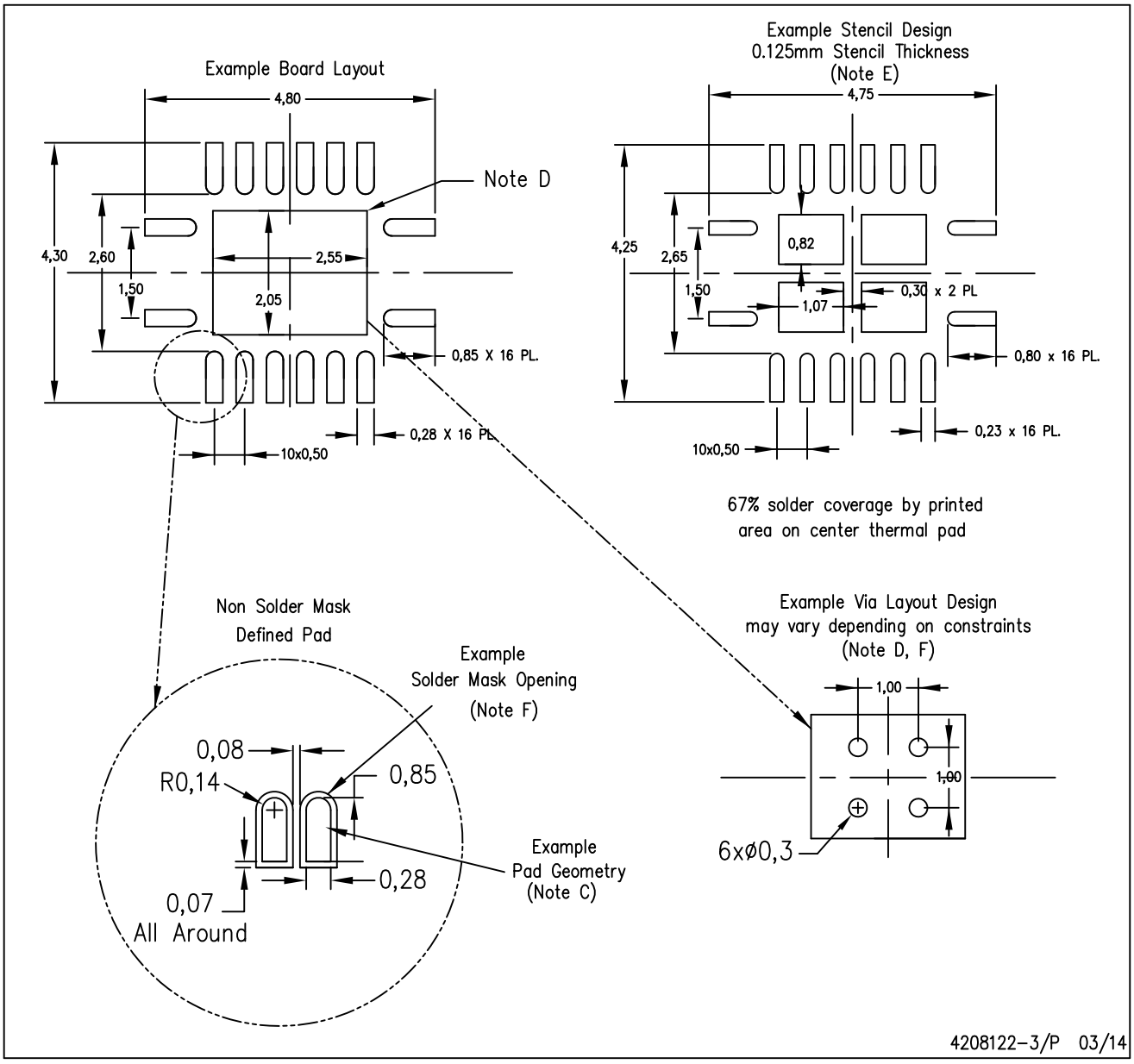
Bottom View

Exposed Thermal Pad Dimensions

4206353–3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

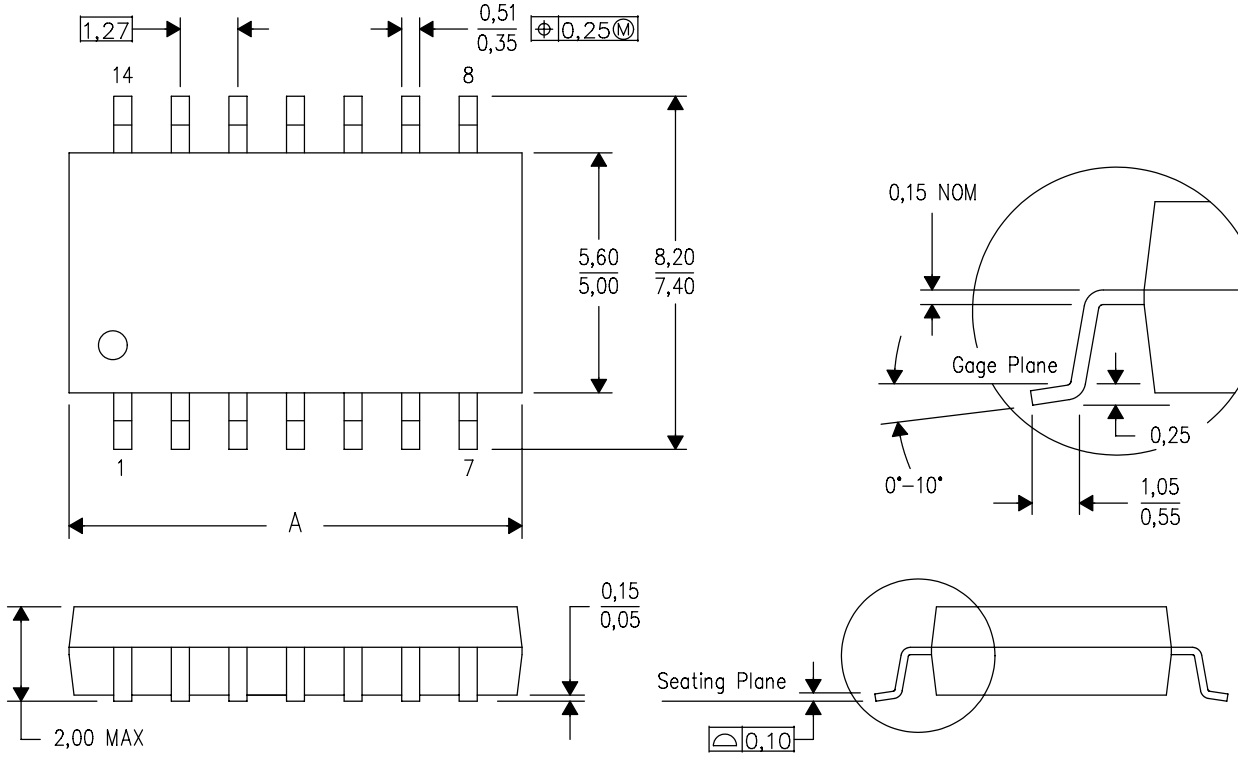


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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