Broadband, Fully-Differential, 14-/16-Bit ADC Driver Amplifier

Check for Samples: THS770012

FEATURES

- **900MHz Bandwidth at Gain of +10dB**
- **3300V/µs Slew Rate, V_{OUT} = 2V step**
- **Adjustable Gain: +10dB to +13.7dB**
- **IMD_3: –100dBc, V_{OUT} = $2V_{PP}$, R_L = 400Ω, f = 100MHz**
- **OIP3: 47dBm, f = 100MHz**
- **Noise Figure: 10.7 dB, f = 100MHz**

APPLICATIONS

- **14-/16-Bit ADC Driver**
- **ADC Driver for Wireless Base Station Signal Chains: GSM, WCDMA, MC-GSM, LTE**
- **ADC Driver for High Dynamic Range Test and Measurement Equipment**

Figure 1. THS770012 Driving 16-Bit ADC

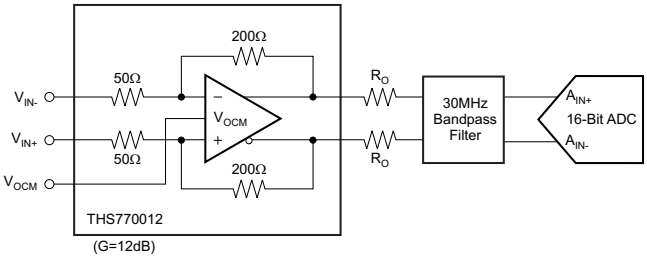
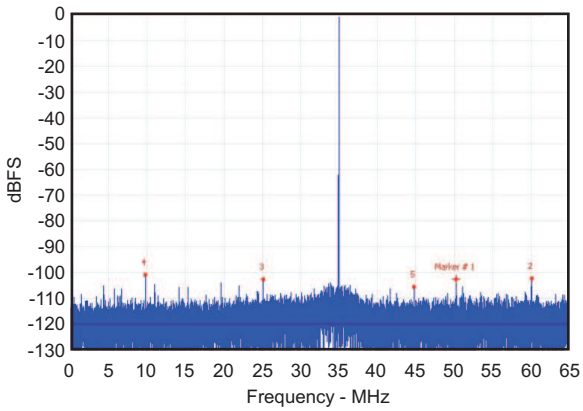


Figure 2. FFT Plot with Two-Tone Input at 96MHz and 100MHz (see *Application Information* section)



DESCRIPTION

The THS770012 is a wideband, fully-differential amplifier, with adjustable gain range from +10dB to +13.7dB (with external components). It is designed and optimized specifically for driving 16-bit analog-to-digital converters (ADCs) at input frequencies up to 130MHz, and 14-bit ADCs at input frequencies up to 200MHz. This device provides high bandwidth, high-voltage output with low distortion and low noise, critical in high-speed data acquisition systems that require very high dynamic range, such as wireless base stations and test and measurement applications. This device also makes an excellent differential amplifier for general-purpose, high-speed differential signal chain and short line driver applications.

The THS770012 operates on a nominal +5V single supply, offers very fast, 7.5ns maximum recovery time from overdrive conditions, and has a power-down mode for power saving. The THS770012 is offered in a Pb-free (RoHS compliant) and green, QFN-24 thermally-enhanced package. It is characterized for operation over the industrial temperature range of –40°C to +85°C.

RELATED DEVICES

DEVICE	DESCRIPTION
THS770006	Fixed Gain of +6dB, wideband, low-noise, low-distortion, fully-differential amplifier
THS4509	Wideband, low-noise, low-distortion, fully-differential amplifier
PGA870	Wideband, low-noise, low-distortion, fully-differential, digitally-programmable gain amplifier
ADS5481 to ADS5485	16-bit, 80MSPS to 200MSPS ADCs
ADS6145	14-bit, 125MSPS ADC
ADS6149	14-bit, 250MSPS ADC

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

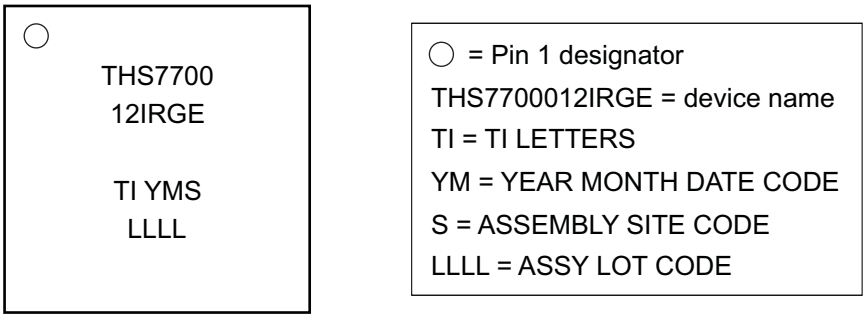
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE TYPE	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
THS770012	VQFN-24	RGE	–40°C to +85°C	THS770012IRGE	THS770012IRGET	Tape and reel, 250
				THS770012IRGE	THS770012IRGER	Tape and reel, 3000

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

Figure 3. DEVICE MARKING INFORMATION



ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		THS770012	UNIT
Power supply (V_{S+} to GND)		5.5	V
Input voltage range		Ground to V_{S+}	V
Differential input voltage, V_{ID}		Ground to V_{S+}	V
Continuous input current, I_I		10	mA
Continuous output current, I_O		100	mA
Storage temperature range, T_{stg}		–65°C to +150°C	°C
Maximum junction temperature, T_J		+150	°C
Maximum junction temperature, continuous operation, long term reliability		+125	°C
ESD ratings	Human body model (HBM)	2500	V
	Charged device model (CDM)	1000	V
	Machine model (MM)	100	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

THERMAL INFORMATION

THERMAL METRIC(1)		THS770012 RGE (24) PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	44.1	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	35	
θ_{JB}	Junction-to-board thermal resistance	19	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	18.8	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	8.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

Test conditions are at T_A = +25°C, V_{S+} = +5V, V_{OCM} = +2.5V, V_{OUT} = $2V_{PP}$, R_L = 400Ω differential, G = +12dB, differential input and output, and input and output referenced to midsupply, unless otherwise noted. Measured using evaluation module as discussed in *Test Circuits* section.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
AC PERFORMANCE						
Small-signal bandwidth	Gain = +10dB, V_{OUT} = $200mV_{PP}$		900		MHz	C
	Gain = +11dB, V_{OUT} = $200mV_{PP}$		810		MHz	C
	Gain = +12dB, V_{OUT} = $200mV_{PP}$		680		MHz	C
	Gain = +13.7dB, V_{OUT} = $200mV_{PP}$		540		MHz	C
Large-signal bandwidth	Gain = +10dB, V_{OUT} = $2V_{PP}$		845		MHz	C
	Gain = +11dB, V_{OUT} = $2V_{PP}$		790		MHz	C
	Gain = +12dB, V_{OUT} = $2V_{PP}$		680		MHz	C
	Gain = +13.7dB, V_{OUT} = $2V_{PP}$		548		MHz	C
Bandwidth for 0.1dB flatness	Gain = +12dB, V_{OUT} = $2V_{PP}$		130		MHz	C
Slew rate	V_{OUT} = 2V step		3300		V/µs	C
	V_{OUT} = 4V step		3400		V/µs	C
Rise time	V_{OUT} = 2V step		0.6		ns	C
Fall time	V_{OUT} = 2V step		0.6		ns	C
Settling time to 0.1%	V_{OUT} = 2V step		2.2		ns	C
Input return loss, s11	See *s-Parameters* section, f < 200MHz		–18		dB	C
Output return loss, s22	See *s-Parameters*section, f < 200MHz		–16		dB	C
Reverse isolation, s12	See *s-Parameters* section, f < 200MHz		–60		dB	C
Second-order harmonic distortion, Gain = +12dB, R_L = 400Ω, V_{OUT} = $2V_{PP}$	f = 10MHz		–90		dBc	C
	f = 50MHz		–70		dBc	C
	f = 100MHz		–73		dBc	C
	f = 200MHz		–74		dBc	C
Third-order harmonic distortion, Gain = +12dB, R_L = 400Ω, V_{OUT} = $2V_{PP}$	f = 10MHz		–100		dBc	C
	f = 50MHz		–85		dBc	C
	f = 100MHz		–84		dBc	C
	f = 200MHz		–73		dBc	C
Second-order intermodulation distortion, Gain = +12dB, R_L = 400Ω, V_{OUT} = $2V_{PP}$	f = 50MHz, 10MHz spacing		–62		dBc	C
	f = 100MHz, 10MHz spacing		–76		dBc	C
	f = 150MHz, 10MHz spacing		–78		dBc	C
	f = 200MHz, 10MHz spacing		–78		dBc	C

(1) Test levels: (A) 100% tested at +25°C. Over-temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

ELECTRICAL CHARACTERISTICS (continued)

Test conditions are at T_A = +25°C, V_{S+} = +5V, V_{OCM} = +2.5V, V_{OUT} = $2V_{PP}$, R_L = 400Ω differential, G = +12dB, differential input and output, and input and output referenced to midsupply, unless otherwise noted. Measured using evaluation module as discussed in *Test Circuits* section.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL(1)
Third-order intermodulation distortion, Gain = +12dB, R_L = 400Ω, V_{OUT} = $2V_{PP}$	f = 50MHz, 10MHz spacing			–97		dBc	C
	f = 100MHz, 10MHz spacing			–100		dBc	C
	f = 150MHz, 10MHz spacing			–92		dBc	C
	f = 200MHz, 10MHz spacing			–81		dBc	C
1dB compression point	f = 100MHz	R_L = 20Ω		19.6		dBm	C
		R_L = 400Ω		8.7		dBm	C
Output third-order intercept point	At device outputs, R_L = 400Ω, f = 100MHz			47		dBm	C
Input-referred voltage noise	f = 1MHz			1.5		nV/√Hz	C
Ouput-referred voltage noise	f = 1MHz			6		nV/√Hz	C
Noise figure	100Ω differential source	f = 50 MHz		9.5		dB	C
		f = 100 MHz		10.7		dB	C
		f = 200 MHz		12.3		dB	C
Overdrive recovery	Overdrive = ±0.5V			5	7.5	ns	B
Output balance error	f = 200MHz			-60		dB	C
Output impedance	f = 100MHz			4		Ω	C
DC PERFORMANCE							
Gain (+12dB gain setting)	T_A = +25°C, R_L = 400Ω		11.65	11.9	12.15	dB	A
	T_A = +25°C, R_L = 100Ω		11.4	11.6	11.85	dB	B
	T_A = –40°C to +85°C, R_L = 400Ω		11.6		12.2	dB	B
	T_A = –40°C to +85°C, R_L = 100Ω		11.6		12.2	dB	B
Output offset	T_A = +25°C		–20	±2	20	mV	A
	T_A = –40°C to +85°C		–22.5		22.5	mV	B
Common-mode rejection ratio	T_A = +25°C		36	60		dB	A
	T_A = –40°C to +85°C		35			dB	B
INPUT							
Differential input resistance			85	100	115	Ω	A
Input common-mode range	Inputs shorted together, V_{OCM} = 2.5V		2.25		2.75	V	A
OUTPUT							
Most positive output voltage	Each output with 200Ω to midsupply	T_A = +25°C	3.64	3.7		V	A
		T_A = –40°C to +85°C	3.59			V	B
Least positive output voltage	Each output with 200Ω to midsupply	T_A = +25°C		1.3	1.4	V	A
		T_A = –40°C to +85°C			1.45	V	B
Most positive output voltage	Each output with 50Ω to midsupply	T_A = +25°C	3.59	3.6		V	A
		T_A = –40°C to +85°C	3.54			V	B
Least positive output voltage	Each output with 50Ω to midsupply	T_A = +25°C		1.3	1.5	V	A
		T_A = –40°C to +85°C			1.55	V	B
Differential output voltage	T_A = +25°C, R_L = 400Ω		4.4	4.8		V_{PP}	B
	T_A = –40°C to +85°C, R_L = 400Ω		4.2			V_{PP}	B
Differential output current drive	T_A = +25°C, R_L = 10Ω			80		mA	B
	T_A = –40°C to +85°C, R_L =10Ω			80		mA	B

ELECTRICAL CHARACTERISTICS (continued)

Test conditions are at T_A = +25°C, V_{S+} = +5V, V_{OCM} = +2.5V, V_{OUT} = $2V_{PP}$, R_L = 400Ω differential, G = +12dB, differential input and output, and input and output referenced to midsupply, unless otherwise noted. Measured using evaluation module as discussed in *Test Circuits* section.

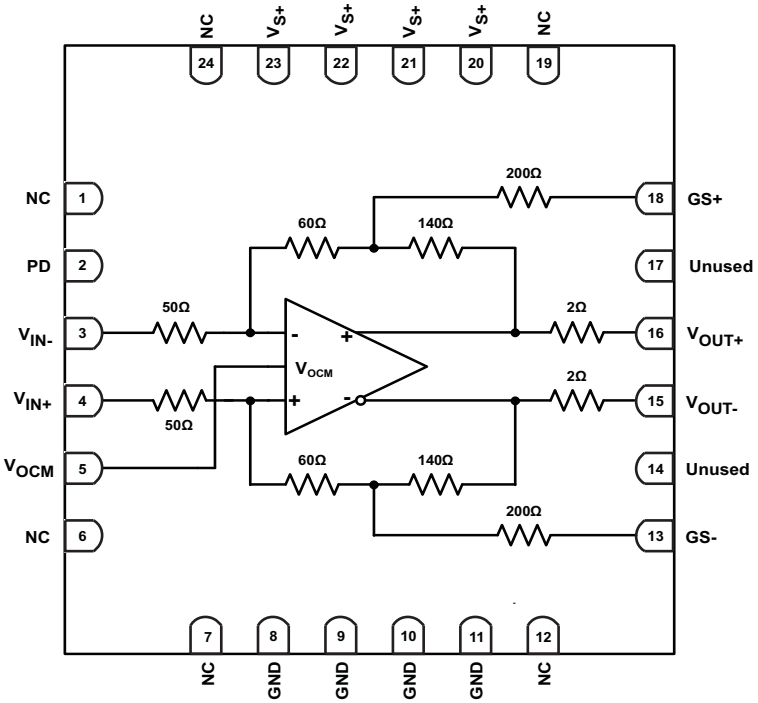
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
OUTPUT COMMON-MODE VOLTAGE CONTROL						
V_{OCM} small-signal bandwidth	V_{OUT_CM} = $200mV_{PP}$		300		MHz	C
V_{OCM} slew rate	V_{OUT_CM} = 500mV step		150		V/µs	C
V_{OCM} voltage range	Supplied by external source(2)	2.25	2.5	2.75	V	C
V_{OCM} gain	V_{OCM} = 2.5V	0.98	1	1.02	V/V	A
Output common-mode offset from V_{OCM} input	V_{OCM} = 2.5V	–30	±12	30	mV	A
V_{OCM} input bias current	2.25V ≤ V_{OCM} ≤ 2.75V	–400	±30	400	µA	A
POWER SUPPLY						
Specified operating voltage		4.75	5	5.25	V	C
Quiescent current	T_A = +25°C	85	100	115	mA	A
	T_A = –40°C to +85°C	80		125	mA	B
Power-supply rejection ratio	T_A = +25°C, V_{S+} = 5V ±0.25V	60	90		dB	A
	T_A = –40°C to +85°C, V_{S+} = 5V ±0.5V	59			dB	B
POWER-DOWN						
Enable voltage threshold	Device powers on below 0.5V			0.5	V	A
Disable voltage threshold	Device powers down above 2.0V	2			V	A
Power-down quiescent current			0.8	3	mA	A
Input bias current			80	100	µA	A
Turn-on time delay	Time to V_{OUT} = 90% of final value		10		µs	C
Turn-off time delay	Time to V_{OUT} = 10% of original value		0.15		µs	C
THERMAL CHARACTERISTICS						
Specified operating range		–40		+85	°C	C
Thermal resistance, θ_{JC}(3)	Junction to case (bottom)		8.9		°C/W	C
Thermal resistance, θ_{JA}(3)	Junction to ambient		44.1		°C/W	C

(2) Limits set by best harmonic distortion with V_{OUT} = $3V_{PP}$. V_{OCM} voltage range can be extended if lower output swing is used or distortion degradation is allowed, and increased bias current into pin is acceptable. For more information, see Figure 18 and Figure 34.

(3) Tested using JEDEC High-K test PCB. Thermal management of the final printed circuit board (PCB) should keep the junction temperature below +125°C for long term reliability.

PIN CONFIGURATION

RGE PACKAGE
VQFN-24
(TOP VIEW)



PIN DESCRIPTIONS

PIN		DESCRIPTION
NO.	NAME	
1	NC	No internal connection
2	PD	Power down. High = low power (sleep) mode. Low = active.
3	V_{IN-}	Inverting input pin
4	V_{IN+}	Non-inverting input pin
5	V_{OCM}	Output common-mode voltage control input pin
6, 7	NC	No internal connection
8, 9, 10, 11	GND	Ground. Must be connected to thermal pad.
12	NC	No internal connection
13	GS-	Gain-setting connection for inverting output
14	Unused	Bonded to die, but not used. Tie to GND.
15	V_{OUT-}	Inverting output pin
16	V_{OUT+}	Non-inverting output pin
17	Unused	Bonded to die, but not used. Tie to GND.
18	GS+	Gain-setting connection for non-inverting output
19	NC	No internal connection
20, 21, 22, 23	V_{S+}	Power supply pins, +5V nominal
24	NC	No internal connection
Thermal pad		Thermal pad on bottom of device is used for heat dissipation and must be tied to GND

TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS

At T_A = +25°C, V_{S+} = +5V, V_{OCM} = +2.5V, V_{OUT} = $2V_{PP}$, R_L = 400Ω differential, G = +12dB, differential input and output, input and output pins referenced to midsupply, unless otherwise noted. Measured using EVM as discussed in *Test Circuits* section.

200mV$_{PP}$ FREQUENCY RESPONSE MAGNITUDE

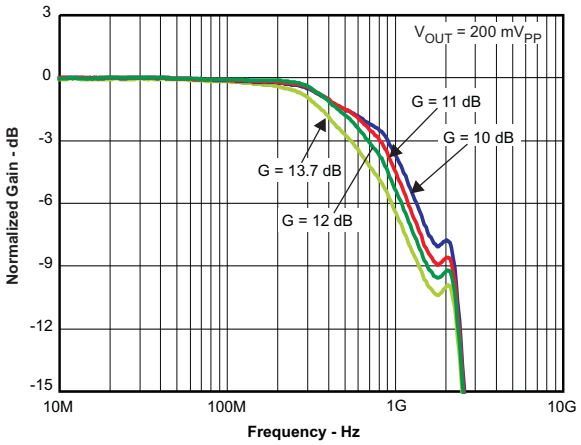

Figure 4.

200mV$_{PP}$ FREQUENCY RESPONSE PHASE

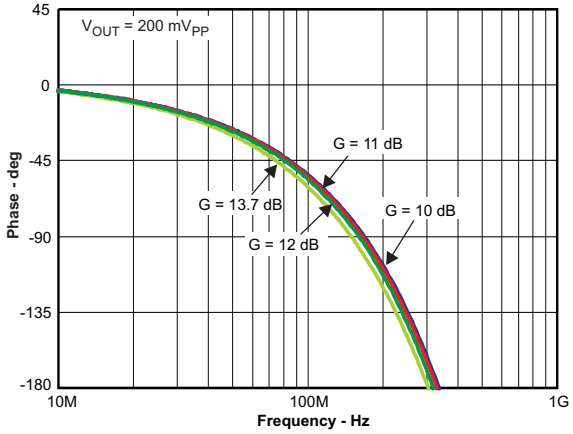

Figure 5.

2V$_{PP}$ FREQUENCY RESPONSE MAGNITUDE

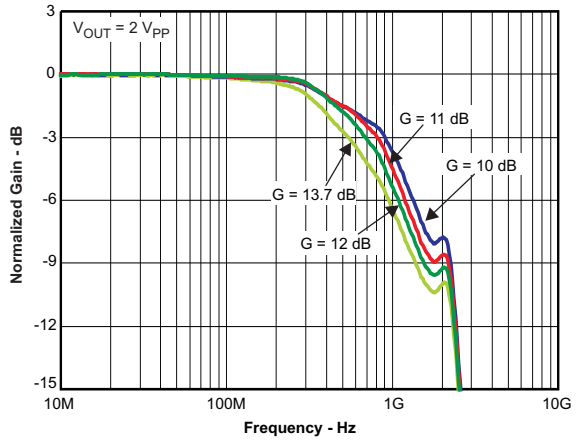

Figure 6.

2V$_{PP}$ FREQUENCY RESPONSE PHASE

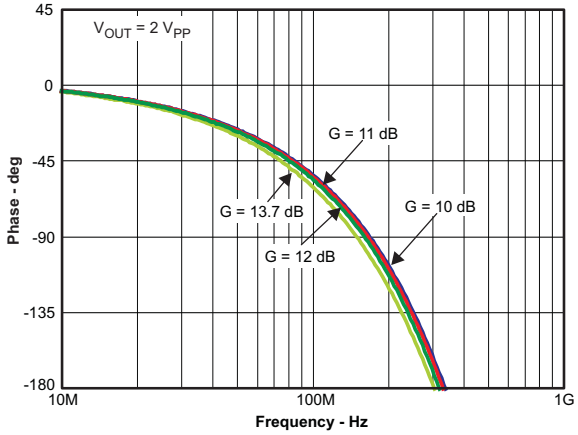

Figure 7.

3V$_{PP}$ FREQUENCY RESPONSE MAGNITUDE

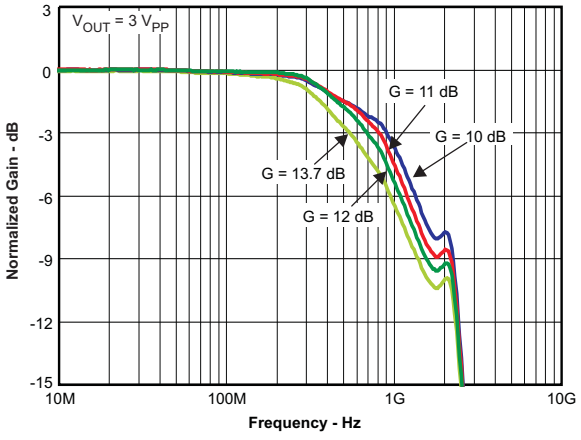

Figure 8.

3V$_{PP}$ FREQUENCY RESPONSE PHASE

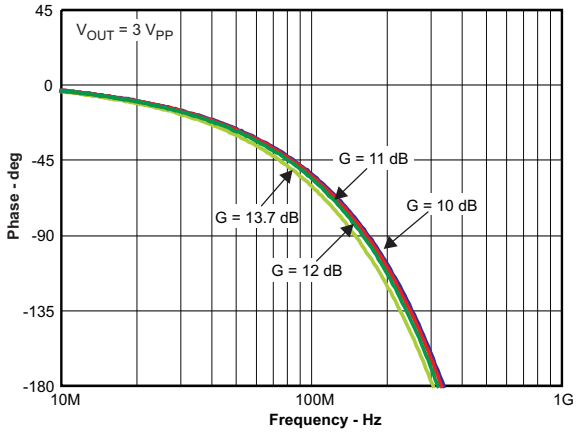

Figure 9.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{S+} = +5V, V_{OCM} = +2.5V, V_{OUT} = 2V_{PP}, R_L = 400Ω differential, G = +12dB, differential input and output, input and output pins referenced to midsupply, unless otherwise noted. Measured using EVM as discussed in *Test Circuits* section.

SMALL- AND LARGE-SIGNAL PULSE RESPONSE

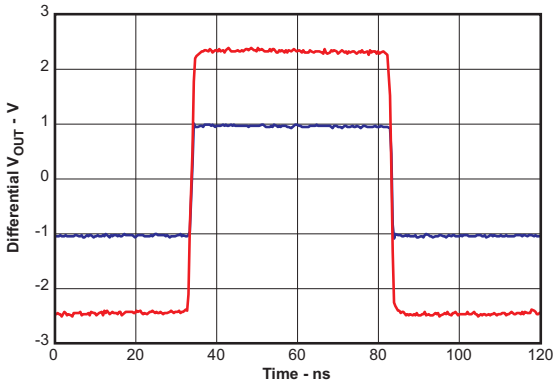

Figure 10.

SLEW RATE vs OUTPUT VOLTAGE STEP

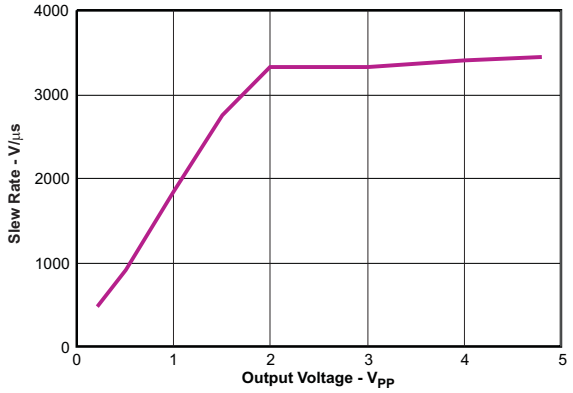

Figure 11.

OVERDRIVE RECOVERY

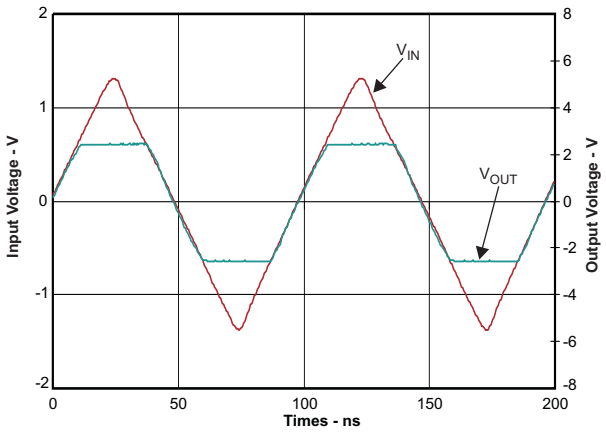

Figure 12.

SINGLE-ENDED INPUT HARMONIC DISTORTION vs FREQUENCY

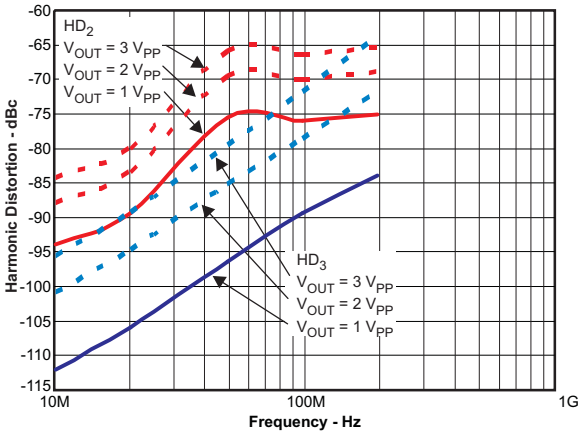

Figure 13.

HARMONIC DISTORTION vs FREQUENCY

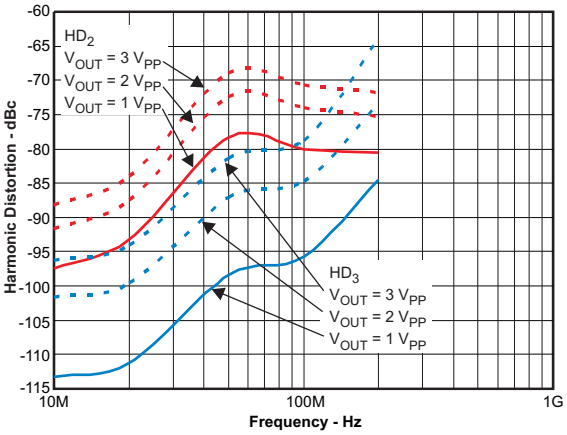

Figure 14.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

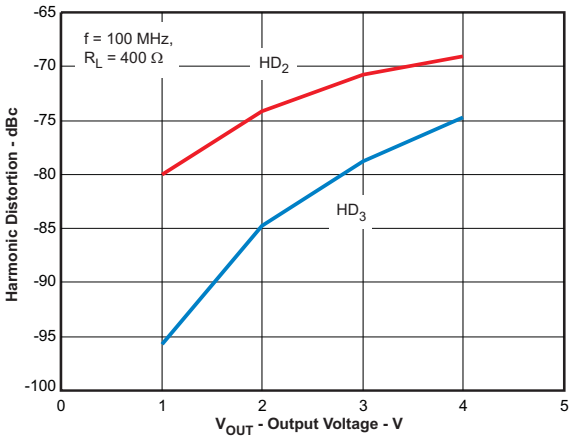

Figure 15.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{S+} = +5V, V_{OCM} = +2.5V, V_{OUT} = 2V_{PP}, R_L = 400Ω differential, G = +12dB, differential input and output, input and output pins referenced to midsupply, unless otherwise noted. Measured using EVM as discussed in *Test Circuits* section.

HARMONIC DISTORTION vs LOAD

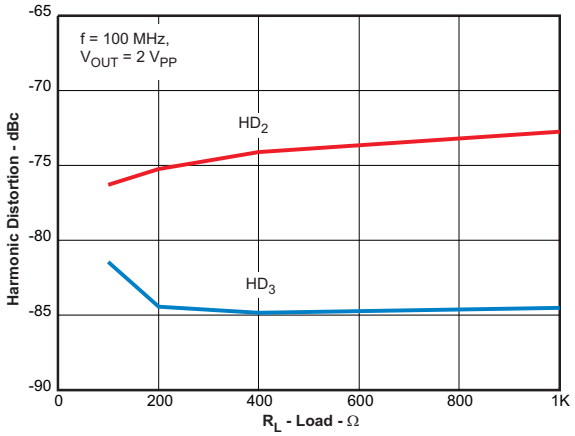

Figure 16.

HARMONIC DISTORTION vs GAIN

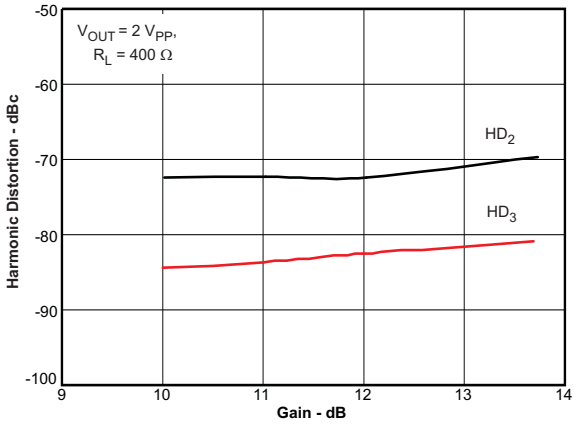

Figure 17.

HARMONIC DISTORTION vs OUTPUT COMMON-MODE VOLTAGE

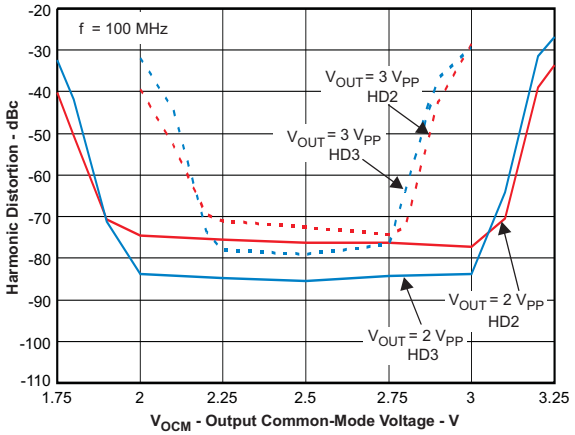

Figure 18.

INTERMODULATION DISTORTION vs FREQUENCY

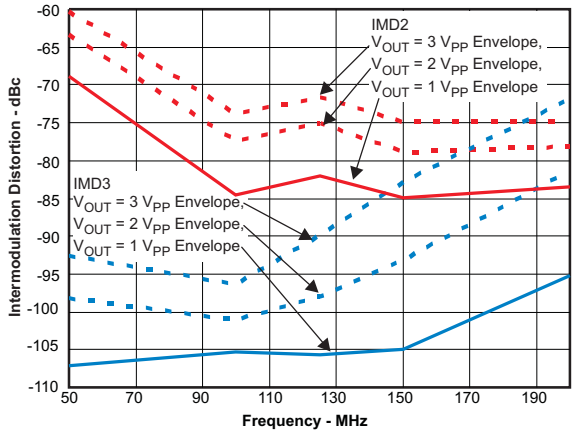

Figure 19.

OUTPUT INTERCEPT POINT vs FREQUENCY

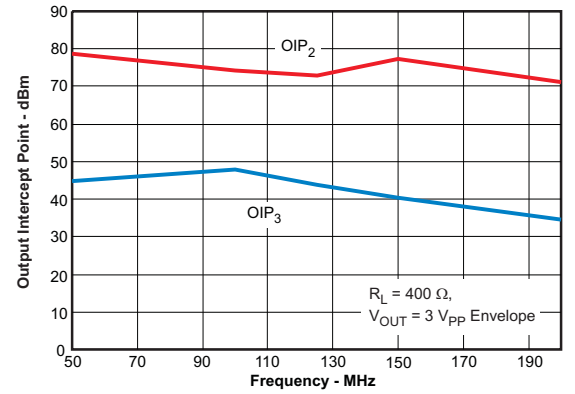

Figure 20.

MAXIMUM DIFFERENTIAL OUTPUT VOLTAGE SWING PEAK-TO-PEAK vs DIFFERENTIAL LOAD RESISTANCE

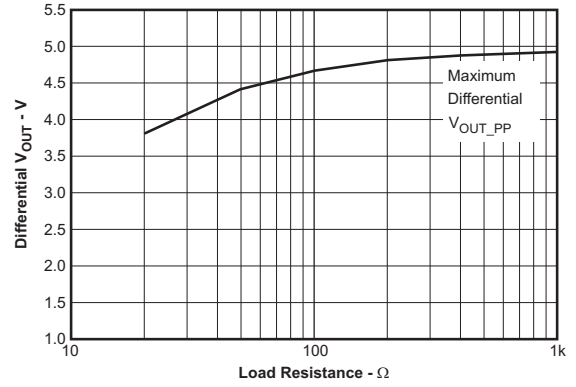

Figure 21.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{S+} = +5V, V_{OCM} = +2.5V, V_{OUT} = $2V_{PP}$, R_L = 400Ω differential, G = +12dB, differential input and output, input and output pins referenced to midsupply, unless otherwise noted. Measured using EVM as discussed in *Test Circuits* section.

MAXIMUM/MINIMUM SINGLE-ENDED OUTPUT VOLTAGE vs DIFFERENTIAL LOAD RESISTANCE

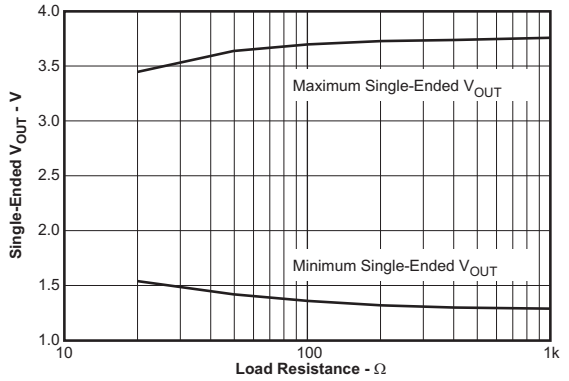

Figure 22.

DIFFERENTIAL OUTPUT IMPEDANCE vs FREQUENCY

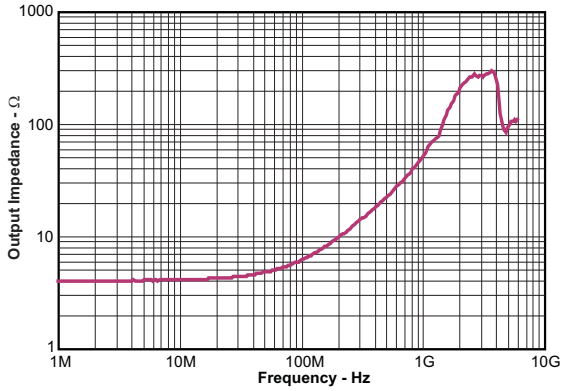

Figure 23.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

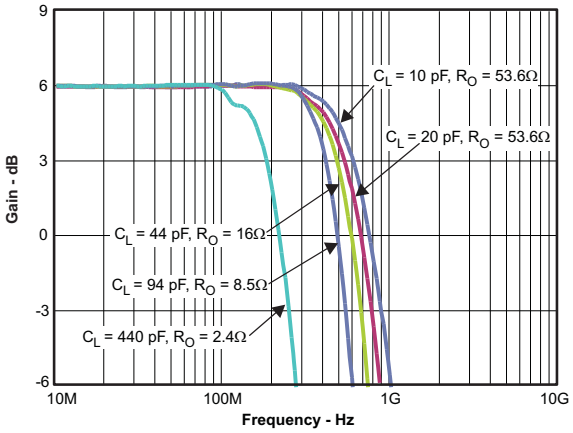

Figure 24.

RECOMMENDED OUTPUT RESISTANCE vs CAPACITIVE LOAD

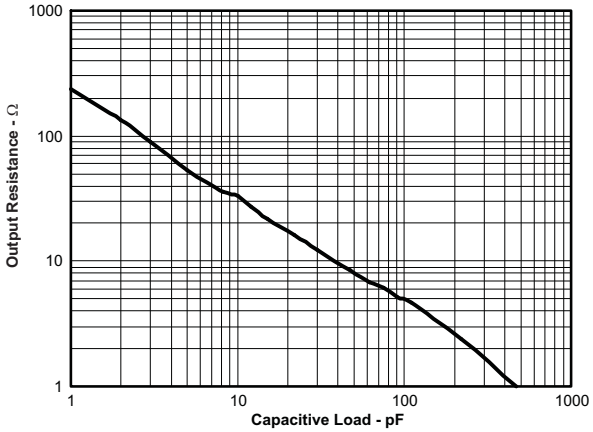

Figure 25.

COMMON-MODE REJECTION RATIO vs FREQUENCY

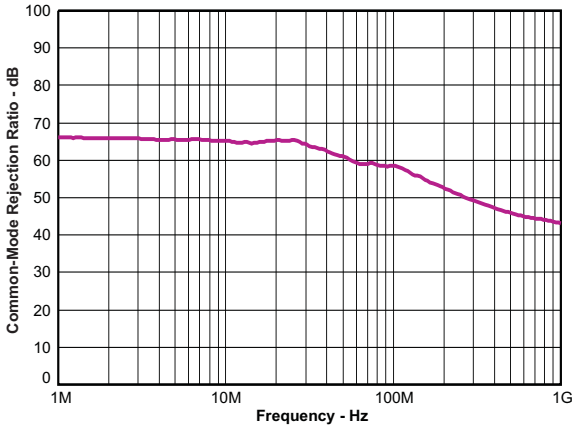

Figure 26.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

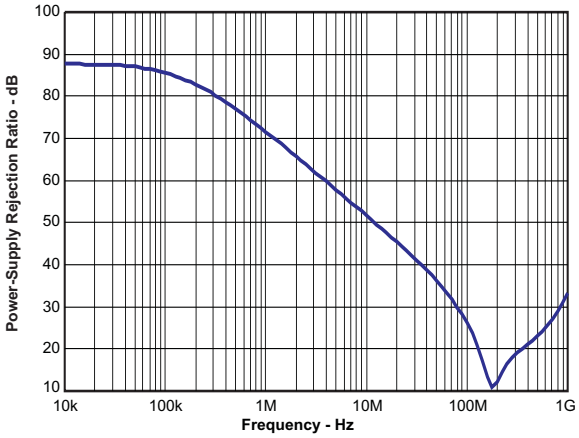

Figure 27.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{S+} = +5V, V_{OCM} = +2.5V, V_{OUT} = $2V_{PP}$, R_L = 400Ω differential, G = +12dB, differential input and output, input and output pins referenced to midsupply, unless otherwise noted. Measured using EVM as discussed in *Test Circuits* section.

TURN-ON TIME

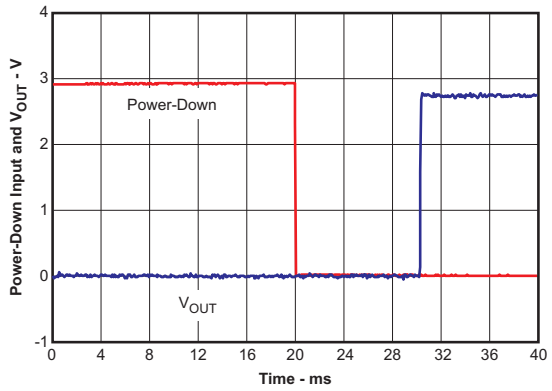

Figure 28.

TURN-OFF TIME

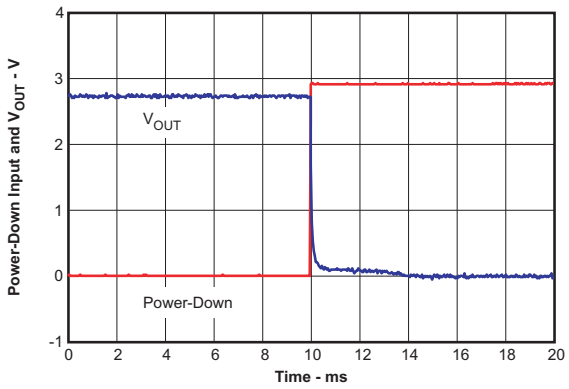

Figure 29.

INPUT AND OUTPUT VOLTAGE NOISE vs FREQUENCY

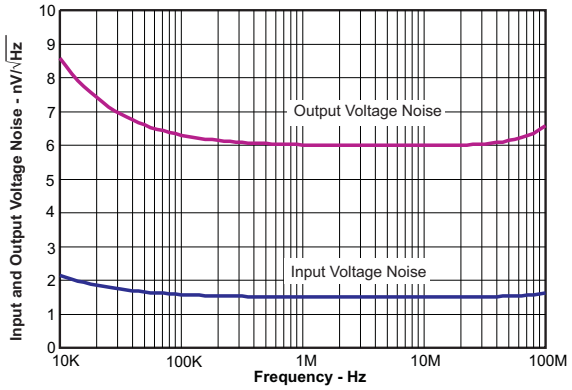

Figure 30.

OUTPUT BALANCE ERROR vs FREQUENCY

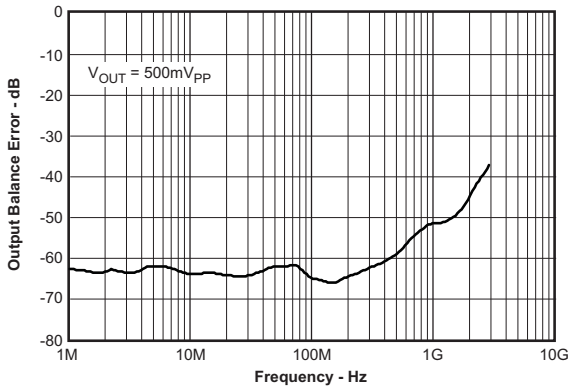

Figure 31.

V_{OCM} SMALL-SIGNAL FREQUENCY RESPONSE

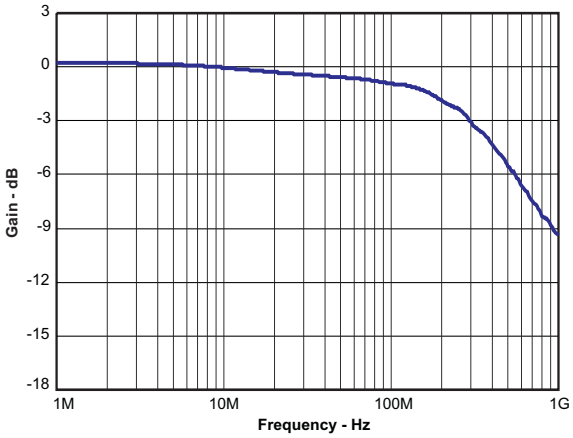

Figure 32.

OUTPUT COMMON-MODE PULSE RESPONSE

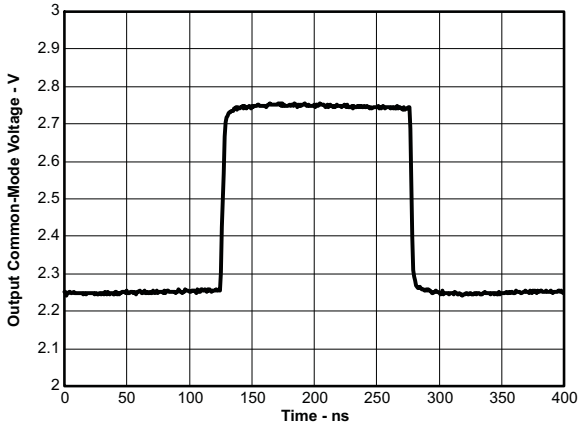

Figure 33.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{S+} = +5V, V_{OCM} = +2.5V, V_{OUT} = $2V_{PP}$, R_L = 400Ω differential, G = +12dB, differential input and output, input and output pins referenced to midsupply, unless otherwise noted. Measured using EVM as discussed in *Test Circuits* section.

V_{OCM} INPUT BIAS CURRENT vs V_{OCM} INPUT VOLTAGE

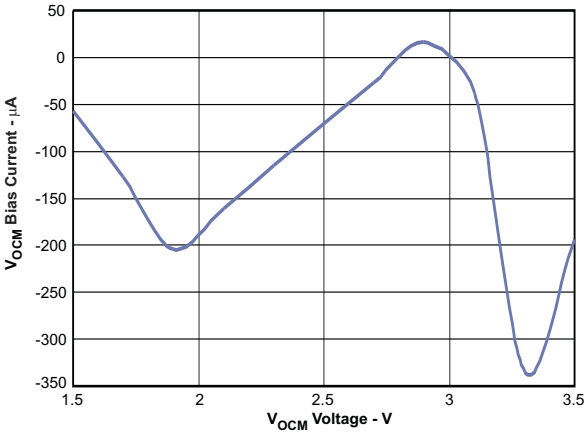

Figure 34.

s-PARAMETERS (MAGNITUDE)

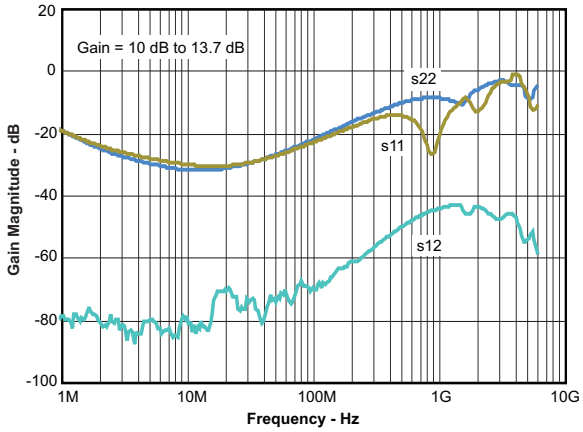

Figure 35.

NOISE FIGURE vs FREQUENCY

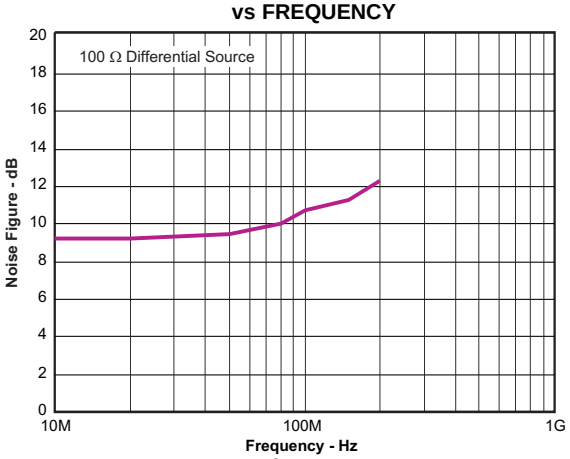

Figure 36.

TEST CIRCUITS

OVERVIEW

The standard THS770012 evaluation module (EVM) is used for testing the typical performance shown in the Typical Characteristics, with changes as noted below. The EVM schematic is shown in Figure 37. The signal generators and analyzers used for most tests have single-ended 50Ω input and output impedance. The THS770012 EVM is configured to convert to and from a single-ended 50Ω impedance by using RF transformers or baluns 1:1 (CX2156NL from Pulse, supplied as a standard configuration of the EVM) to allow easy connection to standard lab equipment. For line input termination, two 49.9Ω resistors (R5 and R6) are placed to ground on the input transformer output pins (terminals 1 and 3). In combination with the 100Ω input impedance of the device, the total impedance seen by the line is 50Ω.

Gain is set by placing external components R11, R12, R13, and R14 as described below in Setting the Gain section.

A resistor network is used on the amplifier output to present various loads (R_L) and maintain line output termination to 50Ω. Depending on the test conditions, component values are changed as shown in Table 1, or as otherwise noted. As a result of the voltage divider on the output formed by the load component values, the amplifier output is attenuated. The *Loss* column in Table 1 shows the attenuation expected from the resistor divider. The output transformer causes slightly more loss, so these numbers are approximate.

Table 1. Load Component Values(1)

LOAD R_L	R15 AND R17	R16	LOSS
100Ω	25Ω	Open	6dB
200Ω	86.6Ω	69.8Ω	16.8dB
400Ω	187Ω	57.6Ω	25.5dB
1kΩ	487Ω	52.3Ω	31.8dB

(1) The total load includes 50Ω termination by the test equipment. Components are chosen to achieve load and 50Ω line termination through a 1:1 transformer.

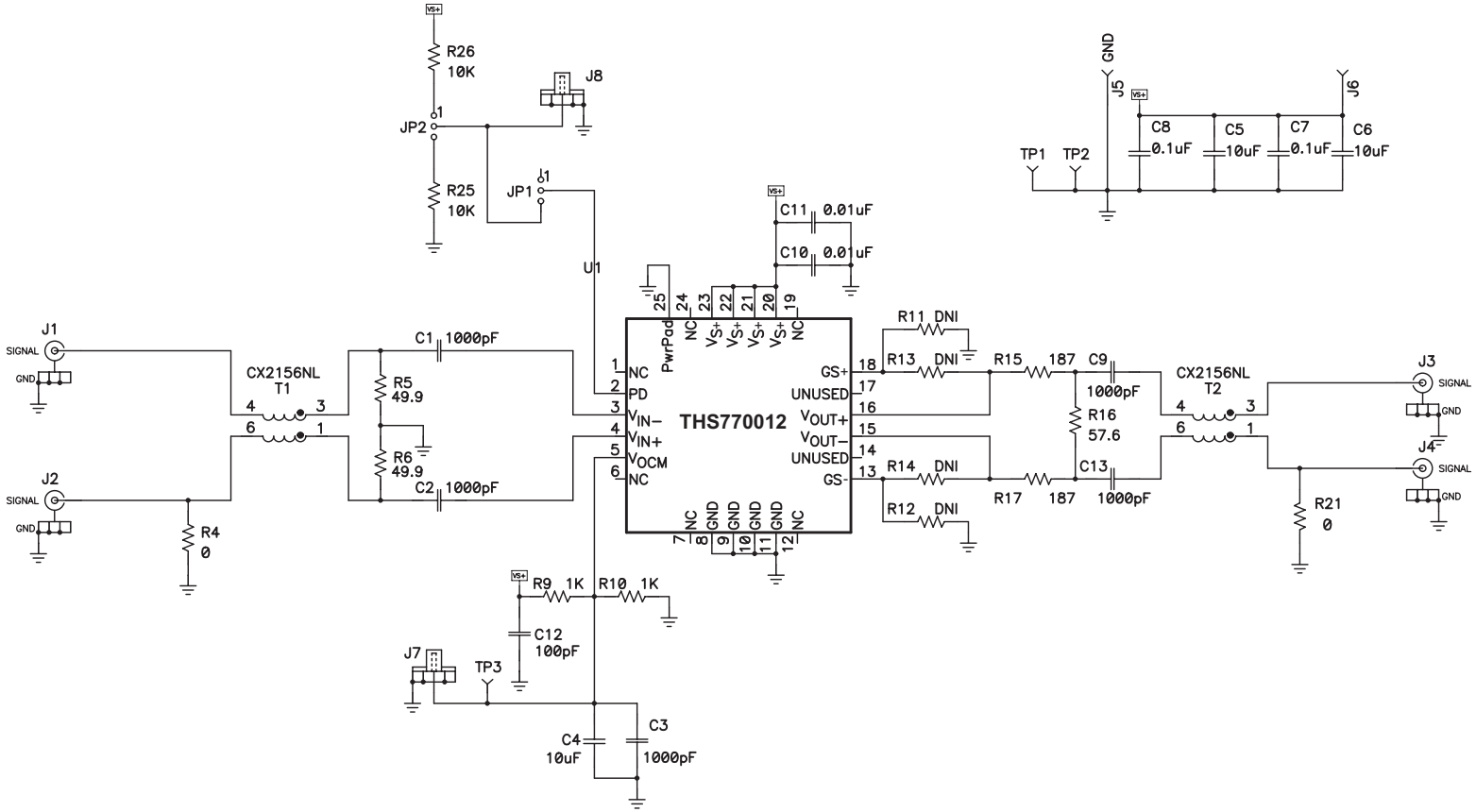

Figure 37. THS770012IRGE EVM Schematic

TEST DESCRIPTIONS

The following sections describe how the tests were performed, as well as the EVM circuit modifications that were made (if any). Modifications made for test purposes include changing capacitors to resistors, resistors to capacitors, the shorting/opening of components, etc., as noted. Unless otherwise noted, C1, C2, C9, and C13 are all changed to 0.1µF to give basically flat frequency response from below 1MHz to the bandwidth of the amplifier, and gain is set to nominal +12dB.

Frequency Response: 200mV$_{PP}$, 2V$_{PP}$, 3V$_{pp}$

The test is run on the standard EVM using the transformers in the signal path.

A network analyzer is connected to the input and output of the EVM with 50Ω coaxial cables and set to measure the forward transfer function (s21). The input signal frequency is swept with signal level set for desired output amplitude.

The test ran for gains of +10dB, +11dB, +12dB and +13.7dB with component values changed per Table 2 in Setting the Gain section.

s-Parameters: s11, s22, and s12

The standard EVM is used with both R15 and R17 = 24.9Ω, and R16 = open, to test the input return loss, output return loss, and reverse isolation. A network analyzer is connected to the input and output of the EVM with 50Ω coaxial cables and set to measure the appropriate transfer function: s11, s22, or s12. Note the transformers are included in the signal chain in order to retrieve proper measurements with single-ended test equipment. The impact is minimal from 10MHz to 200MHz, but further analysis is required to fully de-embed the respective effects.

Frequency Response with Capacitive Load

The standard EVM is used with R15 and R17 = R_O, R16 = C_{LOAD}, C9 and C13 = 953Ω, R21 = open, T2 removed, and jumpers placed across terminals 3 to 4 and 1 to 6. A network analyzer is connected to the input and output of the EVM with 50Ω coaxial cables and set to measure the forward transfer function (s21). Different values of load capacitance are placed on the output (at R16) and the output resistor values (R15 and R17) changed until an optimally flat frequency response is achieved with maximum bandwidth.

Distortion

The standard EVM is used for measurement of single-tone harmonic distortion and two-tone intermodulation distortion. For differential distortion measurements, the standard EVM is used with no modification. For single-ended input distortion measurements, the standard EVM is used with with T1 removed and jumpers placed across terminals 3 to 4 and 1 to 6, and R5 and R6 = 100Ω. A signal generator is connected to the J1 input of the EVM with 50Ω coaxial cables, with filters inserted inline to reduce distortion from the generator. The J3 output of the EVM is connected with 50Ω coaxial cables to a spectrum analyzer to measure the fundamental(s) and distortion products.

Noise Figure

The standard EVM is used with T1 changed to a 1:2 impedance ratio transformer (Mini-Circuits ADT2), R15 and R17 = 24.9Ω, and R5, R6, and R16 = open. A noise figure analyzer is connected to the input and output of the EVM with 50Ω coaxial cables. The noise figure analyzer provides a 50Ω (noise) source so that the data are adjusted to refer to a 100Ω source.

Transient Response, Slew Rate, Overdrive Recovery

The standard EVM is used with T1 and T2 removed and jumpers placed across terminals 3 to 4 and 1 to 6; R15, R17, and R25 = 49.9Ω; C1, C2, C9, and C13 = 0Ω; and R5, R6, R16, and R21 = open. A differential waveform generator is connected to the input of the EVM with 50Ω coaxial cables at J1 and J2. The differential output at J3 and J4 is connected with 50Ω coaxial cables to an oscilloscope to measure the outputs. Waveform math in the oscilloscope is used to combine the differential output of the device.

Power-Down

The standard EVM is used with T1 and T2 removed, jumpers placed across terminals 3 to 4 and 1 to 6, R15 and R17 = 49.9Ω, C9 and C13 = 0Ω, and R5, R6, R16, and R21 = open. A waveform generator is connected to the power-down input of the EVM with a 50Ω coaxial cable at J8. The differential output at J3 and J4 is connected with 50Ω coaxial cables to an oscilloscope to measure the outputs. J1 is left disconnected so that the output is driven to the V_{OCM} voltage when the device is active, and discharged through the resistive load on the output when disabled. Both outputs are the same and only one is shown.

Differential Z-out

The standard EVM is used with R15 and R17 = 24.9Ω, and R16 = open. A network analyzer is connected to the output of the EVM at J3 with 50Ω coaxial cable, both inputs are terminated with a 50Ω load, and a high-impedance differential probe is used for the measurement. The analyzer is set to measure the forward transfer function (s21). The analyzer with probe input is calibrated across the open resistor pads of R16 and the signal is measured at the output pins of the device. The output impedance is calculated using the known resistor values and the attenuation caused by R15 and R17.

Output Balance Error

The standard EVM is used with R15 and R17 = 100Ω, and R16 = 0Ω. A network analyzer is connected to the input of the EVM with 50Ω coaxial cable, the output is left open, and a high-impedance differential probe is used for the measurement. The analyzer is set to measure the forward transfer function (s21). The analyzer with probe input is calibrated at the input pins of the device and the signal is measured from the shorted pads of R16 to ground.

Common-Mode Rejection

The standard EVM is used with T1 removed and jumpers place across terminals 3 to 4, 1 to 6, and 1 to 3. A network analyzer is connected to the input and output of the EVM with 50Ω coaxial cable and set to measure the forward transfer function (s21).

V_{OCM} Frequency Response

The standard EVM is used with T2 removed and jumpers across terminals 3 to 4 and 1 to 6; R10, R15, and R17 = 49.9Ω; C3 and C4 = 0Ω; and R9, R16, and R21 = open. A network analyzer is connected to the V_{OCM} input of the EVM at J7 and output of the EVM with 50Ω coaxial cable, and set to measure the forward transfer function (s21). The input signal frequency is swept with the signal level set for 200mV. Each output at J3 and J4 is measured as single-ended, and because both are the same, only one output is shown.

V_{OCM} Slew Rate and Pulse Response

The standard EVM is used with T2 removed and jumpers across terminals 3 to 4 and 1 to 6; R10, R15, and R17 = 49.9Ω; C9 and C13 = 0Ω; and C3, C4, R9, R16, and R21 = open. A waveform generator is connected to the V_{OCM} input of the EVM at J7 with 50Ω coaxial cable. The differential output at J3 and J4 is connected with 50Ω coaxial cable to an oscilloscope to measure the outputs. J1 is left disconnected so that the output is driven to the V_{OCM} voltage. Both outputs are the same, so only one is shown.

Input/Output Voltage Noise, Settling Time, and Power-Supply Rejection

These parameters are taken from simulation.

THEORY OF OPERATION

GENERAL DESCRIPTION

The THS770012 is a wideband, fully differential amplifier designed and optimized specifically for driving 14-bit and 16-bit ADCs at input frequencies up to 200MHz. This device provides high bandwidth, low distortion, and low noise, which are critical parameters in high-speed data acquisition systems that require very high dynamic range, such as wireless base stations and test and measurement applications. It also makes an excellent differential amplifier for general-purpose, high-speed differential signal chain and short line-driver applications. The device has an operating power-supply range of 4.75V to 5.5V. The THS770012 has proprietary circuitry to provide very fast recovery from overdrive conditions and has a power-down mode for power saving. The THS770012 is offered in a Pb-free (RoHS compliant) and green, QFN-24 thermally-enhanced package. It is characterized for operation over the industrial temperature range of –40°C to +85°C.

The amplifier uses two negative-feedback loops. One is for the primary differential amplifier and the other controls the common-mode operation.

Primary Differential Amplifier

The primary amplifier of the THS770012 is a fully-differential op amp with on-chip gain setting resistors. The gain of the device can be changed by using external components as described in Setting the Gain section below. The nominal gain with no external connections is set to +12dB with R_F = 200Ω and R_G = 50Ω.

V_{OCM} Control Loop

The output common-mode voltage is controlled through a second negative-feedback loop. The output common-mode voltage is internally sensed and compared to the V_{OCM} pin. The loop then works to drive the difference, or error voltage, to zero in order to maintain the output common-mode voltage = V_{OCM} (within the loop gain and bandwidth of the loop). For more details on fully-differential amplifier theory and use, see application report SLOA054, *Fully-Differential Amplifiers*, available for download from www.ti.com.

OPERATION

Differential to Differential

The THS770012 is a fully-differential amplifier that can be used to amplify differential input signals to differential output signals. A basic block diagram of the circuit with nominal gain of +12dB is shown in Figure 38. The differential input to differential output configuration gives the best performance; the signal source and load should be balanced.

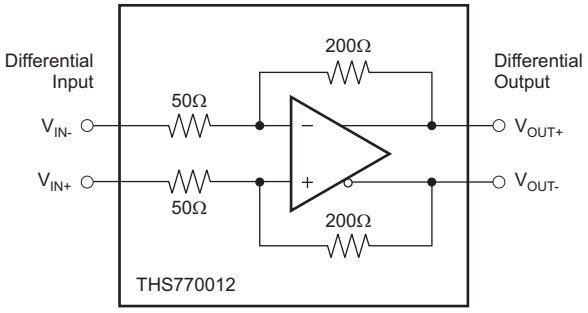

Figure 38. Differential Input to Differential Output Amplifier

Single-Ended to Differential

The THS770012 can be used to amplify and convert single-ended input signals to differential output signals. A basic block diagram of the circuit with nominal gain of +12dB is shown in Figure 39. In order to maintain proper balance in the amplifier and avoid offsets at the output, the alternate input must be biased and the impedance matched to the signal input. For example, if a 50Ω source biased to 2.5V provides the input, the alternate input should be tied to 2.5V through 50Ω. If a 50Ω source is ac-coupled to the input, the alternate input should be ac-coupled to ground through 50Ω. Note that the ac coupling should provide a similar frequency response to balance the gain over frequency.

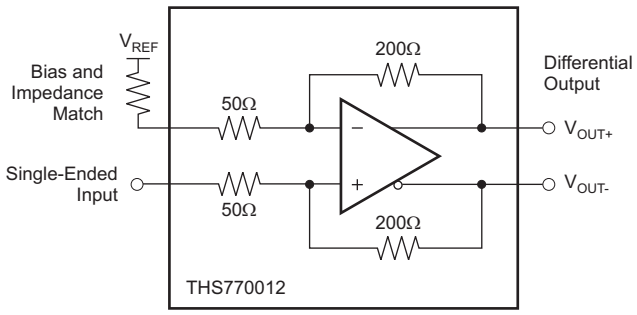

Figure 39. Single-Ended Input to Differential Output Amplifier

Setting the Gain

Gain is adjustable by placing external components in positions R11, R12, R13, and R14 on the EVM. Table 2 below shows the component values for setting gain from +10dB to +13.7dB. The different configurations and values change the effective value of the internal feedback, where the gain is determined by the resultant effective R_F/R_G, where R_G = 50Ω

Table 2. Gain Settings

GAIN	R11, R12	R13, R14	EFFECTIVE R_F
+10dB	Open	140 Ω	140 || 340 + 60 = 159 Ω
+11dB	Open	523 Ω	140 || 723 + 60 = 177 Ω
+12dB	Open	Open	140 + 60 = 200 Ω
+13.7dB (AC gain), +12dB (DC gain)(1)	0.1 µF capacitors	Open	$\frac{(140 \,\|\|\, 200 + 60) \times (140 + 200)}{200} = 242\ \Omega$

(1) Using 0.1 µF capacitors for R11 and R12 limits the low frequency response to the default value of +12dB at frequency below about 10kHz. For +13.7dB gain at DC, connect pins 13 and 18 of the device to a low impedance voltage source equal to V_{OCM} (+2.5V nominal).

Setting the Output Common-Mode Voltage

The V_{OCM} input controls the output common-mode voltage. V_{OCM} has no internal biasing network and must be driven by an external source or resistor divider network to the positive power supply. In ac-coupled applications, the V_{OCM} input impedance and bias current are not critical, but in dc-coupled applications where more accuracy is desired, the input bias current of the pin should be considered. For best harmonic distortion with V_{OUT} = $3V_{PP}$, the V_{OCM} input should be maintained within the operating range of 2.25V to 2.75V. The V_{OCM} input voltage can be operated outside this range if lower output swing is used or distortion degradation is allowed, and increased bias current into the pin is acceptable. For more information, see Figure 18 and Figure 34. It is recommended to use a 0.1µF decoupling capacitor from the V_{OCM} pin to ground to prevent noise and other spurious signals from coupling into the common-mode loop of the amplifier.

Input Common-Mode Voltage Range

The THS770012 is designed primarily for ac-coupled operation. With input dc blocking, the input common-mode voltage of the device is driven to the same voltage as V_{OCM} by the outputs. Therefore, as long as the V_{OCM} input is maintained within the operating range of 2.25V to 2.75V, the input common-mode of the main amplifier is also maintained within its linear operating range of 2.25V to 2.75V. If the device is used with dc coupled input, the driving source needs to bias the input to its linear operating range of 2.25V to 2.75V for proper operation.

Operation with Split Supply ±2.5V

The THS770012 can be operated using a split ±2.5V supply. In this case, V_{S+} is connected to +2.5V, and GND (and any other pin noted to be connected to GND) is connected to -2.5V. As with any device, the THS770012 is impervious to what the user decides to name the levels in the system. In essence, it is simply a level shift of the power pins by –2.5V. If everything else is level-shifted by the same amount, the device sees no difference. With a ±2.5V power supply, the V_{OCM} range is 0V ±0.25V; therefore, power-down levels are –2.5V = on and +2.5V = off, and input and output voltage ranges are symmetrical about 0V. This design has certain advantages in systems where signals are referenced to ground, and as noted in the following section, for driving ADCs with low input common-mode voltage requirements in dc-coupled applications.

Driving Capcitive Loads

The THS770012 is tested as described previously, with the data shown in the typical graphs. Due to the internal gain resistor architecture used on the device, the only practical means to avoid stability problems such as overshoot/ringing, gain peaking, and oscillation when driving capacitive loads is to place small resistors in series with the outputs (R_O) to isolate the phase shift caused by the capacitive load from the feedback loop of the amplifier. Note there are 2Ω internal resistors in series with each output to help maintain stability. The Typical Characteristics graphs show recommended values for an optimally flat frequency response with maximum bandwidth. Smaller values of R_O can be used if more peaking is allowed, and larger values can be used to - reduce the bandwidth.

Driving ADCs

The THS770012 is designed and optimized for the highest performance to drive differential input ADCs. Figure 40 shows a generic block diagram of the THS770012 driving an ADC. The primary interface circuit between the amplifier and the ADC is usually a filter of some type for antialias purposes, and provides a means to bias the signal to the input common-mode voltage required by the ADC. Filters range from single-order real RC poles to higher-order LC filters, depending on the requirements of the application. Output resistors (R_O) are shown on the amplifier outputs to isolate the amplifier from any capacitive loading presented by the filter.

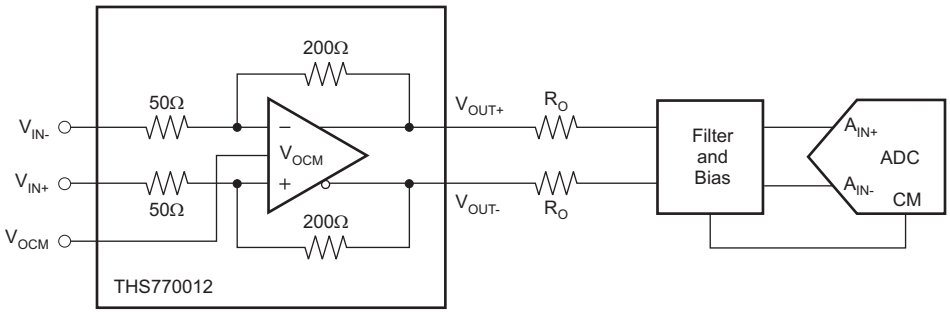

Figure 40. Generic ADC Driver Block Diagram

The key points to consider for implementation are described in the following three subsections.

SNR Considerations

The signal-to-noise ratio (SNR) of the amplifier + filter + ADC adds in RMS fashion. Noise from the amplifier is bandwidth-limited by the filter. Depending on the amplitude of the signal and the bandwidth of the filter, the SNR of the amplifier + filter can be calculated. To get the combined SNR, this value is then squared, added to the square of the ADC SNR, and the square-root is taken. If the SNR of the amplifier + filter equals the SNR of the ADC, the combined SNR is 3dB higher and for minimal inpact on the ADC's SNR the SNR of the amplifier + filter should be 10dB or more lower. The combined SNR calculated in this manner is usually accurate to within ±1dB of actual implementation.

SFDR Considerations

Theoretically, the spurious-free dynamic range (SFDR) of the amplifier + filter + ADC adds linearly on a spur-by-spur basis. The amplifier output spurs are linearly related solely to the input signal and the SFDR is usually set by second-order or third-order harmonic distortion for single-tone inputs, and by second-order or third-order intermodulation distortion for two-tone inputs. Harmonic and second-order intermodulation distortion can be filtered to some degree by the antialias filter, but not third-order intermodulation distortion. Generally, the ADC also has the same distortion products, but as a result of the sampling nature and potential for clock feedthrough, there may be spurs not linearly related solely to the input signal. When the spurs from the amplifier + filter are known, each can be directly added to the same spur from the ADC. This is a worst-case analysis based on the assumption the spurs sources are in phase. If the spur of the amplifier + filter equals the spur of the ADC, the combined spur is 6dB higher. The combined spur calculated in this manner is usually accurate to within ±6dB of actual implementation, but higher variations have been observed especially in second-order performance as a result of phase shift in the filter.

Common-mode phase shift introduced by the filter nullifies the basic assumption that the spur sources are in phase. This phase shift can lead to better performance than predicted as the spurs become phase shifted, and there is the potential for cancellation as the phase shift reaches 180°.

Differential phase and magnitude imbalance in the filter as a result of mismatched components caused by nominal tolerance can severely degrade the second-order distortion of the ADC. Single-order RC filters cause very little differential phase shift with nominal tolerances of 5% or less, but higher-order LC filters are very sensitive to component mismatch. For instance, a third-order Butterworth bandpass filter with 100MHz center frequency and 20MHz bandwidth shows up to 20° differential phase imbalance in a Spice Monte Carlo analysis with 2% component tolerances. Therefore, while a prototype may work, production variance is unacceptable. Low tolerance 1% components and low order filter is recommended for best performance. Otherwise a transformer or balun is recommended at the ADC input to restore the phase balance in the input signal to the ADC.

ADC Input Common-Mode Voltage Considerations

The input common-mode voltage range of the ADC must be observed for proper operation. In an ac-coupled application between the amplifier and the ADC, the input common-mode voltage bias of the ADC is accomplished in different ways depending on the ADC. Some use internal bias networks and others use external components, such as resistors, from each input to the CM output of the ADC. When ac coupling, the output common-mode voltage of the amplifier is a *don't care* for the ADC, and V_{OCM} should be set for optimum performance of the amplifier.

DC-coupled applications vary in complexity and requirements, depending on the ADC. Devices such as the ADS5424 require a nominal 2.4V input common-mode, while others such as the ADS5485 require a nominal 3.1V input common-mode, and still others like the ADS6149 require 1.5V and the ADS4149 require 0.95V. Given the THS770012 output common-mode range, ADCs with input common-mode closer to 2.5V are easier to dc-couple to, and require little or no level shifting. For applications that require a different common-mode voltage between the amplifier and the ADC, a resistor network can be used, as shown in Figure 41. With ADCs that have internal resistors (R_{INT}) that bias the ADC input to V_{CM}, the bias resistors do not affect the desired value of R_P, but do cause more attenuation of the differential input signal. Knowing the differential input resistance is required and sometimes, that is all that is provided.

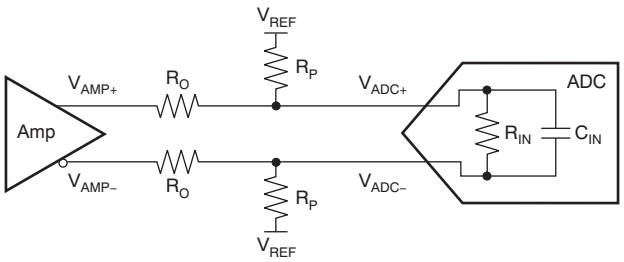

Figure 41. Resistor Network to DC Level Shift Common-Mode Voltage

For common-mode analysis, assume that $V_{AMP±} = V_{OCM}$ and $V_{ADC±} = V_{ADC}$ (the specification for the ADC input common-mode voltage). V_{REF} is chosen to be a voltage within the system (such as the ADC or amplifier analog supply) or ground, depending on whether the voltage must be pulled up or down, and R_O is chosen to be a reasonable value, such as 49.9Ω. With these known values, R_P can be found by using Equation 1:

$$R_P = R_O \left(\frac{V_{ADC} - V_{REF}}{V_{AMP} - V_{ADC}} \right) \quad (1)$$

The insertion of this resistor network also attenuates the amplifier output signal. The gain (or loss) can be calculated by Equation 2:

$$GAIN = \left(\frac{2R_P \parallel Z_{IN}}{2R_O + 2R_P \parallel Z_{IN}} \right) \quad (2)$$

Using the gain and knowing the full-scale input of the ADC, $V_{ADC\ FS}$, the required amplitude to drive the ADC with the network can be calculated using Equation 3:

$$V_{AMP\ PP} = \frac{V_{ADC\ FS}}{GAIN} \quad (3)$$

Using the ADC examples given previously, Table 3 shows sample calculations of the value of R_P and $V_{AMP\ FS}$ for full-scale drive, and then for –1dB (often times, the ADC drive is backed off from full-scale in applications, so lower amplitudes may be acceptable). All voltages are in volts, resistors in Ω (the nearest standard value should be used), and gain as noted. Table 3 does not include the ADS5424 because no level shift is required with this device.

Table 3. Example R_P for Various ADCs

ADC	V_{OCM} (V_{DC})	V_{ADC} (V_{DC})	V_{REF} (V_{DC})	R_{INT} (Ω)	R_O (Ω)	R_P (Ω)	GAIN (V/V)	GAIN (dB)	$V_{ADC\ FS}$ (V_{PP})	$V_{AMP\ PP}$ FS (V_{PP})	$V_{AMP\ PP}$ –1dBFS (V_{PP})
ADS5485	2.5	3.1	5	1k	50	158.3	0.73	–2.71	2	4.10	3.65
ADS6149	2.5	1.5	0	NA	50	75.0	0.60	–4.44	2	3.33	2.97
ADS4149	2.5	0.95	0	NA	50	30.6	0.38	–8.40	2	5.26	4.69
ADS4149	0 (1)	0.95	2.5	NA	50	81.6	0.62	–4.15	2	3.23	2.88

(1) THS770012 with ±2.5V supply.

The calculated values for the ADS5485 give the lowest attenuation, and because of the high V_{FS}, it requires $3.65V_{PP}$ from the amplifier to drive to –1dBFS. Performance of the THS770012 is still very good up to 130MHz at this level, but the designer may want to further back off from full-scale for best performance and consider trading reduced SNR performance for better SFDR performance.

The values calculated for the ADS6149 show reasonable design targets and should work with good performance. Note the ADS6149 does not have buffered inputs, and the inputs have equivalent resistive impedance that varies with sampling frequency. In order to account for the increased loss, half of this resistance should be used for the value of R_{INT} in Equation 2.

The values calculated for the low input common-mode of the ADS4149 result in large attenuation of the amplifier signal leading to $5.26V_{PP}$ being required for full-scale ADC drive. This amplitude is greater than the maximum capability of the device. With a single +5V supply, the THS770012 is not suitable to drive this ADC in dc-coupled applications unless the ADC input is backed off towards –6dBFS. Another option is to operate the THS770012 with a split ±2.5V supply, and is shown in the last row of Table 3. For this situation, if the +2.5V is used as the pull-up voltage, only $2.88V_{PP}$ is required for the –1dBFS input to the ADS4149. See the *Operation with Split Supply ±2.5V* section for more detail. Note that the ADS4149 does not have buffered inputs and the inputs have equivalent resistive impedance that varies with sampling frequency. In order to account for the increased loss, half of this resistance should be used for the value of R_{INT} in Equation 2.

As with any design, testing is recommended to validate whether it meets the specific design goals.

APPLICATION INFORMATION

THS770012 DRIVING 16-BIT ADC

To illustrate the performance of the THS770012 as an ADC driver, the device is tested with a 16-bit ADC.

For testing purposes, a 30MHz, second-order Butterworth bandpass filter with center frequency at 100MHz is designed. The design target for the source impedance is 40Ω differential, and for load impedance is 400Ω differential. Therefore, approximately 1dB insertion loss is expected in the pass-band, requiring the amplifier output amplitude to be $2.5V_{PP}$ to drive the ADC to –1dBFS.

The output noise voltage specification for the THS770012 is 6 nV/√Hz. With $2.5V_{PP}$ amplifier output voltage swing and 30MHz bandwidth, the expected SNR from the amplifier + antialias filter is 88.5dBc. When added in combination with the 16-bit ADC, the expected total SNR is 75.2dBFS for the typical case.

Figure 42 shows the resulting FFT plot when driving the ADC to –1dBFS with a single-tone 95MHz sine wave, and sampling at 130MSPS. Test results show 100dBc SFDR from the forth-order harmonic and 74.4 dBFS SNR; analysis of the plot is shown in Table 4 versus typical ADC specifications. The test results from circuit board to circuit board shows over 10dB of variation in the second order harmonic due to component tolerance. Using lower 1% tolerance components or adding a balun between the filter and ADC inputs resulted in less variation and the typical expected results should be better than 95dBc SFDR and 74dB SNR.

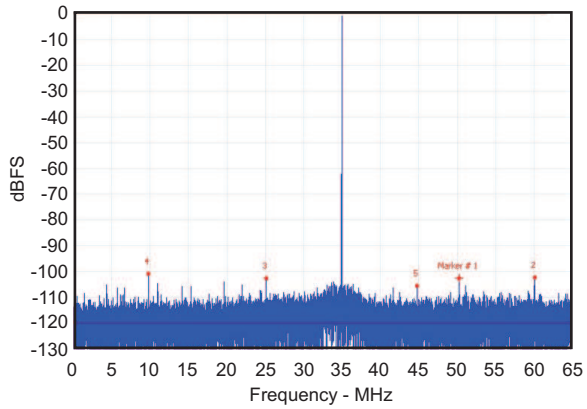

Figure 42. FFT Plot of THS770012 + 30MHz BPF + 16-Bit ADC with 95MHz Single-Tone Input Sampling at 130MSPS

Table 4. Analysis of FFT for THS770012 + BPF + 16-Bit ADC at 95MHz vs Typical ADC Specifications

CONFIGURATION	ADC INPUT	SNR	HD2	HD3
THS770012 + BPF + 16Bit ADC	–1dBFS	74.4dBFS	–101dBc	–101dBc
16-Bit ADC Only (typ)	–1dBFS	75.2dBFS	–100dBc	–100dBc

EVM AND LAYOUT RECOMMENDATIONS

Figure 37 is the THS770012RGE EVM schematic, and Figure 43 through Figure 46 show the layout details of the EVM PCB. Table 5 is the bill of materials for the EVM as supplied from TI. It is recommended to follow the layout of the external components as close as possible to the amplifier, ground plane construction, and power routing. General layout guidelines are:

1. Place a 2.2µF to 10µF capacitor on each supply pin within 2 inches from the device. It can be shared among other op amps.
2. Place a 0.01µF to 0.1µF capacitor on each supply pin to ground as close as possible to the device. Placement within 1mm of the device supply pins ensures best performance.
3. Keep output traces as short as possible to minimize parasitic capacitance and inductance. Doing so reduces unwanted characteristics such as peaking in the frequency response, overshoot, and ringing in the pulse response, and results in a more stable design.
4. To reduce parasitic capacitance, ground plane and power-supply planes should be removed from device output pins.
5. The V_{OCM} pin must be biased to a voltage between 2.25V to 2.75V for proper operation. Place a 0.1µF to 0.22µF capacitor to ground as close as possible to the device to prevent noise coupling into the common-mode.
6. For best performance, drive circuits and loads should be balanced and biased to keep the input and output common-mode voltage between 2.25V to 2.75V. AC-coupling is a simple way to achieve this performance.
7. The THS770012 is provided in a thermally enhanced PowerPAD™ package. The package is constructed using a downset leadframe on which the die is mounted. This arrangement results in low thermal resistance to the thermal pad on the underside of the package. Excellent thermal performance can be achieved by following the guidelines in TI application reports SLMA002, PowerPAD™ Thermally-Enhanced Package and SLMA004, PowerPAD™ Made Easy. For proper operation, the thermal pad on the bottom of the device must be tied to the same voltage potential as the GND pin on the device.

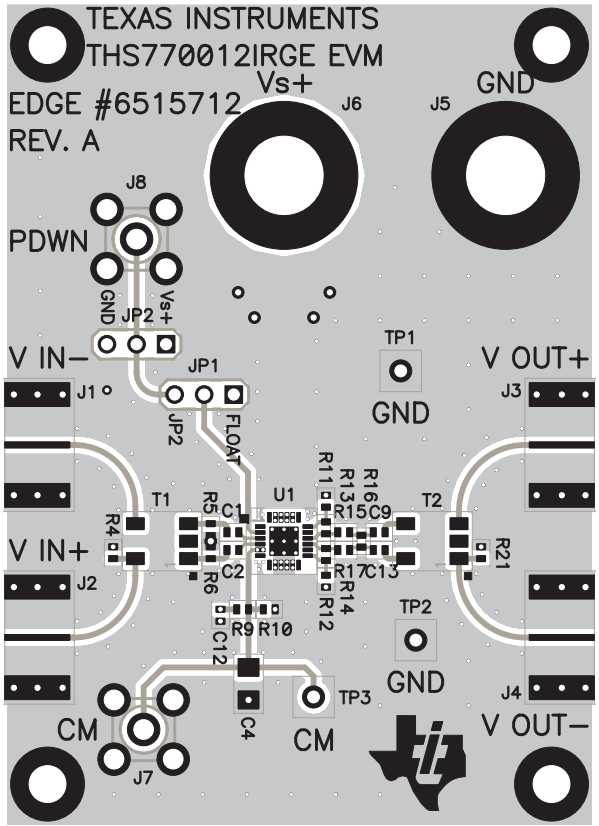

Figure 43. EVM Layout: Top Layer

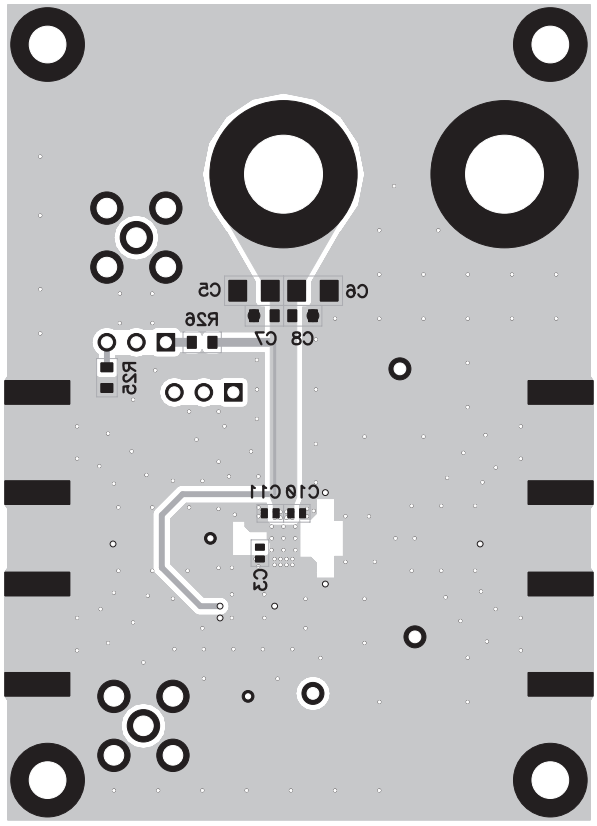

Figure 44. EVM Layout: Bottom Layer

Figure 45. EVM Layout: Layer 2

Figure 46. EVM Layout: Layer 3

Table 5. THS770012RGE EVM Bill of Materials

ITEM	DESCRIPTION	SMD SIZE	REFERENCE DESIGNATOR	QTY	MANUFACTURER PART NUMBER	DISTRIBUTOR PART NUMBER
1	CAP, 10.0uF, CERAMIC, X7R, 10V	1206	C4, C5, C6	3	(TDK) C3216X7R1A106K	(DIGI-KEY) 445-4043-1-ND
2	CAP, 0.1uF, CERAMIC, X7R, 16V	0603	C7, C8	2	(AVX) 0603YC104KAT2A	(DIGI-KEY) 478-1239-1-ND
3	CAP, 0.01uF, CERAMIC, X7R, 16V	0402	C10, C11	2	(AVX) 0402YC103KAT2A	(DIGI-KEY) 478-1114-1-ND
4	CAP, 100pF, CERAMIC, NPO, 50V	0402	C12	1	(AVX) 04025A101KAT2A	(DIGI-KEY) 478-4979-1-ND
5	CAP, 1000pF, CERAMIC, X7R, 50V	0402	C1, C2, C3, C9, C13	5	(AVX) 04025C102KAT2A	(DIGI-KEY) 478-1101-1-ND
6	OPEN	0402	R11, R12, R13, R14	4		
7	RESISTOR, 0 OHM	0402	R4, R21	2	(PANASONIC) ERJ-2GE0R00X	(DIGI-KEY) P0.0JCT-ND
8	RESISTOR, 49.9 OHM, 1/10W, 1%	0402	R5, R6	2	(PANASONIC) ERJ-2RKF49R9X	(DIGI-KEY) P49.9LCT-ND
9	RESISTOR, 57.6 OHM, 1/10W, 1%	0402	R16	1	(PANASONIC) ERJ-2RKF57R6X	(DIGI-KEY) P57.6LCT-ND
10	RESISTOR, 187 OHM, 1/10W, 1%	0402	R15, R17	2	(PANASONIC) ERJ-2RKF1870X	(DIGI-KEY) P187LCT-ND
11	RESISTOR, 1K OHM, 1/10W, 1%	0402	R9, R10	2	(PANASONIC) ERJ-2RKF1001X	(DIGI-KEY) P1.00KLCT-ND
12	RESISTOR, 10K OHM, 1/10W, 1%	0603	R25, R26	2	(PANASONIC) ERJ-3EKF1002V	(DIGI-KEY) P10.0KHCT-ND
13	TRANSFORMER, BALUN		T1, T2	2	(PULSE) CX2156NL	(DIGI-KEY) 553-1499-ND
14	JACK, BANANA RECEPTANCE, 0.25" DIA. HOLE		J5, J6	3	(SPC) 15459	(NEWARK) 79K5034
15	CONNECTOR, SMA PCB JACK		J7, J8	2	(AMPHENOL) 901-144-8RFX	(NEWARK) 34C8151
16	CONNECTOR, EDGE, SMA PCB JACK		J1, J2, J3, J4	4	(JOHNSON) 142-0701-801	(NEWARK) 90F2624
17	HEADER, 0.1" CTRS, 0.025" SQ. PINS	3 POS.	JP1, JP2	2	(SULLINS) PBC36SAAN	(DIGI-KEY) S1011E-36-ND
18	SHUNTS		JP1, JP2	2	(SULLINS) SSC02SYAN	(DIGI-KEY) S9002-ND
19	TEST POINT, RED		TP3	1	(KEYSTONE) 5000	(DIGI-KEY) 5000K-ND
20	TEST POINT, BLACK		TP1, TP2	2	(KEYSTONE) 5001	(DIGI-KEY) 5001K-ND
21	IC, THS770012		U1	1	(TI) THS770012RGE	
22	STANDOFF, 4-40 HEX, 0.625" LENGTH			4	(KEYSTONE) 1808	(DIGI-KEY) 1808K-ND
23	SCREW, PHILLIPS, 4-40, .250"			4	PMSSS 440 0025 PH	(DIGI-KEY) H703-ND
24	BOARD, PRINTED CIRCUIT				(TI) EDGE# 6515711 REV.A	

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 0V to +5.5V and the output voltage range of 0V to +5.5V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +85°C. The EVM is designed to operate properly with certain components above +85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

REVISION HISTORY

Changes from Revision A (November 2010) to Revision B	Page
• Changed to Revision B, May 2011	1
• Deleted "using a.....have changes" from THS770012 Driving ADS5493 section last part of the first sentence	23
• Deleted paragraphs, Figure 39 and section title under the first bulleted lists of THS770012 Driving ADS5493 section. Also deleted the next section title and "and bulit on the EVM" in the sentence under the title.	23

Changes from Revision B (May 2011) to Revision C	Page
• Deleted all ADS5493 information	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
THS770012IRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS7700 12IRGE	Samples
THS770012IRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS7700 12IRGE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

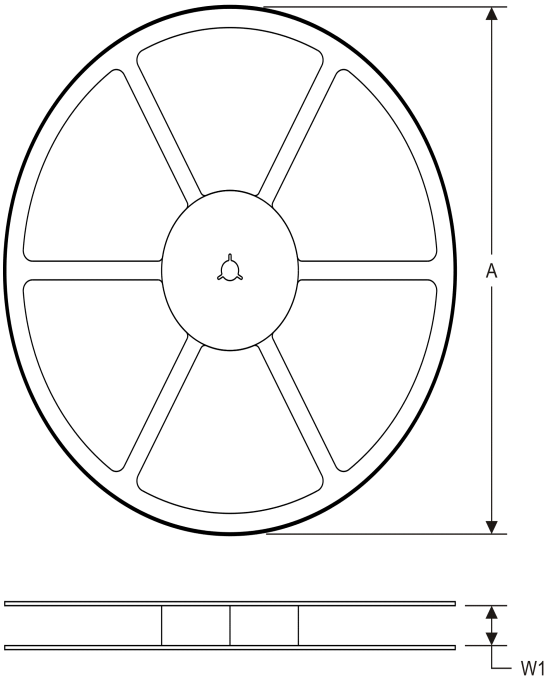
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

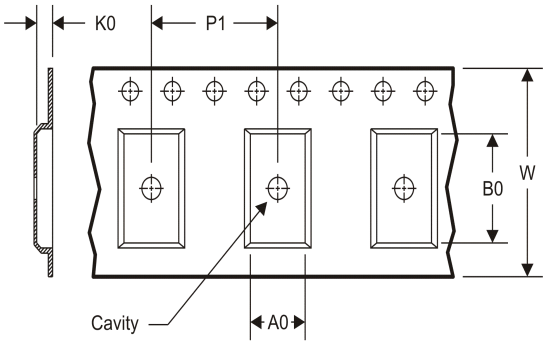
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



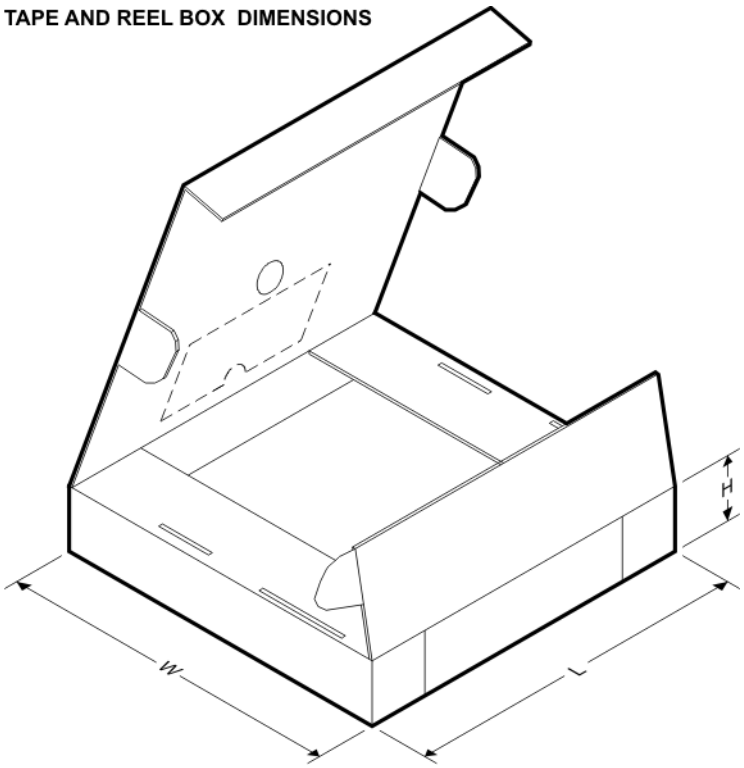
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS770012IRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
THS770012IRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

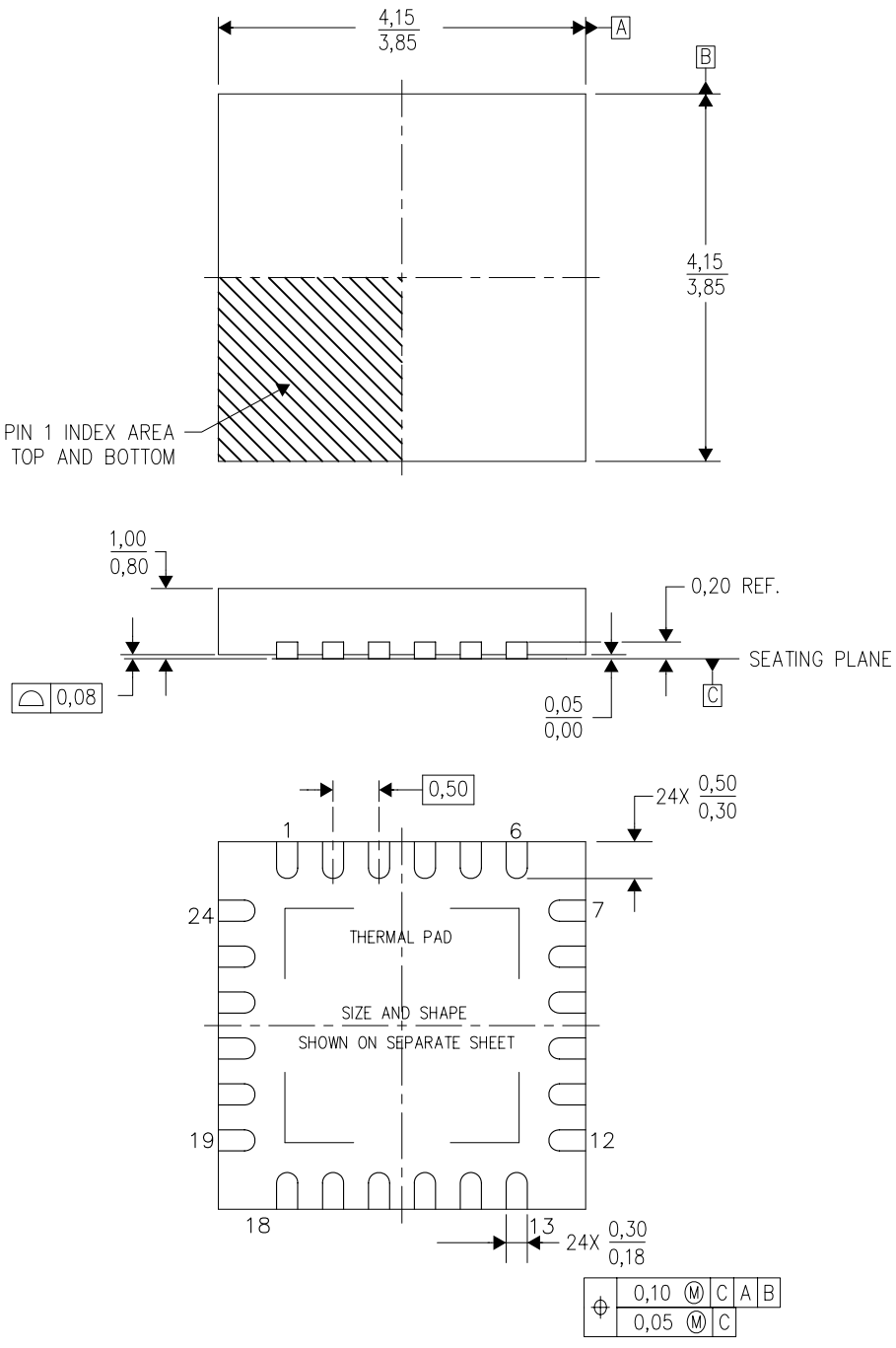
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS770012IRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
THS770012IRGET	VQFN	RGE	24	250	210.0	185.0	35.0

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

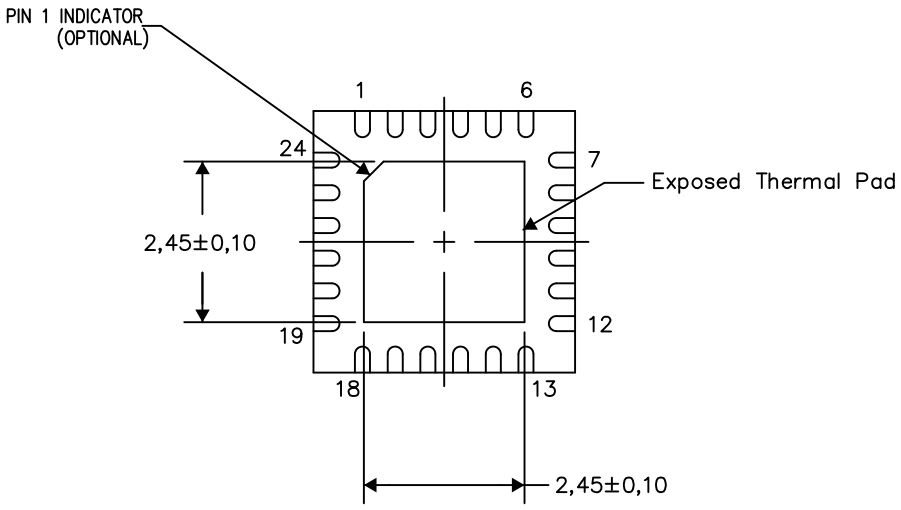
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



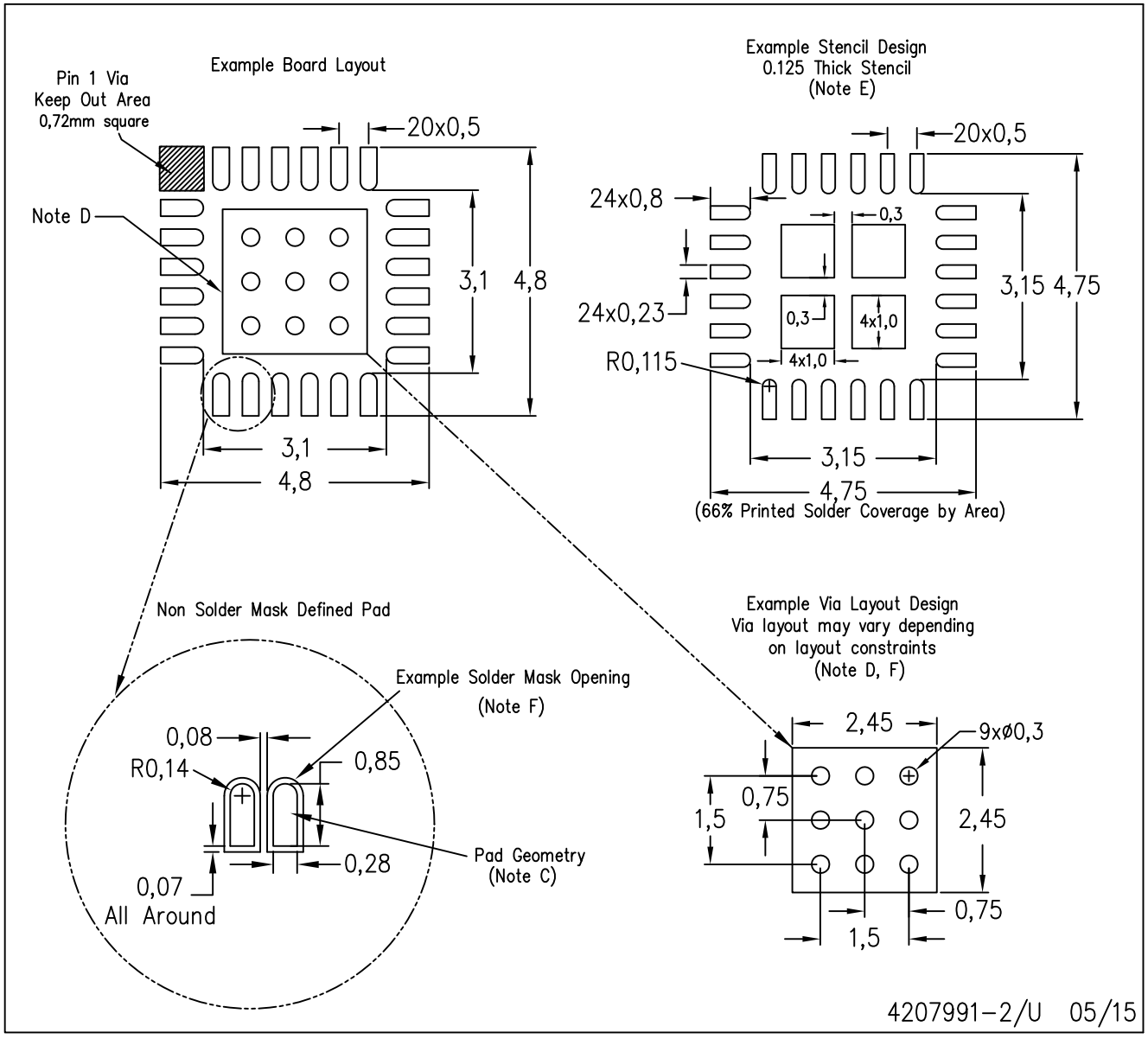
Bottom View

Exposed Thermal Pad Dimensions

4206344–3/AK 08/15

NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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