TLK10034 Quad-Channel XAUI/10GBASE-KR Transceiver

1 Device Overview

1.1 Features

- Quad-Channel Multi-Rate Transceiver
- Supports 10GBASE-KR, XAUI, and 1GBASE-KX Ethernet Standards
- Supports All CPRI and OBSAI Data Rates Up to 10 Gbps
- Supports Multi-Rate SERDES Operation with Up to 10.3125 Gbps Data Rate on the High Speed Side and Up to 5 Gbps on the Low Speed Side
- Differential CML I/Os on Both High Speed and Low Speed Sides
- Interface to Backplanes, Passive and Active Copper Cables, or SFP+ Optical Modules
- Selectable Reference Clock per Channel with Multiple Output Clock Options
- Loopback Capability on Both High Speed and Low Speed Sides
- Supports Data Retime Operation
- Supports PRBS, CRPAT, CJPAT, High-/Low-/Mixed-Frequency Patterns, and KR Pseudo-Random Pattern Generation and Verification, Square-Wave Generation
- Two Power Supplies: 1.0-V, and 1.5 or 1.8-V Nominal
- No Power Supply Sequencing Requirements
- Transmit De-emphasis and Receive Adaptive Equalization to Allow Extended Backplane/Cable Reach on Both High Speed and Low Speed Sides
- Programmable Transmit Output Swing on Both High Speed and Low Speed Sides
- Loss of Signal (LOS) Detection
- Supports 10G-KR Link Training, Forward Error Correction, Auto-Negotiation
- Jumbo Packet Support
- JTAG; IEEE 1149.1/1149.6 Test Interface
- Industry Standard MDIO Clause 45 and 22 Control Interfaces
- 65nm Advanced CMOS Technology
- Industrial Ambient Operating Temperature (–40°C to 85°C)
- Power Consumption: 825 mW per Channel (Nominal)
- Device Package: 19-mm x 19-mm, 324-Pin PBGA, 1-mm Ball-Pitch

1.2 Applications

- 10GBASE-KR Compliant Backplane Links
- 10 Gigabit Ethernet Switch, Router, and Network Interface Cards
- 10 Gigabit Ethernet Blade Servers
- Proprietary Cable/Backplane Links
- High-Speed Point- to-Point Transmission Systems

1.3 Description

The TLK10034 is a quad-channel multi-rate transceiver intended for use in high-speed bi-directional point-to-point data transmission systems. This device supports three primary modes. It can be used as a XAUI to 10GBASE-KR transceiver, as a general-purpose 8b/10b multi-rate 4:1, 2:1, or 1:1 serializer/deserializer, or can be used in 1G-KX mode.

While operating in the 10GBASE-KR mode, the TLK10034 performs serialization of the 8B/10B encoded XAUI data stream presented on its low speed (LS) side data inputs. The serialized 8B/10B encoded data is presented on the high speed (HS) side outputs in 64B/66B encoding format. Likewise, the TLK10034 performs deserialization of 64B/66B encoded data streams presented on its high speed side data inputs. The deserialized 64B/66B data is presented in 8B/10B format on the low speed side outputs. Link Training is supported in this mode as well as Forward Error Correction (FEC) for extended length applications.

While operating in the General Purpose SERDES mode, the TLK10034 performs 2:1 and 4:1 serialization of the 8B/10B encoded data streams presented on its low speed (LS) side data inputs. The serialized 8B/10B encoded data is presented on the high speed (HS) side outputs. Likewise, the TLK10034 performs 1:2 and 1:4 deserialization of 8B/10B encoded data streams presented on its high speed side data inputs. The deserialized 8B/10B encoded data is presented on the low speed side outputs. Depending on the serialization/deserialization ratio, the low speed side data rate can range from 0.5Gbps to 5Gbps and the high speed side data rate can range from 1Gbps to 10Gbps. 1:1 retime mode is also supported but limited to 1Gbps to 5Gbps rates.

The TLK10034 also supports 1G-KX (1.25Gbps) mode with PCS (CTC) capabilities. This mode can be enabled via software provisioning or via auto negotiation. If software provisioFCBGAning is used, data rates up to 3.125 Gbps are supported.

Both low speed and high speed side data inputs and outputs are of differential current mode logic (CML) type with integrated termination resistors.

The TLK10034 provides flexible clocking schemes to support various operations. They include the support for clocking with an externally-jitter-cleaned clock recovered from the high speed side. The device is also capable of performing clock tolerance compensation (CTC) in 10GBASE-KR and 1G-KX modes, allowing for asynchronous clocking.

The TLK10034 provides low speed side and high speed side loopback modes for self-test and system diagnostic purposes.

The TLK10034 has built-in pattern generators and verifiers to help in system tests. The device supports generation and verification of various PRBS, High, Low, Mixed, CRPAT long/short, CJPAT, and KR pseudo-random test patterns and square wave generation. The types of patterns supported on the low speed and high speed side are dependent on the operational mode chosen.

The TLK10034 has an integrated loss of signal (LOS) detection function on both high speed and low speed sides. LOS is asserted in conditions where the input differential voltage swing is less than the LOS assert threshold.

In the 10GBASE-KR mode, the lane alignment for each channel is achieved through the standard XAUI lane alignment scheme. In the General Purpose SERDES mode the low speed side lane alignment for each channel is achieved through a proprietary lane alignment scheme. The upstream link partner device needs to implement the lane alignment scheme for the correct link operation. Normal link operation resumes only after lane alignment is achieved.

The four TLK10034 channels are fully independent. They can be operated with different reference clocks, at different data rates, and with different serialization/deserialization ratios.

The low speed side of the TLK10034 is ideal for interfacing with an FPGA or ASIC capable of handling lower-rate serial data streams. The high speed side is ideal for interfacing with remote systems through optical fibers, electrical cables, or backplane interfaces. The TLK10034 supports operation with SFP and SFP+ optical modules, as well as 10GBASE-KR compatible backplane systems.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLK10034	FCBGA (324)	19.00 mm × 19.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

1.4 Functional Block Diagram

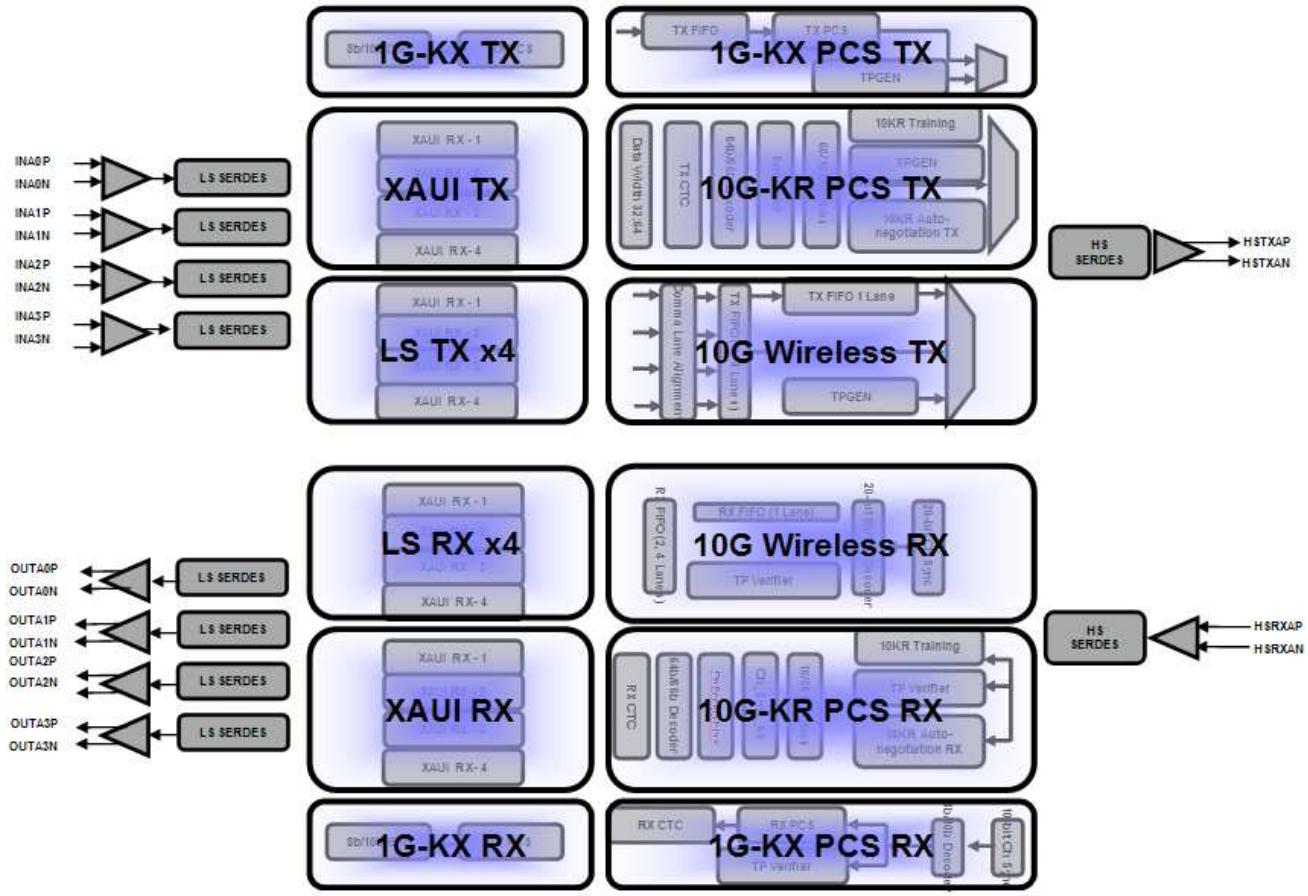

Figure 1-1. A Simplified One Channel Block Diagram of the TLK10034 Data Paths

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2012) to Revision A	Page
• Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

3 Pin Configuration and Functions

3.1 Pin Diagrams

A 19-mm x 19-mm, 324-pin PBGA package with a ball pitch of 1 mm is used. The device pin-out is as shown in Figure 3-1, Figure 3-2 and is described in detail in Table 3-1 and Table 3-2.

	1	2	3	4	5	6	7	8	9
A	VSS	INA0N	INA0P	VSS	HSRXAN	HSRXAP	VSS	HSTXAP	HSTXAN
B	INA1N	INA1P	VSS	VSS	VSS	VDDRA_HS	VSS	AMUXA_HS	VSS
C	VSS	VSS	OUTA0P	VSS	HSTX0_CLKOUTN	HSTX0_CLKOUTP	VSS	TESTEN	LS0_CLKOUTP
D	INA2P	VSS	OUTA0N	OUTA1P	GPI0	LOSA	HSRXA_CLKOUTN	HSRXA_CLKOUTP	VSS
E	INA2N	AMUXA_LS	VSS	OUTA1N	PRBSEN	PDTRXA_N	REFCLK_SEL	VDDT0_HS	VSS
F	VSS	VSS	OUTA2P	VSS	MDIO	LS_OK_IN_A	VSS	RESET_N	VDDA0_HS
G	INA3P	VSS	OUTA2N	VDDRA_LS	MDC	PRBS_PASS	VDDO0	VSS	VSS
H	INA3N	VDDA0_LS	VDDA0_LS	OUTA3P	VSS	VSS	DVDD	VDDD	DVDD
J	VSS	OUTB0N	VSS	OUTA3N	VDDT0_LS	LS_OK_OUT_A	VSS	VDDD	DVDD
K	VSS	OUTB0P	OUTB1N	VDDRB_LS	VDDT0_LS	VSS	DVDD	VDDD	VSS
L	INB0P	VDDA0_LS	OUTB1P	VSS	VSS	VSS	DVDD	VDDD	DVDD
M	INB0N	VSS	VDDA0_LS	OUTB2N	PRTAD4	VSS	VDDO3	VSS	VDDD
N	VSS	VSS	VSS	OUTB2P	VSS	LS_OK_OUT_B	VPP	VSS	VDDA1_HS
P	INB1P	AMUXB_LS	OUTB3N	VSS	PDTRXB_N	LS_OK_IN_B	LOSB	VDDT1_HS	VSS
R	INB1N	VSS	OUTB3P	VSS	VSS	VSS	HSRXB_CLKOUTP	HSRXB_CLKOUTN	VSS
T	VSS	INB2P	VSS	REFCLK0N	REFCLK0P	VSS	VSS	VSS	HSTX1_CLKOUTN
U	INB3P	INB2N	VSS	VSS	VSS	VDDRB_HS	VSS	AMUXB_HS	VSS
V	INB3N	VSS	VSS	HSTXBN	HSTXBP	VSS	HSRXBP	HSRXBN	VSS

Figure 3-1. The Pin-Out of the TLK10034 in a 19-mm x 19-mm 324-pin PBGA Package (1 of 2)

	10	11	12	13	14	15	16	17	18
A	VSS	HSRXCN	HSRXCP	VSS	HSTXCP	HSTXCN	VSS	VSS	INC0N
B	AMUXC_HS	VSS	VDDRC_HS	VSS	VSS	VSS	VSS	INC1N	INC0P
C	LS0_CLKOUTN	VSS	VSS	VSS	REFCLK1N	REFCLK1P	VSS	INC1P	VSS
D	VSS	HSRXC_CLKOUTN	HSRXC_CLKOUTP	PDTRXC_N	LOSC	VSS	OUTC0P	VSS	INC2N
E	VDDA0_HS	VSS	TDI	TCK	TMS	VSS	OUTC0N	AMUXC_LS	INC2P
F	VSS	VDDA0_HS	LS_OK_IN_C	LS_OK_OUT_C	PRTAD1	OUTC1P	VSS	VSS	VSS
G	VDDD	VSS	VDDO1	VSS	TDO	OUTC1N	VDDA1_LS	VSS	INC3N
H	DVDD	VDDD	DVDD	TRST_N	VSS	VSS	OUTC2P	VDDA1_LS	INC3P
J	VSS	VDDD	DVDD	VSS	VDDT1_LS	VDDRC_LS	OUTC2N	OUTC3P	VSS
K	DVDD	VDDD	VSS	LS_OK_IN_D	VDDT1_LS	OUTD0N	VSS	OUTC3N	VSS
L	DVDD	VDDD	DVDD	VSS	VSS	OUTD0P	VDDA1_LS	VDDA1_LS	IND0N
M	VSS	VSS	VDDO2	VSS	GPI2	VDDRD_LS	OUTD1N	VSS	IND0P
N	VSS	VDDA1_HS	PRTAD0	LS_OK_OUT_D	PRTAD3	VSS	OUTD1P	VSS	VSS
P	VDDA1_HS	MODE_SEL	PRTAD2	PDTRXD_N	GPI1	OUTD2N	VSS	AMUXD_LS	IND1N
R	VSS	HSRXD_CLKOUTP	HSRXD_CLKOUTN	LOSD	VSS	OUTD2P	OUTD3N	VSS	IND1P
T	HSTX1_CLKOUTP	VSS	ST	LS1_CLKOUTP	LS1_CLKOUTN	VSS	OUTD3P	VSS	VSS
U	AMUXD_HS	VSS	VDDRD_HS	VSS	VSS	VSS	VSS	IND2P	IND2N
V	HSTXDN	HSTXDP	VSS	HSRXDP	HSRXDN	VSS	IND3P	IND3N	VSS

Figure 3-2. The Pin-Out of the TLK10034 in a 19-mm x 19-mm 324-pin PBGA Package (2 of 2)

3.2 Pin Attributes

The details of the terminal functions of the TLK10034 are provided in Table 3-1 and Table 3-2.

Table 3-1. Pin Functions - Signal Pins

PIN		DIRECTION TYPE SUPPLY	DESCRIPTION
SIGNAL	BGA		
CHANNEL A			
HSTXAP HSTXAN	A8 A9	Output CML VDDA_HS	**High Speed Transmit Channel A Output.** HSTXAP and HSTXAN comprise the high speed side transmit direction Channel A differential serial output signal. During device reset (RESET_N asserted low) these pins are driven differential zero. These CML outputs must be AC coupled.
HSRXAP HSRXAN	A6 A5	Input CML VDDA_HS	**High Speed Receive Channel A Input.** HSRXAP and HSRXAN comprise the high speed side receive direction Channel A differential serial input signal. These CML input signals must be AC coupled.
INA[3:0]P/N	G1/H1 D1/E1 B2/B1 A3/A2	Input CML VDDA_LS	**Low Speed Channel A Inputs.** INAP and INAN comprise the low speed side transmit direction Channel A differential input signals. These signals must be AC coupled.
OUTA[3:0]P/N	H4/J4 F3/G3 D4/E4 C3/D3	Output CML VDDA_LS	**Low Speed Channel A Outputs.** OUTAP and OUTAN comprise the low speed side receive direction Channel A differential output signals. During device reset (RESET_N asserted low) these pins are driven differential zero. These signals must be AC coupled.
LOSA	D6	Output LVCMOS 1.5V/1.8V VDDO0 40Ω Driver	C**hannel A Receive Loss Of Signal (LOS) Indicator.** LOSA=0: Signal detected. LOSA=1: Loss of signal. Loss of signal detection is based on the input signal level. When HSRXAP/N has a differential input signal swing of ≤65 mV_{pp}, LOSA will be asserted (if enabled). If the input signal is greater than 175 mV_{p-p}, LOS will be deasserted. Outside of these ranges, the LOS indication is undefined. Other functions can be observed on LOSA real-time, configured via MDIO During device reset (RESET_N asserted low) this pin is driven low. During pin based power down (PDTRXA_N asserted low), this pin is floating. During register based power down (30.1.15 asserted high), this pin is floating. It is highly recommended that LOSA be brought to an easily accessible point on the application board (header) in the event that debug is required.
LS_OK_IN_A	F6	Input LVCMOS 1.5V/1.8V VDDO0	**Channel A Receive Lane Alignment Status Indicator.** Lane alignment status signal received from a Lane Alignment Slave on the link partner device. Valid in 10G General Purpose Serdes Mode. LS_OK_IN_A=0: Channel A link partner receive lanes not aligned. LS_OK_IN_A=1: Channel A link partner receive lanes aligned
LS_OK_OUT_A	J6	Output LVCMOS 1.5V/1.8V VDDO0 40Ω Driver	**Channel A Transmit Lane Alignment Status Indicator.** Lane alignment status signal sent to a Lane Alignment Master on the link partner device. Valid in 10G General Purpose Serdes Mode. LS_OK_OUT_A=0: Channel A link partner transmit lanes not aligned. LS_OK_OUT_A=1: Channel A link partner transmit lanes aligned.
PDTRXA_N	E6	Input LVCMOS 1.5V/1.8V VDDO0	**Transceiver Power Down.** When this pin is held low (asserted), Channel A is placed in power down mode. When deasserted, Channel A operates normally. After deassertion, a software data path reset should be issued through the MDIO interface.
CHANNEL B			
HSTXBP HSTXBN	V5 V4	Output CML VDDA_HS	**High Speed Transmit Channel B Output.** HSTXBP and HSTXBN comprise the high speed side transmit direction Channel B differential serial output signal. During device reset (RESET_N asserted low) these pins are driven differential zero. These CML outputs must be AC coupled.
HSRXBP HSRXBN	V7 V8	Input CML VDDA_HS	**High Speed Receive Channel B Input.** HSRXBP and HSRXBN comprise the high speed side receive direction Channel B differential serial input signal. These CML input signals must be AC coupled.
INB[3:0]P/N	U1/V1 T2/U2 P1/R1 L1/M1	Input CML VDDA_LS	**Low Speed Channel B Inputs.** INBP and INBN comprise the low speed side transmit direction Channel B differential input signals. These signals must be AC coupled.
OUTB[3:0]P/N	R3/P3 N4/M4 L3/K3 K2/J2	Output CML VDDA_LS	**Low Speed Channel B Outputs.** OUTBP and OUTBN comprise the low speed side receive direction Channel B differential output signals. During device reset (RESET_N asserted low) these pins are driven differential zero. These signals must be AC coupled.

Table 3-1. Pin Functions - Signal Pins (continued)

PIN		DIRECTION TYPE SUPPLY	DESCRIPTION
SIGNAL	BGA		
LOSB	P7	Output LVCMOS 1.5V/1.8V VDDO3 40Ω Driver	**Channel B Receive Loss Of Signal (LOS) Indicator.** LOSB=0: Signal detected. LOSB=1: Loss of signal. Loss of signal detection is based on the input signal level. When HSRXBP/N has a differential input signal swing of ≤65 mV_{pp}, LOSB will be asserted (if enabled). If the input signal is greater than 175 mV_{p-p}, LOS will be deasserted. Outside of these ranges, the LOS indication is undefined. Other functions can be observed on LOSB real-time, configured via MDIO During device reset (RESET_N asserted low) this pin is driven low. During pin based power down (PDTRXB_N asserted low), this pin is floating. During register based power down (30.1.15 asserted high), this pin is floating. It is highly recommended that LOSB be brought to easily accessible point on the application board (header), in the event that debug is required.
LS_OK_IN_B	P6	Input LVCMOS 1.5V/1.8V VDDO3	**Channel B Receive Lane Alignment Status Indicator.** Lane alignment status signal received from a Lane Alignment Slave on the link partner device. Valid in 10G General Purpose Serdes Mode. LS_OK_IN_B=0: Channel B Receive lanes not aligned. LS_OK_IN_B=1: Channel B Receive lanes aligned
LS_OK_OUT_B	N6	Output LVCMOS 1.5V/1.8V VDDO3 40Ω Driver	**Channel B Transmit Lane Alignment Status Indicator.** Lane alignment status signal sent to a Lane Alignment Master on the link partner device. Valid in 10G General Purpose Serdes Mode. LS_OK_OUT_B=0: Channel B Transmit lanes not aligned. LS_OK_OUT_B=1: Channel B Transmit lanes aligned.
PDTRXB_N	P5	Input LVCMOS 1.5V/1.8V VDDO1	**Transceiver Power Down.** When this pin is held low (asserted), Channel B is placed in power down mode. When deasserted, Channel B operates normally. After deassertion, a software data path reset should be issued through the MDIO interface.
CHANNEL C			
HSTXCP HSTXCN	A14 A15	Output CML VDDA_HS	**High Speed Transmit Channel C Output.** HSTXCP and HSTXCN comprise the high speed side transmit direction Channel C differential serial output signal. During device reset (RESET_N asserted low) these pins are driven differential zero. These CML outputs must be AC coupled.
HSRXCP HSRXCN	A12 A11	Input CML VDDA_HS	**High Speed Receive Channel C Input.** HSRXCP and HSRXCN comprise the high speed side receive direction Channel C differential serial input signal. These CML input signals must be AC coupled.
INC[3:0]P/N	H18/G18 E18/D18 C17/B17 B18/A18	Input CML VDDA_LS	**Low Speed Channel C Inputs.** INCP and INCN comprise the low speed side transmit direction Channel C differential input signals. These signals must be AC coupled.
OUTC[3:0]P/N	J17/K17 H16/J16 F15/G15 D16/E16	Output CML VDDA_LS	**Low Speed Channel C Outputs.** OUTCP and OUTCN comprise the low speed side receive direction Channel C differential output signals. During device reset (RESET_N asserted low) these pins are driven differential zero. These signals must be AC coupled.
LOSC	D14	Output LVCMOS 1.5V/1.8V VDDO1 40Ω Driver	**Channel C Receive Loss Of Signal (LOS) Indicator.** LOSC=0: Signal detected. LOSC=1: Loss of signal. Loss of signal detection is based on the input signal level. When HSRXCP/N has a differential input signal swing of ≤65 mVpp, LOSC will be asserted (if enabled). If the input signal is greater than 175 mV_{p-p}, LOS will be deasserted. Outside of these ranges, the LOS indication is undefined. Other functions can be observed on LOSC real-time, configured via MDIO During device reset (RESET_N asserted low) this pin is driven low. During pin based power down (PDTRXC_N asserted low), this pin is floating. During register based power down (30.1.15 asserted high), this pin is floating. It is highly recommended that LOSC be brought to easily accessible point on the application board (header), in the event that debug is required.
LS_OK_IN_C	F12	Input LVCMOS 1.5V/1.8V VDDO1	**Channel C Receive Lane Alignment Status Indicator.** Lane alignment status signal received from a Lane Alignment Slave on the link partner device. Valid in 10G General Purpose Serdes Mode. LS_OK_IN_C=0: Channel C Receive lanes not aligned. LS_OK_IN_C=1: Channel C Receive lanes aligned
LS_OK_OUT_C	F13	Output LVCMOS 1.5V/1.8V VDDO1 40Ω Driver	**Channel C Transmit Lane Alignment Status Indicator.** Lane alignment status signal sent to a Lane Alignment Master on the link partner device. Valid in 10G General Purpose Serdes Mode. LS_OK_OUT_C=0: Channel C Transmit lanes not aligned. LS_OK_OUT_C=1: Channel C Transmit lanes aligned.

Table 3-1. Pin Functions - Signal Pins (continued)

PIN		DIRECTION TYPE SUPPLY	DESCRIPTION
SIGNAL	BGA		
PDTRXC_N	D13	Input LVCMOS 1.5V/1.8V VDDO1	**Transceiver Power Down.** When this pin is held low (asserted), Channel C is placed in power down mode. When deasserted, Channel C operates normally. After deassertion, a software data path reset should be issued through the MDIO interface.
CHANNEL D			
HSTXDP HSTXDN	V11 V10	Output CML VDDA_HS	**High Speed Transmit Channel D Output.** HSTXDP and HSTXDN comprise the high speed side transmit direction Channel D differential serial output signal. During device reset (RESET_N asserted low) these pins are driven differential zero. These CML outputs must be AC coupled.
HSRXDP HSRXDN	V13 V14	Input CML VDDA_HS	**High Speed Receive Channel D Input.** HSRXDP and HSRXDN comprise the high speed side receive direction Channel D differential serial input signal. These CML input signals must be AC coupled.
IND[3:0]P/N	V16/V17 U17/U18 R18/P18 M18/L18	Input CML VDDA_LS	**Low Speed Channel D Inputs.** INDP and INDN comprise the low speed side transmit direction Channel D differential input signals. These signals must be AC coupled.
OUTD[3:0]P/N	T16/R16 R15/P15 N16/M16 L15/K15	Output CML VDDA_LS	**Low Speed Channel D Outputs.** OUTDP and OUTDN comprise the low speed side receive direction Channel D differential output signals. During device reset (RESET_N asserted low) these pins are driven differential zero. These signals must be AC coupled.
LOSD	R13	Output LVCMOS 1.5V/1.8V VDDO2 40Ω Driver	**Channel D Receive Loss Of Signal (LOS) Indicator.** LOSD=0: Signal detected. LOSD=1: Loss of signal. Loss of signal detection is based on the input signal level. When HSRXDP/N has a differential input signal swing of ≤65 mVpp, LOSD will be asserted (if enabled). If the input signal is greater than 175 mV_{p-p}, LOS will be deasserted. Outside of these ranges, the LOS indication is undefined. Other functions can be observed on LOSD real-time, configured via MDIO. During device reset (RESET_N asserted low) this pin is driven low. During pin based power down (PDTRXD_N asserted low), this pin is floating. During register based power down (30.1.15 asserted high), this pin is floating. It is highly recommended that LOSD be brought to easily accessible point on the application board (header), in the event that debug is required.
LS_OK_IN_D	K13	Input LVCMOS 1.5V/1.8V VDDO2	**Channel D Receive Lane Alignment Status Indicator.** Lane alignment status signal received from a Lane Alignment Slave on the link partner device. LS_OK_IN_D=0: Channel D Receive lanes not aligned. LS_OK_IN_D=1: Channel D Receive lanes aligned
LS_OK_OUT_D	N13	Output LVCMOS 1.5V/1.8V VDDO2 40Ω Driver	**Channel D Transmit Lane Alignment Status Indicator.** Lane alignment status signal sent to a Lane Alignment Master on the link partner device. LS_OK_OUT_D=0: Channel D Transmit lanes not aligned. LS_OK_OUT_D=1: Channel D Transmit lanes aligned.
PDTRXD_N	P13	Input LVCMOS 1.5V/1.8V VDDO2	**Transceiver Power Down.** When this pin is held low (asserted), Channel D is placed in power down mode. When deasserted, Channel D operates normally. After deassertion, a software data path reset should be issued through the MDIO interface.
REFERENCE CLOCKS, OUTPUT CLOCKS, AND CONTROL AND MONITORING SIGNALS			
REFCLK0P/N	T5 T4	Input LVDS/ LVPECL DVDD	**Reference Clock Input Zero.** This differential input is a clock signal used as a reference to channels A, B, C, or D. The reference clock selection is done through MDIO or the REFCLK_SEL pin. This input signal **must** be AC coupled. If unused, REFCLK0P/N should be pulled down to GND through a shared 100 Ω resistor.
REFCLK1P/N	C15 C14	Input LVDS/ LVPECL DVDD	**Reference Clock Input One.** This differential input is a clock signal used as a reference to channels A, B, C, or D. The reference clock selection is done through MDIO or the REFCLK_SEL pin. This input signal **must** be AC coupled. If unused, REFCLK1P/N should be pulled down to GND through a shared 100 Ω resistor.
HSRXA_CLKOUTP/N HSRXB_CLKOUTP/N HSRXC_CLKOUTP/N HSRXD_CLKOUTP/N	D8/D7 R7/R8 D12/D11 R11/R12	Output CML DVDD	**High Speed Side Recovered Byte Output Clock.** By default, these outputs are disabled. When enabled they output the high speed side Channel A/B/C/D recovered byte clocks (high speed line rate divided by 16 or 20). Optionally they can be configured to output the VCO clock divided by 2. (Note: For full rates, VCO/2 pre divided clocks will be equivalent to the line rate divided by 8, for sub-rates, VCO/2 pre divided clocks will be equivalent to the line rate divided by 4) Additional MDIO-selectable divide ratios of 1, 2, 4, 5, 8, 10, 16, 20, and 25 are available. See Figure 5-35 for more information. These CML outputs must be AC coupled. During device reset (RESET_N asserted low), pin-based power down (PDTRXA_N, PDTRXB_N, PDTRXC_N, and PDTRXD_N asserted low), or register-based power down (30.1.15 asserted high per channel), these pins are floating.

Table 3-1. Pin Functions - Signal Pins (continued)

PIN		DIRECTION TYPE SUPPLY	DESCRIPTION
SIGNAL	BGA		
HSTX0_CLKOUTP/N HSTX1_CLKOUTP/N	C6/C5 T10/T9	Output CML DVDD	**High Speed Side Transmit Output Clock.** By default, these outputs are disabled. When enabled, they can be configured to output the high speed side transmit clock of any of the four channels. Additional MDIO-selectable divide ratios of 1, 2, 4, 5, 8, 10, 16, 20, and 25 are available. See Figure 5-35 for more information. These CML outputs must be AC coupled. During device reset (RESET_N asserted low), pin-based power down (PDTRXA_N, PDTRXB_N, PDTRXC_N, and PDTRXD_N asserted low), or register-based power down (30.1.15 asserted high on all channels), these pins are floating.
LS0_CLKOUTP/N LS1_CLKOUTP/N	C9/C10 T13/T14	Output CML DVDD	**Low Speed Side Output Clock.** By default, these outputs are disabled. When enabled, they can be configured to output the low speed side transmit byte clock or recovered byte clock (low speed line rate divided by 10) of any of the four channels. Additional MDIO-selectable divide ratios of 1, 2, 4, 5, 8, 10, 16, 20, and 25 are available. See Figure 5-35 for more information. These CML outputs must be AC coupled. During device reset (RESET_N asserted low), pin-based power down (PDTRXA_N, PDTRXB_N, PDTRXC_N, and PDTRXD_N asserted low), or register-based power down (30.1.15 asserted high on all channels), these pins are floating.
REFCLK_SEL	E7	Input LVCMOS 1.5V/1.8V VDDO0	**Reference Clock Select.** This input, when low, selects REFCLK0P/N as the reference clock to all the SERDES channels. When high, REFCLK1P/N is selected as the reference clock to all the SERDES channels. If software control is desired (register bit 30.1.1), this input signal should be tied low. With software control, the reference clock for each channel can be independently selected. See Figure 5-34 for more information. Default reference clock for all the channels is REFCLK0P/N.
PRBSEN	E5	Input LVCMOS 1.5V/1.8V VDDO0	**Enable PRBS:** When this pin is asserted high, the internal PRBS generator and verifier circuits are enabled on both transmit and receive data paths on high speed and low speed sides of all the channels. The PRBS 2^{31}-1 pattern is selected by default, and can be changed through MDIO. For more details, see the test mode descriptions for the various operating modes.
PRBS_PASS	G6	Output LVCMOS 1.5V/1.8V VDDO0 40Ω Driver	**Receive PRBS Error Free (Pass) Indicator.** When PRBS test is enabled (PRBSEN=1): PRBS_PASS=1 indicates that PRBS pattern reception is error free. PRBS_PASS=0 indicates that a PRBS error is detected. The channel, high speed or low speed side, and lane (for low speed side) that this signal refers to is chosen through MDIO. During device reset (RESET_N asserted low) this pin is driven high. During pin based power down (PDTRXA_N, PDTRXB_N, PDTRXC_N, and PDTRXD_N asserted low), this pin is floating. During register based power down, this pin is floating. It is highly recommended that PRBS_PASS be brought to easily accessible point on the application board (header), in the event that debug is required.
ST	T12	Input LVCMOS 1.5V/1.8V VDDO2	**MDIO Select**. Used to select Clause 22 (=1) or Clause 45 (=0) operation. Note that selecting clause 22 will impact mode availability. See MODE_SEL. A hard or soft reset must be applied after a change of state occurs on this input signal.
MODE_SEL	P11	Input LVCMOS 1.5V/1.8V VDDO2	**Device Operating Mode Select.** Used together with ST pin to select device operating mode. See Table 5-13 for details.
PRTAD[4:0]	M5 N14 P12 F14 N12	Input LVCMOS 1.5V/1.8V VDDO[3:1]	**MDIO Port Address.** Used to select the MDIO port address. PRTAD[4:2] selects the MDIO port address. Selecting a unique PRTAD[4:2] per TLK10034 device allows 8 TLK10034 devices per MDIO bus. Each channel can be accessed by setting the appropriate port address field within the serial interface protocol transaction. The TLK10034 will respond if the 3 MSB's of the port address field on MDIO protocol (PA[4:2]) matches PRTAD[4:2]. If PA[1:0] = 2'b00, TLK10034 Channel A will respond. If PA[1:0] = 2'b01, TLK10034 Channel B will respond. If PA[1:0] = 2'b10, TLK10034 Channel C will respond. If PA[1:0] = 2'b11, TLK10034 Channel D will respond. PRTAD1 is not needed for device addressing, but shares functionality with the stopwatch latency timer function. PRTAD0 is not used functionally, but is present for device testability and compatibility with other devices in the family of products. PRTAD0 should be grounded on the application board.
RESET_N	F8	Input LVCMOS 1.5V/1.8V VDDO0	**Low True Device Reset.** RESET_N must be held asserted (low logic level) for at least 10us after device power stabilization.
MDC	G5	Input LVCMOS with Hysteresis 1.5V/1.8V VDDO0	**MDIO Clock Input.** Clock input for the MDIO interface. Note that an external pullup is generally not required on MDC except if driven by an open-drain/open-collector clock source.

Table 3-1. Pin Functions - Signal Pins (continued)

PIN		DIRECTION TYPE SUPPLY	DESCRIPTION
SIGNAL	BGA		
MDIO	F5	Input/ Output LVCMOS 1.5V/1.8V VDDO0 25Ω Driver	**MDIO Data I/O.** MDIO interface data input/output signal for the MDIO interface. **This signal must be externally pulled up to VDDO using a 2kΩ resistor.** During device reset (RESET_N asserted low) this pin is floating. During software initiated power down the management interface remains active for control register writes and reads. Certain status bits will not be deterministic as their generating clock source may be disabled as a result of asserting either power down input signal. During pin based power down (PDTRXA_N, PDTRXB_N, PDTRXC_N, and PDTRXD_N asserted low), this pin is floating. During register based power down (30.1.15 asserted high all channels), this pin is driven normally.
TDI	E12	Input LVCMOS 1.5V/1.8V VDDO1 (Internal Pullup)	**JTAG Input Data.** TDI is used to serially shift test data and test instructions into the device during the operation of the test port. In system applications where JTAG is not implemented, this input signal may be left floating. During pin based power down (PDTRXA_N, PDTRXB_N, PDTRXC_N, and PDTRXD_N asserted low), this pin is not pulled up. During register based power down (30.1.15 asserted high all channels), this pin is pulled up normally.
TDO	G14	Output LVCMOS 1.5V/1.8V VDDO1 50Ω Driver	**JTAG Output Data.** TDO is used to serially shift test data and test instructions out of the device during operation of the test port. When the JTAG port is not in use, TDO is in a high impedance state. During device reset (RESET_N asserted low) this pin is floating. During pin based power down (PDTRXA_N, PDTRXB_N, PDTRXC_N, and PDTRXD_N asserted low), this pin is floating. During register based power down (30.1.15 asserted high all channels), this pin is floating.
TMS	E14	Input LVCMOS 1.5V/1.8V VDDO1 (Internal Pullup)	**JTAG Mode Select.** TMS is used to control the state of the internal test-port controller. In system applications where JTAG is not implemented, this input signal can be left unconnected. During pin based power down (PDTRXA_N, PDTRXB_N, PDTRXC_N, and PDTRXD_N asserted low), this pin is not pulled up. During register based power down (30.1.15 asserted high all channels), this pin is pulled up normally.
TCK	E13	Input LVCMOS with Hysteresis 1.5V/1.8V VDDO1	**JTAG Clock.** TCK is used to clock state information and test data into and out of the device during boundary scan operation. In system applications where JTAG is not implemented, this input signal should be grounded.
TRST_N	H13	Input LVCMOS 1.5V/1.8V VDDO1 (Internal Pulldown)	**JTAG Test Reset.** TRST_N is used to reset the JTAG logic into system operational mode. This input can be left unconnected in the application and is pulled down internally, disabling the JTAG circuitry. If JTAG is implemented on the application board, this signal should be deasserted (high) during JTAG system testing, and otherwise asserted (low) during normal operation mode. During pin based power down (PDTRXA_N, PDTRXB_N, PDTRXC_N, and PDTRXD_N asserted low), this pin is not pulled down. During register based power down (30.1.15 asserted high all channels), this pin is pulled down normally.
TESTEN	C8	Input LVCMOS 1.5V/1.8V VDDO0	**Test Enable.** This signal is used during the device manufacturing process. It should be grounded through a resistor in the device application board. The application board should allow the flexibility of easily reworking this signal to a high level if device debug is necessary (by including an uninstalled resistor to VDDO).
GPI[2:0]	M14 P14 D5	Input LVCMOS .5V/1.8V VDDO0,2	G**eneral Purpose Input.** This signal is used during the device manufacturing process. It should be grounded through a resistor on the device application board. The application board should also allow the flexibility of easily reworking this signal to a high level if device debug is necessary (by including an uninstalled resistor to VDDO).
AMUXA_LS/HS	E2 B8	Analog I/O	**Analog Testability I/O.** This signal is used during the device manufacturing process. It should be left unconnected in the device application.
AMUXB_LS/HS	P2 U8	Analog I/O	**Analog Testability I/O.** This signal is used during the device manufacturing process. It should be left unconnected in the device application.
AMUXC_LS/HS	E17 B10	Analog I/O	**Analog Testability I/O.** This signal is used during the device manufacturing process. It should be left unconnected in the device application.
AMUXD_LS/HS	P17 U10	Analog I/O	**Analog Testability I/O.** This signal is used during the device manufacturing process. It should be left unconnected in the device application.

Table 3-2. Pin Description - Power Pins

TERMINAL		TYPE	DESCRIPTION
SIGNAL	BGA		
VDDA[1:0]_LS/HS	H2, H3, L2, M3, F9, E10, F11, G16, H17, L16, L17, N9, P10, N11	Power	**SERDES Analog Power.** VDDA_LS and VDDA_HS provide supply voltage for the analog circuits on the low-speed and high-speed sides respectively. 1.0V nominal. Can be tied together on the application board.

Table 3-2. Pin Description - Power Pins (continued)

TERMINAL		TYPE	DESCRIPTION
SIGNAL	BGA		
VDDT[1:0]_LS/HS	J5, K5, E8, J14, K14, P8	Power	**SERDES Analog Power.** VDDT_LS and VDDT_HS provide termination and supply voltage for the analog circuits on the low-speed and high-speed sides respectively. 1.0V nominal. Can be tied together on the application board.
VDDD	H8, J8, K8, L8, M9, G10, H11, J11, K11, L11	Power	**SERDES Digital Power.** VDDD provides supply voltage for the digital circuits internal to the SERDES. 1.0V nominal.
DVDD	H7, K7, L7, H9, J9, L9, H10, K10, L10, H12, J12, L12	Power	**Digital Core Power.** DVDD provides supply voltage to the digital core. 1.0V nominal.
VDDRA_LS/HS	G4 B6	Power	**SERDES Analog Regulator Power.** VDDRA_LS and VDDRA_HS provide supply voltage for the internal PLL regulator for Channel A low speed and high speed sides respectively. 1.5V or 1.8V nominal.
VDDRB_LS/HS	K4 U6	Power	**SERDES Analog Regulator Power** VDDRB_LS and VDDRB_HS provide supply voltage for the internal PLL regulator for Channel B low speed and high speed sides respectively. 1.5V or 1.8V nominal.
VDDRC_LS/HS	J15 B12	Power	**SERDES Analog Regulator Power.** VDDRC_LS and VDDRC_HS provide supply voltage for the internal PLL regulator for Channel C low speed and high speed sides respectively. 1.5V or 1.8V nominal.
VDDRD_LS/HS	M15 U12	Power	**SERDES Analog Regulator Power** VDDRD_LS and VDDRD_HS provide supply voltage for the internal PLL regulator for Channel D low speed and high speed sides respectively. 1.5V or 1.8V nominal.
VDDO[3:0]	M7 M12 G12 G7	Power	**LVCMOS I/O Power.** VDDO0[3:0] and VDDO1 provide supply voltage for the LVCMOS inputs and outputs. 1.5V or 1.8V nominal. Can be tied together on the application board.
VPP	N7	Power	**Factory Program Voltage.** Used during device manufacturing. The application must connect this power supply directly to DVDD.
VSS	A1, A4, A7, A10, A13, A16, A17, B3, B4, B5, B7, B9, B11, B13, B14, B15, B16, C1, C2, C4, C7, C11, C12, C13, C16, C18, D2, D9, D10, D15, D17, E3, E9, E11, E15, F1, F2, F4, F7, F10, F16, F17, F18, G2, G8, G9, G11, G13, G17, H5, H6, H14, H15, J1, J3, J7, J10, J13, J18, K1, K6, K9, K12, K16, K18, L4, L5, L6, L13, L14, M2, M6, M8, M10, M11, M13, M17, N1, N2, N3, N5, N8, N10, N15, N17, N18, P4, P9, P16, R2, R4, R5, R6, R9, R10, R14, R17, T1, T3, T6, T7, T8, T11, T15, T17, T18, U3, U4, U5, U7, U9, U11, U13, U14, U15, U16, V2, V3, V6, V9, V12, V15, V18	Ground	**Ground.** Common analog and digital ground.

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	DVDD, VDDA, LS/HS, VPP, VDDD	–0.3	1.4	V
	VDDRA/B/C/D_LS/HS, VDDO[3:0]	–0.3	2.2	V
Input Voltage, V_I	LVCMOS/CML/Analog	–0.3	Supply + 0.3	V
Characterized free-air operating temerature		–40	85	°C
Storage temperature T_{stg}		–65	85	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

				MIN	NOM	MAX	UNIT
	Digital / analog supply voltages	VDDD, VDDA_LS/HS, DVDD, VDDT_LS/HS, VPP		0.95	1.00	1.05	V
	SERDES PLL regulator voltage	VDDRA_LS/HS, VDDRB_LS/HS, VDDRC_LS/HS, VDDRD_LS/HS	1.5-V Nominal	1.425	1.5	1.575	V
			1.8-V Nominal	1.71	1.8	1.89	
	LVCMOS I/O supply voltage	VDDO[3:0]	1.5-V Nominal	1.425	1.5	1.575	V
			1.8-V Nominal	1.71	1.8	1.89	
I_{DD}	Supply current	VDDD	10.3 Gbps			913	mA
		VDDA_LS/HS				1020	
		DVDD + VPP				1117	
		VDDT_LS/HS				1249	
		VDDRA/B/C/D_LS				168	
		VDDRA/B/C/D_HS				118	
		VDDO[3:0]				10	
P_D	Power dissipation		Nominal		3.3		W
			All supplies worst case, 10GBASE-KR			3.7(1)	

(1) Total worst-case power is not a sum of the individual power supply worst cases, as the individual worst-case powers are taken from multiple modes. These modes are mutually exclusive and therefore used only for power supply requirements.

Recommended Operating Conditions *(continued)*

over operating free-air temperature range (unless otherwise noted)

				MIN	NOM	MAX	UNIT
I_{SD}	Shutdown current	VDDD	PD* Asserted			125	mA
		VDDA				60	
		DVDD + VPP				130	
		VDDT				95	
		VDDRA_HS/LS + VDDRB_HS/LS + VDDRC_HS/LS + VDDRD_HS/LS				5	
		VDDO				10	

4.4 Thermal Information

THERMAL METRIC[1]		TLK10034 AAJ (FCBGA) 324 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	21.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

4.5 LVCMOS Electrical Characteristics (VDDO)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 2 mA, Driver Enabled (1.8V)	VDDO – 0.45		VDDO	V
		I_{OH} = 2 mA, Driver Enabled (1.5V)	0.75 × VDDO			
V_{OL}	Low-level output voltage	I_{OL} = –2 mA, Driver Enabled (1.8V)	0		0.45	V
		I_{OL} = –2 mA, Driver Enabled (1.5V)			0.25 × VDDO	
V_{IH}	High-level input voltage		0.65 × VDDO		VDDO + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.35 × VDDO	V
I_{IH}, I_{IL}	Receiver only	Low/High Input Current			±170	µA
I_{OZ}	Driver only	Driver Disabled			±25	µA
	Driver/Receiver With Pullup/Pulldown	Driver disabled With Pull Up/Down Enabled			±195	
CIN	Input capacitance				3	pF

4.6 High Speed Side Serial Transmitter Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OD(p-p)}$	TX Output differential peak-to-peak voltage swing, transmitter enabled	SWING (3.15:22) = 0000	50	130	220	mV_{pp}
		SWING (3.15:22) = 0001	110	220	320	
		SWING (3.15:22) = 0010	180	300	430	
		SWING (3.15:22) = 0011	250	390	540	
		SWING (3.15:22) = 0100	320	480	650	
		SWING (3.15:22) = 0101	390	570	770	
		SWING (3.15:22) = 0110	460	660	880	
		SWING (3.15:22) = 0111	530	750	1000	
		SWING (3.15:22) = 1000	590	830	1100	
		SWING (3.15:22) = 1001	660	930	1220	
		SWING (3.15:22) = 1010	740	1020	1320	
		SWING (3.15:22) = 1011	820	1110	1430	
		SWING (3.15:22) = 1100	890	1180	1520	
		SWING (3.15:22) = 1101	970	1270	1610	
		SWING (3.15:22) = 1110	1060	1340	1680	
		SWING (3.15:22) = 1111	1090	1400	1740	
		Transmitter disabled			30	
$V_{pre/post}$	TX Output pre/post cursor emphasis voltage	See register bits TWPOST1, TWPOST2, and TWPRE for de-emphasis settings. See Figure 4-2	–17.5/ –37.5%		+17.5/ +37.5%	
V_{CMT}	TX Output common mode voltage	100-Ω differential termination. DC-coupled.		V_{DDT} - .25*$V_{OD(p-p)}$		mV
t_{skew}	Intra-pair output skew	Serial Rate = 9.8304 Gbps			0.045	UI
T_r, T_f	Differential output signal rise, fall time (20% to 80%), Differential Load = 100Ω		24			ps
J_{T1}	Serial output total jitter (CPRI LV/LV-II/LV-III, OBSAI and 10GBASE-KR Rates)	Serial Rate ≤ 3.072Gbps			0.35	UI_{pp}
		Serial Rate > 3.072Gbps			0.28	
J_{D1}	Serial output deterministic jitter (CPRI LV/LV-II, OBSAI and 10GBASE-KR Rates)	Serial Rate ≤ 3.072Gbps			0.17	UI_{pp}
		Serial Rate > 3.072Gbps			0.15	
J_{R1}	Serial output random jitter (CPRI LV/LV-II/LV-III, OBSAI and 10GBASE-KR Rates)	Serial Rate > 3.072Gbps			0.15	UI_{pp}
J_{T2}	Serial output total jitter (CPRI E.6/12.HV)	Serial Rate = 0.6144 and 1.2288Gbps			0.279	UI_{pp}
J_{D2}	Serial output deterministic jitter (CPRI E.6/12.HV)				0.14	
SDD22	Differential output return loss	50 MHz < f < 2.5 GHz			9	dB
		2.5 GHz < f < 7.5 GHz			See (1)	dB
SCC22	Common-mode output return loss	50 MHz < f < 2.5 GHz			6	dB
		2.5 GHz < f < 7.5 GHz			See (2)	dB
$T_{(LATENCY)}$	Transmit path latency	10GBASE-KR mode	see Figure 5-10			
		1GBASE-KX mode	see Figure 5-11			
		General Purpose mode	see Figure 5-18			

(1) Differential input return loss, SDD22 = 9 – 12 $\log_{10}$(f / 2500MHz)) dB
(2) Common-mode output return loss, SDD22 = 6 – 12 log10(f / 2500MHz)) dB

4.7 High Speed Side Serial Receiver Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ID}	RX Input differential voltage, |RXP – RXN|	Full Rate, AC Coupled	50		600	mV
		Half/Quarter/Eighth Rate, AC Coupled	50		800	
$V_{ID(pp)}$	RX Input differential peak-to-peak voltage swing, 2×|RXP – RXN|	Full Rate, AC Coupled	100		1200	mV_{pp}
		Half/Quarter/Eighth Rate, AC Coupled	100		1600	
C_I	RX Input capacitance				2	pF
J_{TOL}	10GBASE-KR Jitter tolerance, test channel with mTC =1 (see Figure 4-5 for attenuation curve), PRBS31 test pattern at 10.3125 Gbps	Applied sinusoidal jitter			0.115	UI_{pp}
		Applie drandom jitter			0.130	
		Applied duty cycle distortion			0.035	
		Broadband noise amplitude (RMS)			5.2	
SDD11	Differential input return loss	50 MHz < f < 2.5 GHz	9			dB
		2.5 GHz < f < 7.5 GHz	See (1)			
t_{skew}	Intra-pair input skew				0.23	UI
$t_{(LATENCY)}$	Receive path latency	10GBASE-KR mode	see Figure 5-10			
		1GBASE-KX mode	see Figure 5-11			
		General Purpose mode	see Figure 5-18			

(1) Differential input return loss, SDD11 = 9 – 12 $\log_{10}$(f / 2.5GHz)) dB

4.8 Low Speed Side Serial Transmitter Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OD(pp)}$	Transmitter output differential peak-to-peak voltage swing	SWING = 000	110	190	280	mVpp
		SWING = 001	280	380	490	
		SWING = 010	420	560	700	
		SWING = 011	560	710	870	
		SWING = 100	690	850	1020	
		SWING = 101	760	950	1150	
		SWING = 110	800	1010	1230	
		SWING = 111	830	1050	1270	
DE	Transmitter output de-emphasis voltage swing reduction	DE = 0000		0		dB
		DE = 0001		0.42		
		DE = 0010		0.87		
		DE = 0011		1.34		
		DE = 0100		1.83		
		DE = 0101		2.36		
		DE = 0110		2.92		
		DE = 0111		3.52		
		DE = 1000		4.16		
		DE = 1001		4.86		
		DE = 1010		5.61		
		DE = 1011		6.44		
		DE = 1100		7.35		
		DE = 1101		8.38		
		DE = 1110		9.54		
		DE = 1111		10.87		
V_{CMT}	Transmitter output common mode voltage	100-Ω differential termination. DC-coupled.		V_{DDT}-.5*$V_{DD(p-p)}$		mV
t_{skew}	Intra-pair output skew				0.045	UI
t_R, t_F	Differential output signal rise, fall time (20% to 80%) Differential Load = 100Ω		30			ps

Low Speed Side Serial Transmitter Characteristics *(continued)*

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
J_T	Serial output total jitter				0.35	UI
J_D	Serial output deterministic jitter				0.17	UI
t_{skew}	Lane-to-lane output skew				50	ps

4.9 Low Speed Side Serial Receiver Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ID}	Receiver input differential voltage, |INP – INN|	Full Rate, AC Coupled	50		600	mV
		Half/Quarter Rate, AC Coupled	50		800	
$V_{ID(pp)}$	Receiver input differential peak-to-peak voltage swing 2×|INP – INN|	Full Rate, AC Coupled	100		1200	mV_{dfpp}
		Half/Quarter Rate, AC Coupled	100		1600	
C_I	Receiver input capacitance				2	pF
J_{TOL}	Jitter tolerance, total jitter at serial input (DJ + RJ) (BER 10^{-15})	Zero crossing, Half/Quarter Rate			0.66	UI_{p-p}
		Zero crossing, Full Rate			0.65	
J_{DR}	Serial input deterministic jitter (BER 10^{-15})	Zero crossing, Half/Quarter Rate			0.50	UI_{p-p}
		Zero crossing, Full Rate			0.35	
t_{skew}	Intra-pair input skew				0.23	UI
$t_{lane-skew}$	Lane-to-lane input skew				30	UI

4.10 Reference Clock Characteristics (REFCLK0P/N, REFCLK1P/N)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F	Frequency		122.88		425	MHz
FHS_{offset}	Accuracy	Relative to Nominal HS Serial Data Rate	–100		100	ppm
		Relative to Incoming HS Serial Data Rate	–200		200	
DC	Duty cycle	High Time	45%	50%	55%	
V_{ID}	Differential input voltage		250		2000	mV_{pp}
C_{IN}	Input capacitance				1	pF
R_{IN}	Differential input impedance		80	100	120	Ω
T_{RISE}	Rise/fall time	10% to 90%	50		350	ps
J_R	Random jitter	10 kHz to 1 MHz			3	ps-RMS
		Above 1 MHz			1	ps-RMS

4.11 Differential Output Clock Characteristics (CLKOUTA/B/C/DP/N)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OD}	Differential output voltage	Peak to peak	1000		2000	mV_{pp}
T_{RISE}	Output rise time	10% to 90%, 2pF lumped capacitive load, AC-Coupled			350	ps
R_{TERM}	Output termination	CLKOUT×P/N to DVDD		50		Ω
F	Output frequency		0		500	MHz

4.12 MDIO Timing Requirements

over recommended operating conditions (unless otherwise noted)

			MIN	NOM	MAX	UNIT
t_{period}	MDC period	See Figure 4-3	100			ns
t_{setup}	MDIO setup to ↑ MDC		10			ns
t_{hold}	MDIO hold to ↑ MDC		10			ns
T_{valid}	MDIO valid from MDC ↑		0		40	ns

4.13 JTAG Timing Requirements

over recommended operating conditions (unless otherwise noted)

			MIN	NOM	MAX	UNIT
T_{PERIOD}	TCK period	See Figure 4-4	66.67			ns
T_{SETUP}	TDI/TMS/TRST_N setup to ↑ TCK		3			
T_{HOLD}	TDI/TMS/TRST_N hold from ↑ TCK		5			
T_{VALID}	TDO delay from TCK Falling		0		10	ns

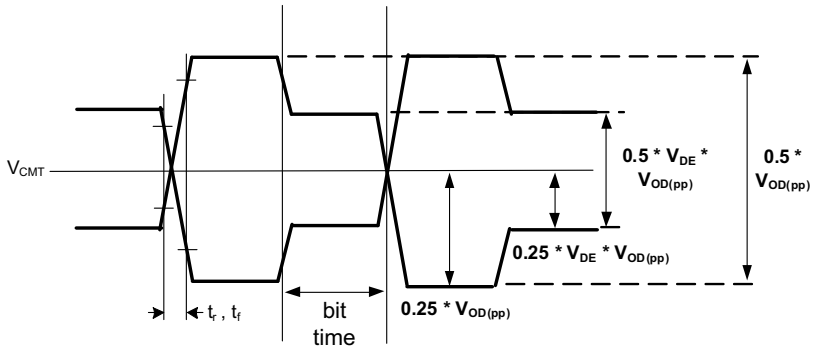
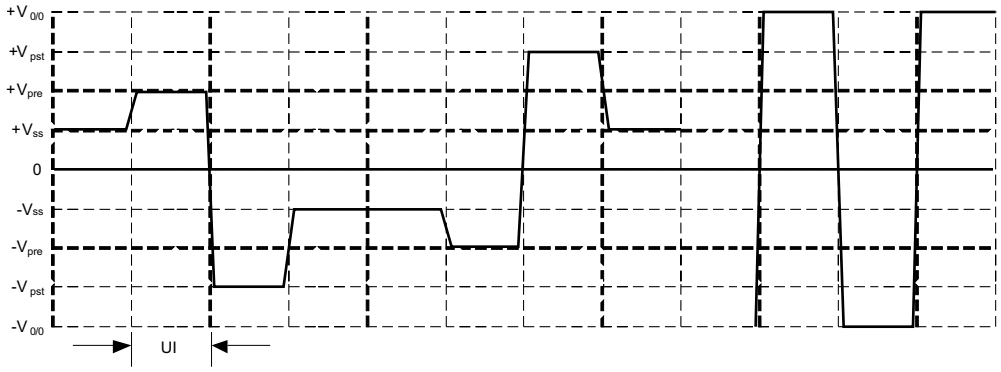


Figure 4-1. Transmit Output Waveform Parameter Definitions



h_{-1} = TWPRE (0% ⩾ -17.5% for typical application) setting

h_1 = TWPOST1 (0% ⩾ -37.5% for typical application) setting

$h_0 = 1 - |h_1| - |h_{-1}|$

$V_{0/0}$ = Output Amplitude with TWPRE = 0%, TWPOST = 0%.

V_{ss} = Steady State Output Voltage = $V_{0/0} * | h_1 + h_0 + h_{-1}|$

V_{pre} = PreCursor Output Voltage = $V_{0/0} * | -h_1 - h_0 + h_{-1}|$

V_{pst} = PostCursor Output Voltage = $V_{0/0} * | -h_1 + h_0 + h_{-1}|$

Figure 4-2. Pre and Post Cursor Swing Definitions

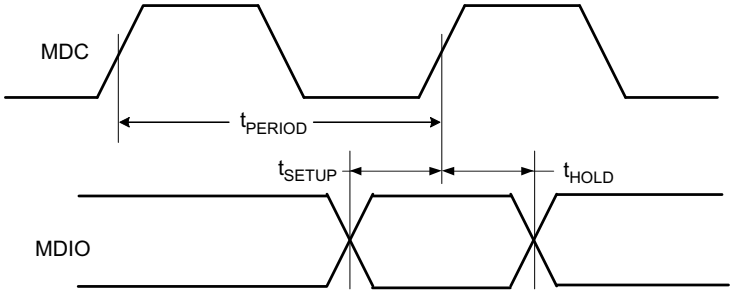


Figure 4-3. MDIO Read and Write Timing

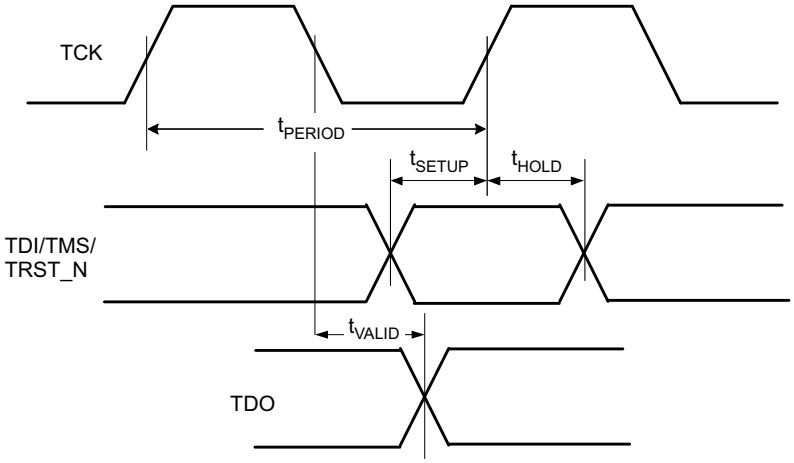


Figure 4-4. JTAG Timing

4.14 Typical Characteristics

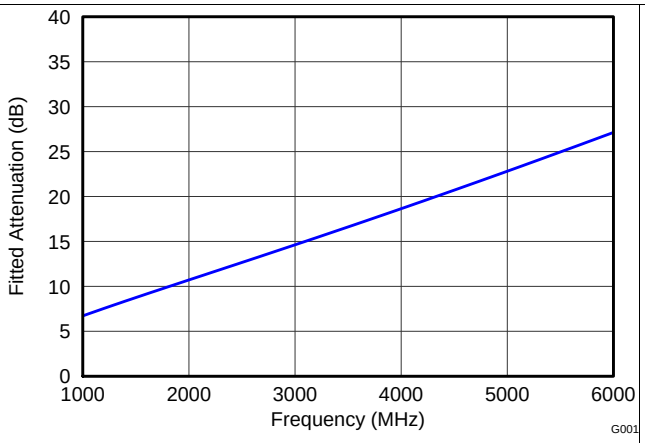


Figure 4-5. 10GBASE-KR Fitted Channel Attenuation Limit

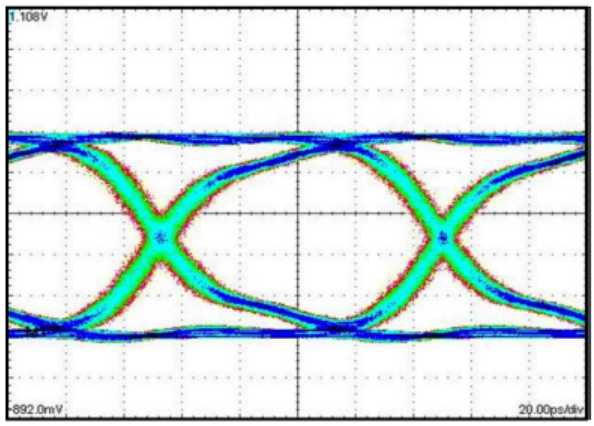


Figure 4-6. Eye Diagram of the TLK100034 at 10.3125 Gbps Under Nominal Conditions

5 Detailed Description

5.1 Overview

Various interfaces of the TLK10034 device are shown in Figure 5-1 for Channel A. The implementation of all four channels is identical. The block diagrams for the transmit and receive data paths are shown in Figure 5-2. This low-power transceiver consists of two serializer/deserializer (SERDES) blocks, one on the low speed side and the other on the high speed side. The core logic block that lies between the two SERDES blocks carries out all the logic functions including channel synchronization, lane alignment, 8B/10B and 64B/66B encoding/decoding, as well as test pattern generation and verification. The TLK10034 provides a management data input/output (MDIO) interface as well as a JTAG interface for device configuration, control, and monitoring. Detailed description of the TLK10034 pin functions is provided in Table 3-1.

5.2 Functional Block Diagrams

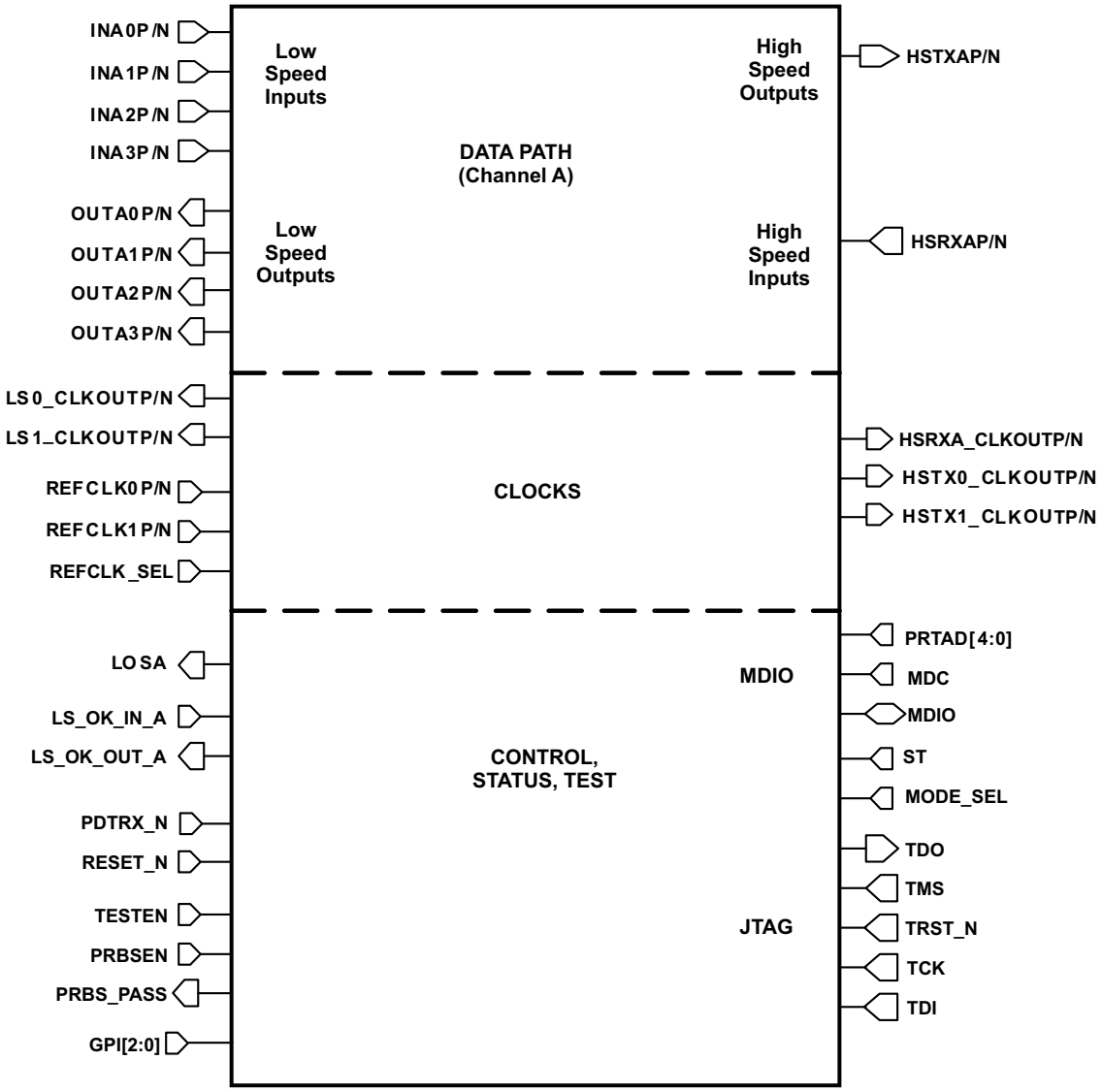


Figure 5-1. TLK10034 Interfaces

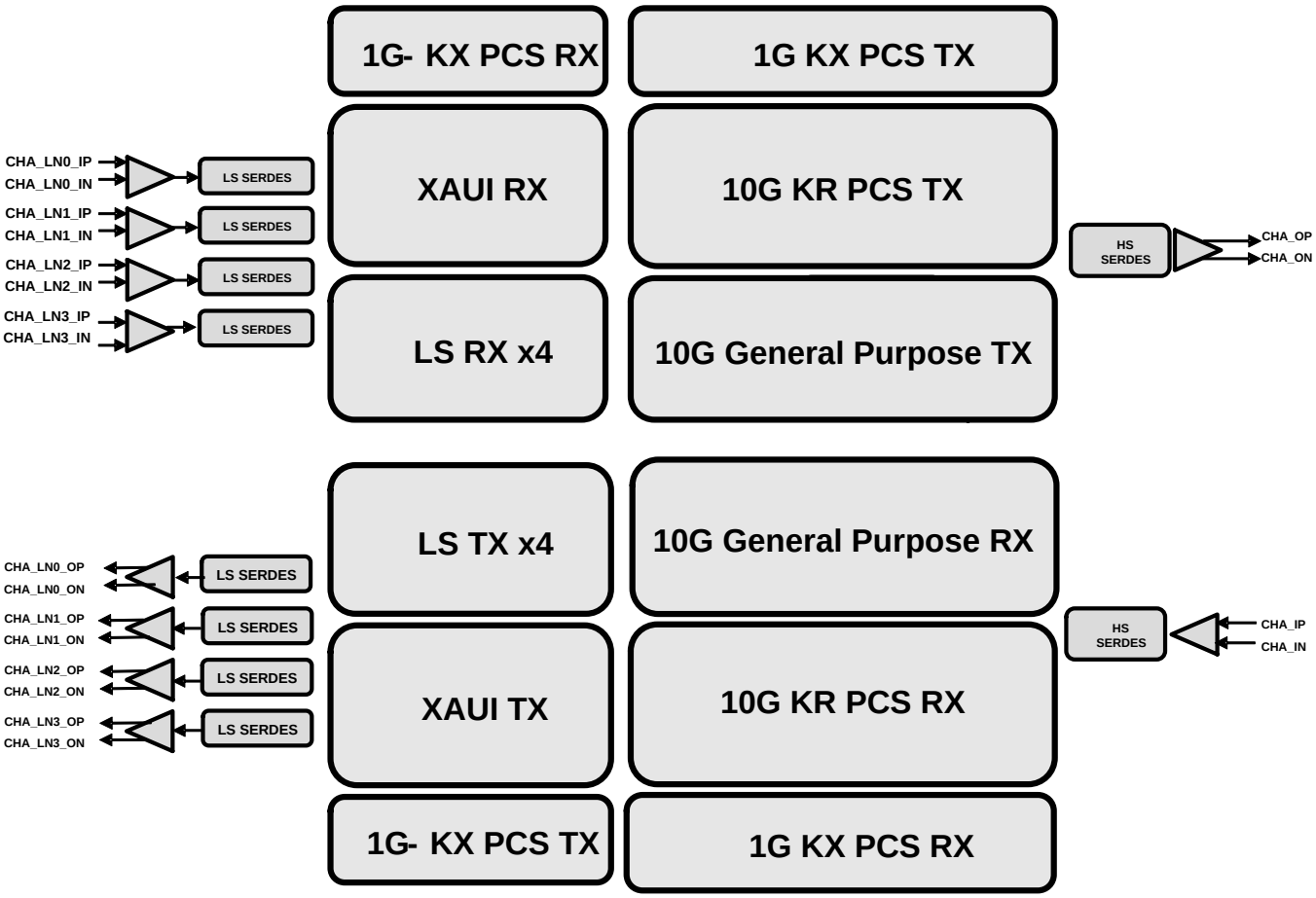


Figure 5-2. Simplified, One-Channel Block Diagram of TLK10034 Data Paths

5.3 Feature Description

5.3.1 10GBASE-KR Mode

5.3.1.1 10GBASE-KR Transmit Data Path Overview

In 10GBASE-KR Mode, the TLK10034 takes in XAUI data on the four low speed input lanes. The serial data in each lane is deserialized into 10-bit parallel data, then byte aligned (channel synchronized) based on comma detection. The four XAUI lanes are then aligned with one another, and the aligned data is input to four 8B/10B decoders. The decoded data is then input to the transmit clock tolerance compensation (CTC) block which compensates for any frequency offsets between the incoming XAUI data and the local reference clock. The CTC block then delivers the data to a 64B/66B encoder and a scrambler. The resulting scrambled 10GBASE-KR data is then input to a transmit gearbox which in turn delivers it to the high speed side SERDES for serialization and output through the HSTX*P/N pins.

5.3.1.2 10GBASE-KR Receive Data Path Overview

In the receive direction, the TLK10034 will take in 64B/66B-encoded serial 10GBASE-KR data on the HSRX*P/N pins. This data is deserialized by a high speed SERDES, then input to a receive gearbox. After the gearbox, the data is aligned to 66-bit frames, descrambled, 64B/66B decoded, and then input to the receive CTC block. After CTC, the data is encoded by four 8B/10B encoders, and the resulting four 10-bit parallel words are serialized by the low speed SERDES blocks. The four serial XAUI output lanes are transmitted out the OUT*P/N pins.

5.3.1.3 Channel Synchronization Block

When parallel data is clocked into a parallel-to-serial converter, the byte boundary that was associated with the parallel data is lost in the serialization of the data. When the serial data is received and converted to parallel format again, a method is needed to be able to recognize the byte boundary again. Generally, this is accomplished through the use of a synchronization pattern. This is a unique pattern of 1's and 0's that either cannot occur as part of valid data or is a pattern that repeats at defined intervals. 8B/10B encoding contains a character called the comma (b'0011111' or b'1100000') which is used by the comma detect circuit to align the received serial data back to its original byte boundary. The TLK10034 channel synchronization block detects the comma pattern found in the K28.5 character, generating a synchronization signal aligning the data to their 10-bit boundaries for decoding. It is important to note that the comma can be either a (b'0011111') or the inverse (b'1100000') depending on the running disparity. The TLK10034 decoder will detect both patterns.

The TLK10034 performs channel synchronization per lane as shown in the flowchart of Figure 5-3.

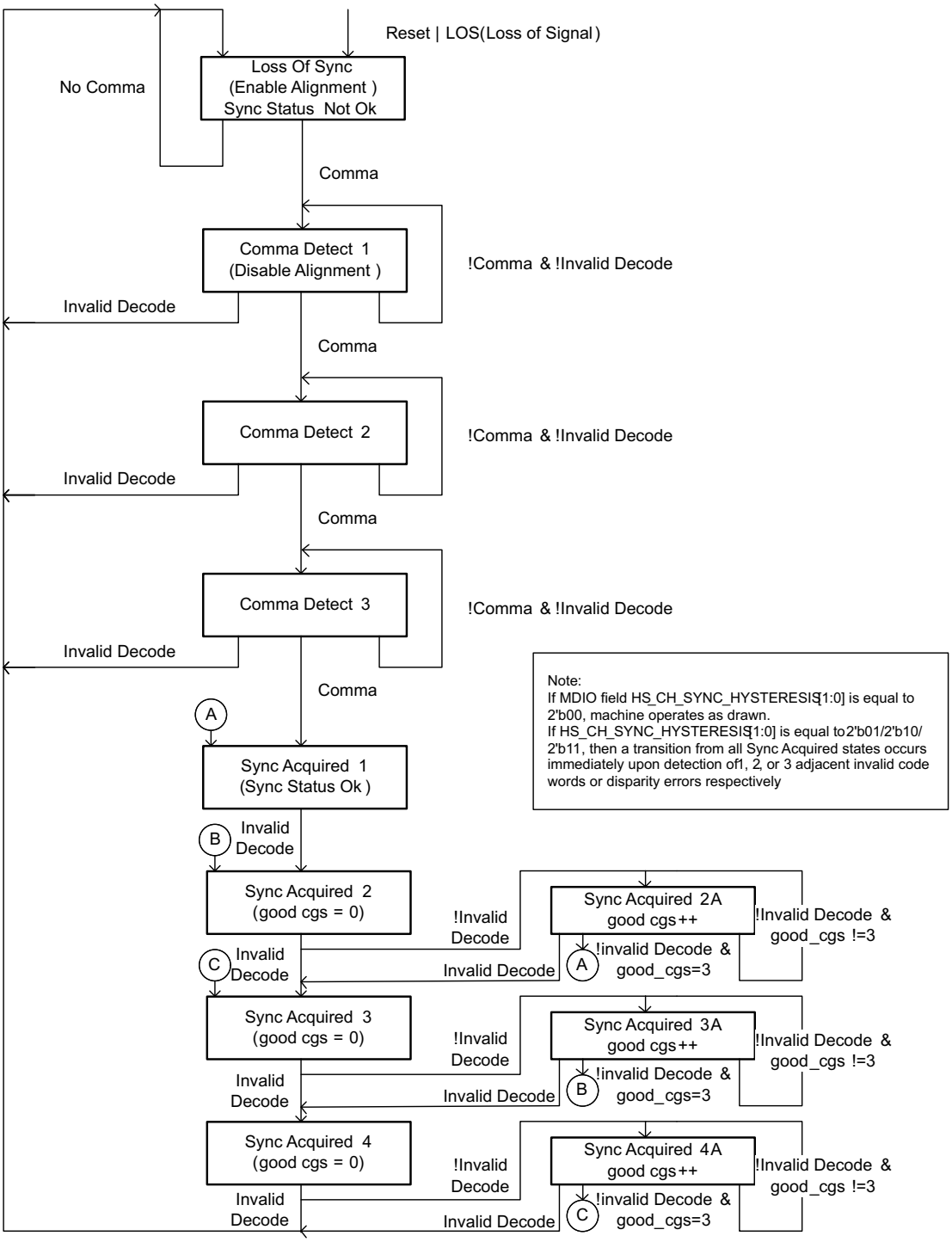


Figure 5-3. Channel Synchronization Flowchart

5.3.1.4 8B/10B Encoder

Embedded-clock serial interfaces require a method of encoding to ensure sufficient transition density for the receiving CDR to acquire and maintain lock. The encoding scheme also maintains the signal DC balance by keeping the number of ones and zeros balanced which allows for AC coupled data transmission. The TLK10034 uses the 8B/10B encoding algorithm that is used by 10Gbps and 1Gbps Ethernet and Fibre Channel standards. This provides good transition density for clock recovery and improves error checking.

The 8B/10B encoder converts each 8-bit wide data to a 10-bit wide encoded data character to improve its transition density. This transmission code includes /D/ Characters, used for transmitting data, and /K/ Characters, used for transmitting protocol information. Each /K/ or /D/ character code word can also have both a positive and a negative disparity version. The disparity of a code word is selected by the encoder to balance the running disparity of the serialized data stream.

5.3.1.5 8B/10B Decoder

Once the Channel Synchronization block has identified the byte boundaries from the received serial data stream, the 8B/10B decoder converts 10-bit 8B/10B-encoded characters into their respective 8-bit formats. When a code word error or running disparity error is detected in the decoded data, the appropriate LOS pin is asserted (depending on the LOS overlay selection).

5.3.1.6 64B/66B Encoder/Scrambler

To facilitate the transmission of data received from the media access control (MAC) layer, the TLK10034 encodes data received from the MAC using the 64B/66B encoding algorithm defined in the IEEE802.3ae Clause 49.2.4 standard. The TLK10034 takes two consecutive transfers from the XAUI interface and encodes them into a 66-bit code word. The information from the two XAUI transfers includes 64 bits of data and 8 bits of control information after 8B/10B decoding.

If the 64B/66B encoder detects an invalid packet format from the XAUI interface, it replaces erroneous information with appropriately-encoded error information. The resulting 66-bit code word is then sent on to the transmit gearbox.

The encoding process implemented in the TLK10034 includes two steps:

1. an encoding step, which converts the 72 bits of data (8 data bytes plus 8 control-code indicators) received from the transmit CTC FIFO into a 66-bit code word
2. a scrambling step, which scrambles 64 bits of encoded data using the scrambler polynomial $x^{57}+x^{39}+1$. The 66 bits created by the encoder consists of 64 bits of data and a 2-bit synchronization field consisting of either 01 or 10. Only the 64 bits of data are scrambled, leaving the two synchronization bits unmodified. The two synchronization bits allow the receive gearbox to obtain frame alignment and, in addition, ensure an edge transition of at least once in 66 bits of data. The encoding process allows a limited amount of control information to be sent in-line with the data.

5.3.1.7 64B/66B Decoder/Descrambler

The data received from the serial 10GBASE-KR is 64B/66B-encoded data. The TLK10034 decodes the data received using the 64B/66B decoding algorithm defined in the IEEE 802.3-2008 Clause 49.2.4 standard. The TLK10034 creates consecutive 72-bit data words from the encoded 66-bit code words for transfer over the XAUI interface to the MAC. The information for the two XAUI transfers includes 64 bits of data and 8 bits of control information before 8B/10B encoding.

Not all 64B/66B block payloads are valid. Invalid block payloads are handled by the 64B/66B decoder block and appropriate error handling is provided, as defined in the IEEE 802.3-2008 standard. The decoding algorithm includes two steps: a descrambling step which descrambles 64 bits of the 66-bit code word with the scrambling polynomial $x^{57}+x^{39}+1$, and a decoding step which converts the 66 bits of data received into 64 bits of data and 8 bits of control information. These words are sent to the receive CTC FIFO.

5.3.1.8 Transmit Gearbox

The function of the transmit gearbox is to convert the 66-bit encoded, scrambled data stream into a 16-bit-wide data stream to be sent out to the serializer and ultimately to the physical medium attachment (PMA) device. The gearbox is needed because while the effective bit rate of the 66-bit data stream is equal to the effective bit rate of the 16-bit data, the clock rates of the two buses are of different frequencies.

5.3.1.9 Receive Gearbox

While the transmit gearbox only performs the task of converting 66-bit data to be transported on to the 16-bit serializer, the receive gearbox has more to do than just the reverse of this function. The receive gearbox must also determine where within the incoming data stream the boundaries of the 66-bit code words are.

The receive gearbox has the responsibility of initially synchronizing the header field of the code words and continuously monitoring the ongoing synchronization. After obtaining synchronization to the incoming data stream, the gearbox assembles 66-bit code words and presents these to the 64B/66B decoder.

Note that in FEC mode, the Receive Gearbox blindly converts 16-bit data to 66-bit data and depends on the RX FEC logic to frame align the data.

5.3.1.10 XAUI Lane Alignment / Code Gen (XAUI PCS)

The XAUI interface standard is defined to allow for 21 UI of skew between lanes. This block is implemented to handle up to 30 UI (XAUI UI) of skew between lanes using /A/ characters. The state machine follows the standard 802.3-2008 defined state machine.

5.3.1.11 XAUI Inter-Packet Gap (IPG) Handling

The XAUI interface transports information that consists of packets and inter-packet gap (IPG) characters. The IEEE 802.3ae standard defines that the IPG, when transferred over the XAUI interface, consists of alignment characters (/A/), control characters (/K/) and replacement characters (/R/).

TLK10034 converts all AKR characters to IDLE characters, performs insertions or deletions on the IDLE characters, and transmits only encoded IDLE characters out to the 10GBASE-KR interface. The receive channel expects encoded IDLE characters to enter the 10GBASE-KR interface, and performs insertions and deletions on IDLE characters and then converts IDLE characters back to AKR characters. Any AKR characters received on the high speed interface are by default converted to IDLE characters for reconversion to AKR columns.

Both the transmit and receive FIFOs rely upon a valid IDLE stream to perform clock tolerance compensation (CTC).

5.3.1.12 Clock Tolerance Compensation (CTC)

The XAUI interface is defined to allow for separate clock domains on each side of the link. Though the reference clocks for two devices on a XAUI link have the same specified frequencies, there are slight differences that, if not compensated for, will lead to over or under run of the FIFO's on the receive/transmit data path. The TLK10034 provides compensation for these differences in clock frequencies via the insertion or the removal of idle (/I/) characters on all lanes, as shown in Figure 5-4 and Figure 5-5.

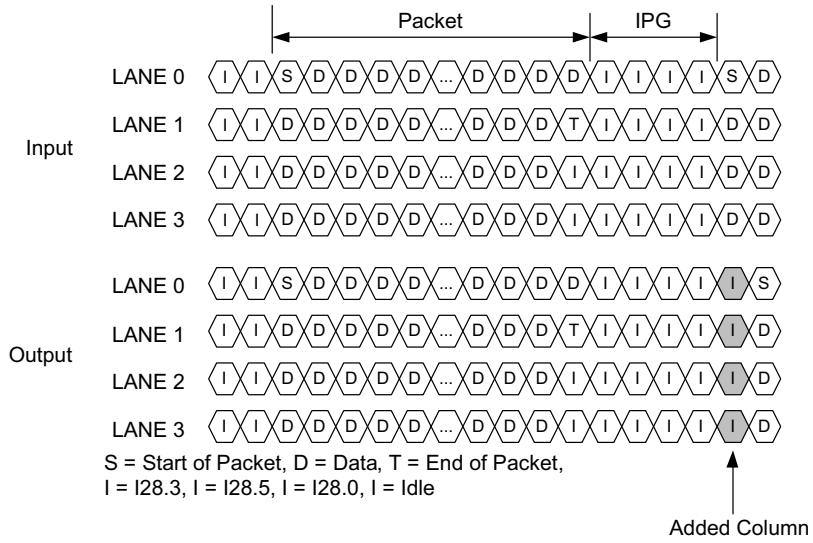


Figure 5-4. Clock Tolerance Compensation: Add

The /R/ code is disparity neutral, allowing its removal or insertion without affecting the current running disparity of each channel's serial stream.

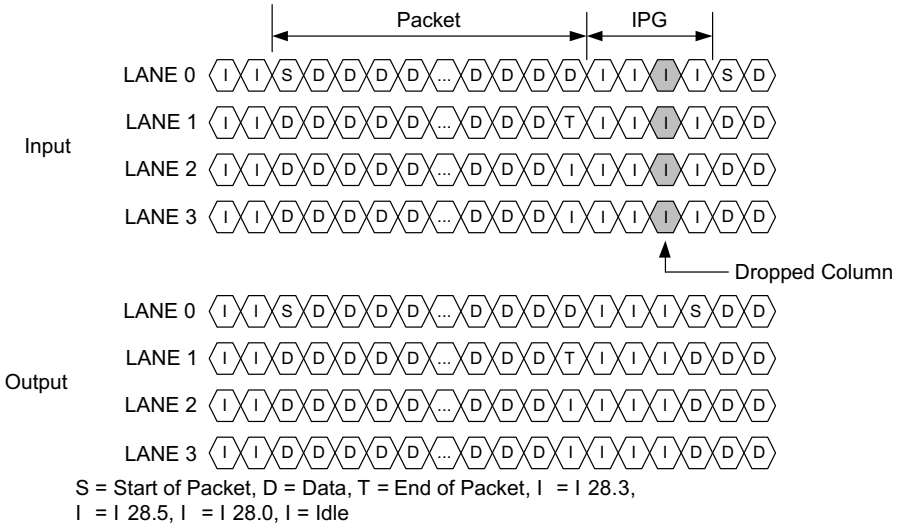


Figure 5-5. Clock Tolerance Compensation: Drop

The TLK10034 allows for provisioning of both the CTC FIFO depth and the low/high watermark thresholds that trigger idle insertion/deletion beyond the standard requirements. This allows for optimization between maximum clock tolerance and packet length. For more information on the TLK10034 CTC provisioning, see Appendix A.

5.3.1.13 10GBASE-KR Auto-Negotiation

When TLK10034 is selected to operate in 10GKR/1G-KX mode (MODE_SEL pin held low), Clause 73 Auto-Negotiation will commence after power up or hardware or software reset. The data path chosen from the result of Auto-Negotiation will be the highest speed of 10G-KR or 1G-KX as advertised in the MDIO ability fields (set to 10G-KR by default). If 10G-KR is chosen, link training will commence immediately following the completion of Auto-Negotiation. Legacy devices that operate in 1G-KX mode and do not support Clause 73 Auto Negotiation will be recognized through the Clause 73 parallel detect mechanism.

5.3.1.14 10GBASE-KR Link Training

Link training for 10G-KR mode is performed after auto-negotiation, and follows the procedure described in IEEE 802.3-2008. The high speed TX SERDES side will update pre-emphasis tap coefficients as requested through the Coefficient update field. Received training patterns are monitored for bit errors (MDIO configurable), and requests are made to update partner channel TX coefficients until optimal settings are achieved.

The RX link training algorithm consists of sending a series of requests to move the link partner's transmitter tap coefficients to the center point of an error free region. Once link training has completed, the 10G-KR data path is enabled. If link is lost, the entire process repeats with auto-negotiation, link training, and 10G-KR mode.

5.3.1.15 Forward Error Correction

Optionally enabled, Forward Error Correction (FEC) follows the IEEE 802.3-2008 standard, and is able to correct a burst errors up to 11 bits. In the TX data path, the FEC logic resides between the scrambler and gearbox. In the RX datapath, FEC resides between the gearbox and descrambler. Frame alignment is handled inside the RX FEC block during FEC operation, and the RX gearbox sync header alignment is bypassed. Because latency is increased in both the TX and RX data paths with FEC enabled, it is disabled by default and must be enabled through MDIO programming. Note that FEC by nature will add latency due to frame storage.

5.3.1.16 10GBASE-KR Line Rate, PLL Settings, and Reference Clock Selection

The TLK10034 includes internal low-jitter high quality oscillators that are used as frequency multipliers for the low speed and high speed SERDES and other internal circuits of the device. Specific MDIO registers are available for SERDES rate and PLL multiplier selection to match line rates and reference clock (REFCLK0/1) frequencies for various applications.

The external differential reference clock has a large operating frequency range allowing support for many different applications. The reference clock frequency must be within ±200 PPM of the incoming serial data rate (±100 PPM of nominal data rate), and have less than the specified jitter characteristics (see Section 4.10).

When the TLK10034 device is set to operate in the 10GBASE-KR mode with a low speed side line rate of 3.125Gbps and a high speed side line rate of 10.3125Gbps, the reference clock choices are as shown in Table 5-1.

Table 5-1. Specific Line Rate and Reference Clock Selection for the 10GBASE-KR Mode

LOW SPEED SIDE					HIGH SPEED SIDE			
Line Rate (Mbps)	SERDES PLL Multiplier	Rate	REFCLKP/N (MHz)		Line Rate (Mbps)	SERDES PLL Multiplier	Rate	REFCLKP/N (MHz)
3125	10	Full	156.25		10312.5	16.5	Full	156.25
3125	5	Full	312.5		10312.5	8.25	Full	312.5

5.3.1.17 10GBASE-KR Loopback Modes

In 10G-KR mode, the TLK10034 supports looping back of data on both the XAUI (local) side and 10G-KR (remote) side. In either case, the loopback point can be chosed to be either prior to serialization (shallow) or after serialization (deep). The various loopback modes can be activated and configured via MDIO register settings.

The datapath for deep remote loopback is shown in Figure 5-6. The data is accepted on the high speed side receive SERDES pins (HSRX*P/N), traverses the entire receive data path is returned through the entire transmit data path and sent out through the high speed side transmit SERDES pins (HSTX*P/N). The low speed side outputs on OUT*P/N pins are still available for monitoring and should be correctly terminated. The low speed side inputs on IN*P/N should be electrically idle (floating).

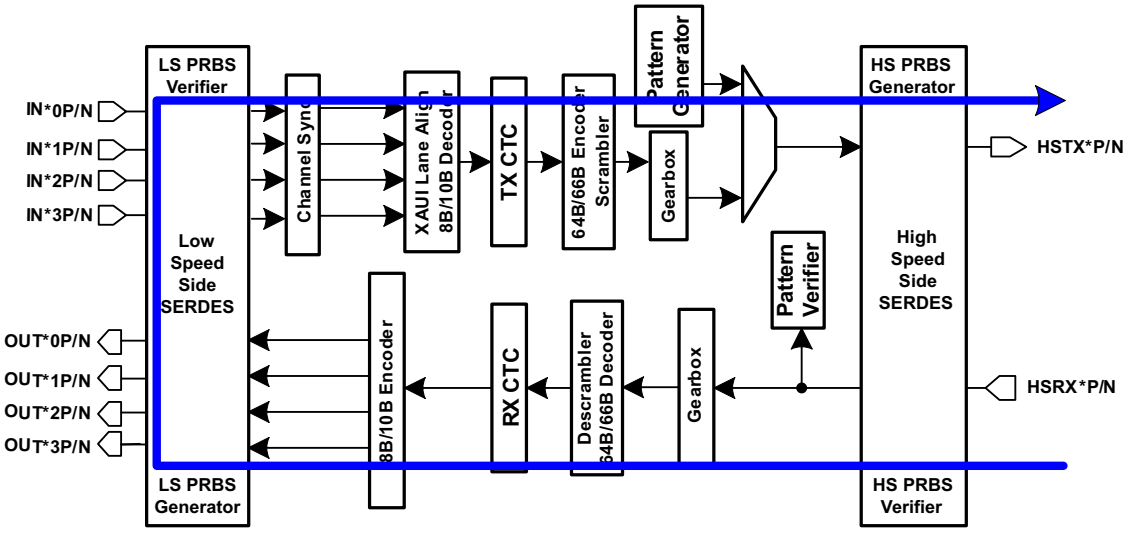


Figure 5-6. Deep Remote Loopback for the 10GBASE-KR Mode

Note that in deep remote loopback mode, the the LS serial transmitter is internally connected directly to the LS serial receiver. This short, low-loss interconnect will have different properties than a typical PCB interconnect, so different transmit and receive link settings should be used to optimize BER.

The datapath for shallow remote loopback is shown in Figure 5-7. In this mode, the device functions as a high speed serial retimer. The data is accepted on the high speed side receive SERDES pins (HSRX*P/N), traverses the receive data path through the RX CTC block, is looped back before the 8B/10B encoders, and is returned through the transmit data path to be sent out through the high speed side transmit SERDES pins (HSTX*P/N).

The low speed side transmit path SERDES can be optionally enabled or disabled, but the PLL needs to be enabled to provide the required clock. The low speed side outputs on OUTA*P/N pins are available for monitoring and must be correctly terminated.

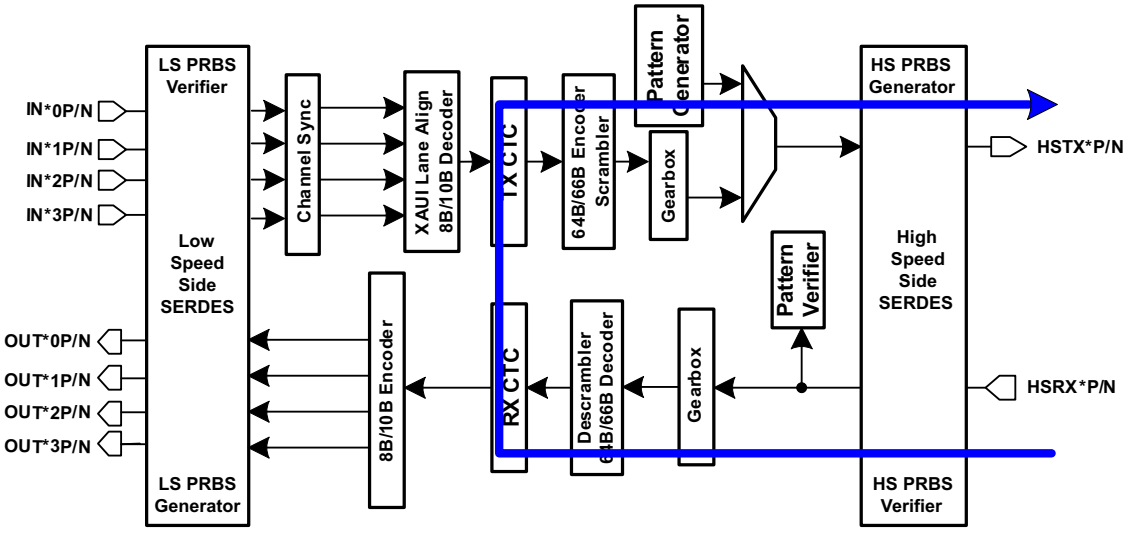


Figure 5-7. Shallow Remote Loopback (Serial Retime) for the 10GBASE-KR Mode

The datapath for deep local loopback is shown in Figure 5-8. The data is accepted on the low speed side SERDES pins (IN*P/N), traverses the entire transmit data path, is returned through the entire receive data path and sent out through the low speed side receive SERDES pins (OUT*P/N). The high speed side outputs on HSTX*P/N pins are available for monitoring. The high speed side inputs on HSRX*P/N should be electrically idle (floating).

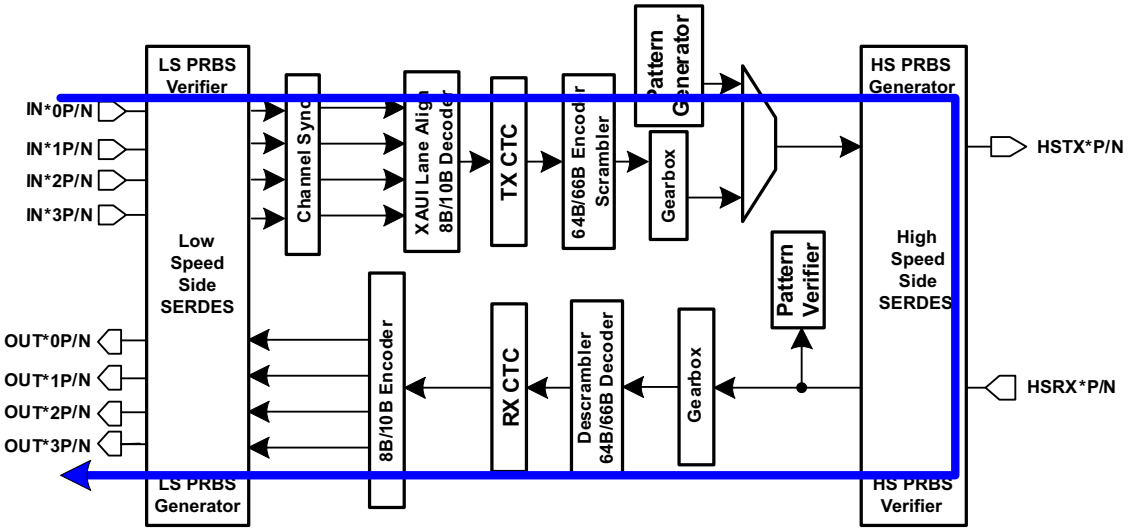


Figure 5-8. Deep Local Loopback for the 10GBASE-KR Mode

Note that in deep local loopback mode, the HS serial transmitter is internally connected directly to the HS serial receiver. This short, low-loss interconnect will have different properties than a typical PCB interconnect, so different transmit and receive link settings should be used to optimize BER.

The datapath for shallow local loopback is shown in Figure 5-9. The data is accepted on the low speed side SERDES pins (IN*P/N), traverses the transmit data path up to the HS SERDES, is looped back before through the receive data path, and sent out through the low speed side receive SERDES pins (OUT*P/N). The high speed side outputs on HSRX*P/N pins are available for monitoring.

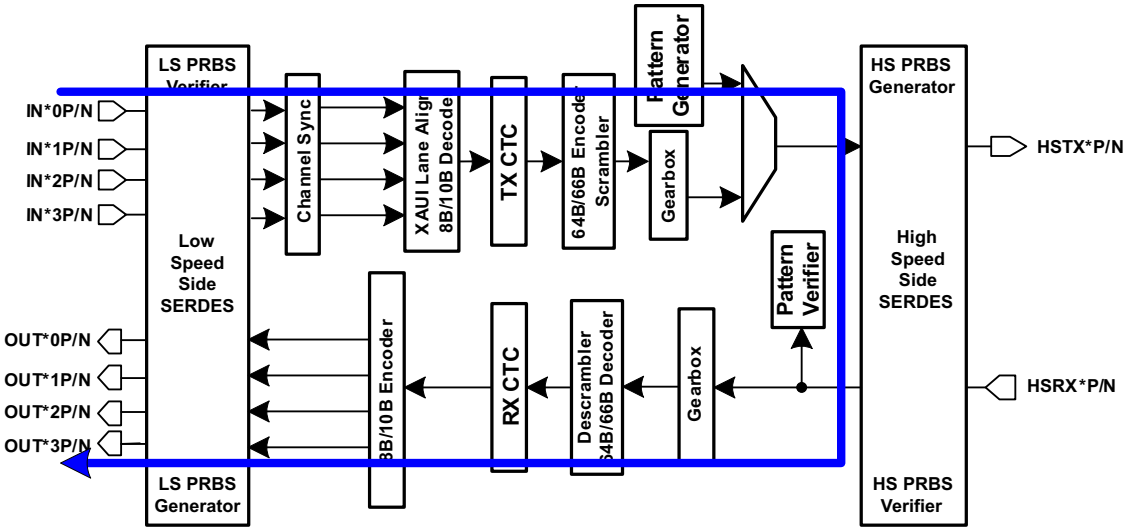


Figure 5-9. Shallow Local Loopback for the 10GBASE-KR Mode

5.3.1.18 10GBASE-KR Test Pattern Support

The TLK10034 has the capability to generate and verify various test patterns for self-test and system diagnostic measurements. The following test patterns are supported:

- High Speed (HS) Side: PRBS 2^7 – 1, PRBS 2^{23} – 1, PRBS 2^{31} – 1, Square Wave with Provisionable Length, and KR Pseudo-Random Pattern
- Low Speed (LS) Side: PRBS 2^7 – 1, PRBS 2^{23} – 1, PRBS 2^{31} – 1, High Frequency, Low Frequency, Mixed Frequency, CRPAT, CJPAT.

The TLK10034 provides two pins: PRBSEN and PRBS_PASS, for additional control and monitoring of PRBS pattern generation and verification. When the PRBSEN is asserted high, the internal PRBS generator and verifier circuits are enabled on both transmit and receive data paths on high speed and low speed sides of all channels. PRBS 2^{31}-1 is selected by default, and can be changed through MDIO.

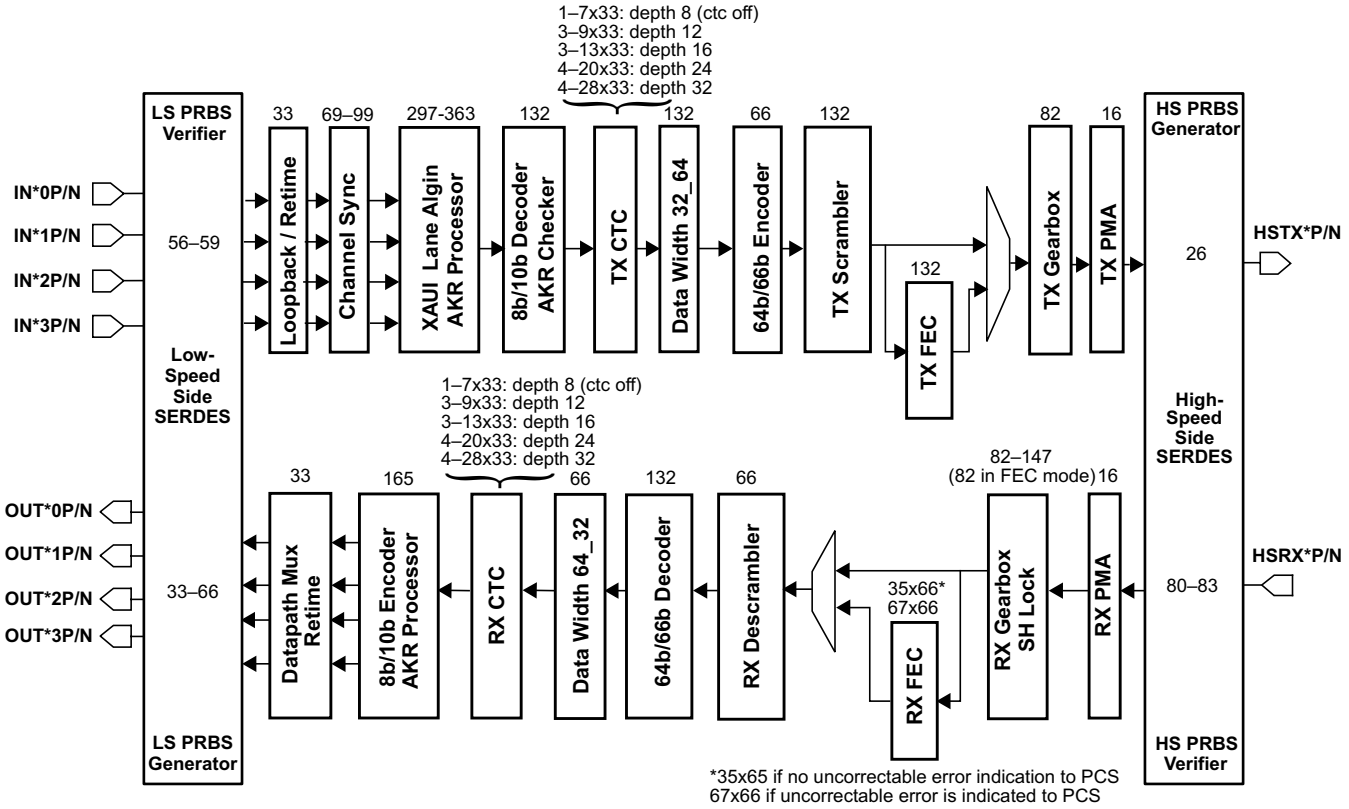
When PRBS test is enabled (PRBSEN=1):

- PRBS_PASS = 1 indicates that PRBS pattern reception is error free.
- PRBS_PASS = 0 indicates that a PRBS error is detected. The channel, the side (high speed or low speed), and the lane (for low speed side) that this signal refers to is chosen through MDIO.

For further details, refer to the application note *TLK10034 Test Pattern Procedures*.

5.3.1.19 10GBASE-KR Latency

The latency through the TLK10034 in 10GBASE-KR mode is as shown in Figure 5-10. Note that the latency ranges shown indicate static rather than dynamic latency variance, i.e., the range of possible latencies when the serial link is initially established. During normal operation, the latency through the device is fixed.



TX, FEC bypassed, CTC depth 12: 1140–1473 UI (111 ns–143 ns)
NOTE: TX Latency numbers represent no external skew between lanes. External lane skew will increase overall latency.

RX, FEC bypassed, CTC depth 12: 772–107 UI (76 ns–104 ns)

Figure 5-10. 10GBASE-KR Mode Latency Per Block

5.3.2 1GBASE-KX Mode

5.3.2.1 Sync 1 GX Block

This block is used to align the deserialized signals to the proper 10-bit word boundaries. The Sync 1 GX block generates a synchronization flag indicating incoming data is synchronized to the correct bit boundary. This module implements the synchronization state machine found in Figure 36-9 of the IEEE 802.3-2008 Standard. A synchronization status signal, latched low, is available to indicate synchronization errors.

5.3.2.2 8b/10b Encoder and Decoder Blocks

As in the 10GBASE-KR operating mode, these blocks are used to convert between 10-bit (encoded) data and 8-bit data words. They can be optionally bypassed. A code invalid signal, latched low, is available to indicate 8b/10b encode and decode errors.

5.3.2.3 RX PCS

This block implements the PCS receive function for Gigabit Ethernet mode as defined in Clause 36. It operates on decoded characters. This block can also be bypassed.

5.3.2.4 TX CTC

The transmit clock tolerance compensation (CTC) block acts as a FIFO with add and delete capabilities, adding and deleting 2 cycles each time to support ±200ppm during IFG (no errors) between the read and write clocks. This block implements a 12 deep asynchronous FIFO with a usable space 8 deep. It has two separate pointer tracking systems. One determines when to delete or insert and another determines when to reset. Inserts and deletes are only allowed during non-errored inter-frame gaps and occurs 2 cycles at a time. It has an auto reset feature once collision occurs. If a collision occurs, the indication is latched high until read by MDIO.

5.3.2.5 TX PCS

The TX PCS block implements the PCS Transmit ordered_set and transmit code_group FSMs as specified in Clause 36. This block can be bypassed.

5.3.2.6 Test Pattern Generator

In 1G-KX mode, this block can be used to generate test patterns allowing the 1G-KX channel to be tested for compliance while in a system environment or for diagnostic purposes. Test patterns generated are high/low/mixed frequency and CRPAT long or short.

5.3.2.7 Test Pattern Verifier

The 1G-KX test pattern verifier performs the verification and error reporting for the CRPAT Long and Short test patterns specified in Annex 36A of the IEEE 802.3-2002 standard. Errors are reported to MDIO registers.

5.3.2.8 1GBASE-KX Line Rate, PLL Settings, and Reference Clock Selection

When the TLK10034 is configured to operate in the 1GBASE-KX mode, the available line rates, reference clock frequencies, and corresponding PLL multipliers are summarized in Table 5-2.

Table 5-2. Specific Line Rate and Reference Clock Selection for the 1GBASE-KX Mode

LOW SPEED SIDE					HIGH SPEED SIDE			
Line Rate (Mbps)	SERDES PLL Multiplier	Rate	REFCLKP/N (MHz)		Line Rate (Mbps[1])	SERDES PLL Multiplier	Rate	REFCLKP/N (MHz)
3125[2]	10	Full	156.25		3125[2]	16.5	Full	156.25
3125[2]	5	Full	312.5		3125[2]	8.25	Full	312.5
1250	10	Half	125[2]		1250	20	Quarter	125[2]
1250	8	Half	156.25		1250	16	Quarter	156.25
1250	8	Quarter	312.5		1250	8	Quarter	312.5

(1) High Speed Side SERDES runs at 2x effective data rate.
(2) Manual mode only, as auto negotiate does not support 125Mhz REFCLK or line rate of 3125Mbps. To disable automatic setting of PLL and rate modes, write 1'b1 to bit 13 of register 0x1E.001D.

5.3.2.9 1GBASE-KX Mode Latency

The latency through the TLK10034 in 1G-KX mode is as shown in Figure 5-11. Note that the latency ranges shown indicate static rather than dynamic latency variance, i.e., the range of possible latencies when the serial link is initially established. During normal operation, the latency through the device is fixed.

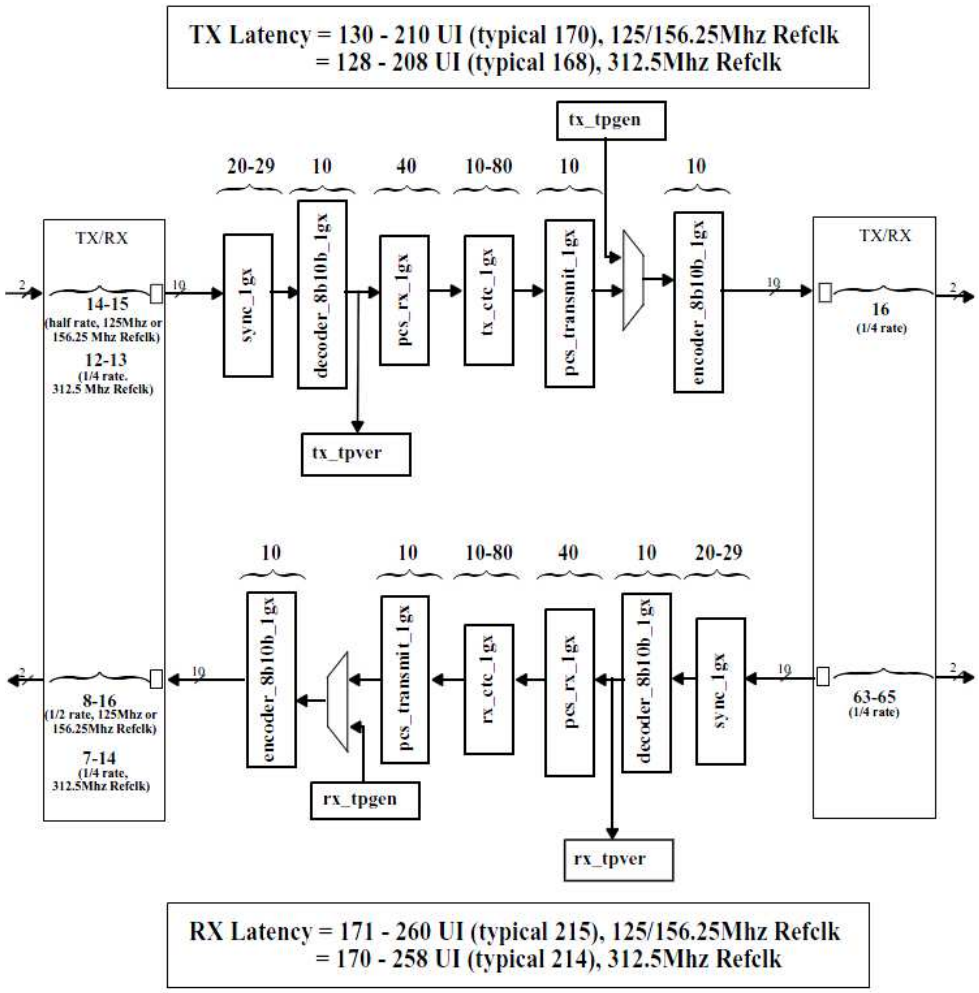


Figure 5-11. 1G-KX Mode Latency

5.3.3 General Purpose (10G) SerDes Mode

5.3.3.1 General Purpose SERDES Transmit Data Path

The TLK10034 General Purpose SERDES low speed to high speed (transmit) data path with the device configured to operate in the normal transceiver (mission) mode is shown in the upper half of Figure 5-33. In this mode, 8B/10B encoded serial data (IN*P/N) in 2 or 4 lanes is received by the low speed side SERDES and deserialized into 10-bit parallel data for each lane. The data in each individual lane is then byte aligned (channel synchronized) and then 8B/10B decoded into 8-bit parallel data for each lane. The lane data is then lane aligned by the Lane Alignment Slave. 32-bits of lane aligned parallel data is subsequently fed into a transmit FIFO which delivers it to an 8B/10B encoder, 16 data bits at a time. The resulting 20-bit 8B/10B encoded parallel data is sent to the high speed side SERDES for serialization and output through the HSTX*P/N pins.

5.3.3.2 General Purpose SERDES Receive Data Path

With the device configured to operate in the normal transceiver (mission) mode, the high speed to low speed (receive) data path is shown in the lower half of Figure 5-33. 8B/10B encoded serial data (HSRX*P/N) is received by the high speed side SERDES and deserialized into 20-bit parallel data. The data is then byte aligned, 8B/10B decoded into 16-bit parallel data, and then delivered to a receive FIFO. The receive FIFO in turn delivers 32-bit parallel data to the Lane Alignment Master which splits the data into the same number of lanes as configured on the transmit data path. The lane data is then 8B/10B encoded and the resulting 10-bit parallel data for each lane is fed into the low speed side SERDES for serialization and output through the OUT*P/N pins. This process is exactly the same for all the channels (A, B, C, and D).

5.3.3.3 Channel Synchronization

As in the 10GBASE-KR mode, the channel synchronization block is used in the 10G General Purpose SERDES mode to align received serial data to a defined byte boundary. The channel synchronization block detects the comma pattern found in the K28.5 character, and follows the synchronization flowchart shown in Figure 5-3.

5.3.3.4 8B/10B Encoder and Decoder

As in the 10GBASE-KR and 1GBASE-KX modes, the 8B/10B encoder and decoder blocks are used to convert between 10-bit (encoded) and 8-bit (unencoded) data words.

5.3.3.5 Lane Alignment Scheme for 8b/10b General Purpose Serdes Mode (Non XAUI Fata, - No /A/)

Lower rate multi-lane serial signals per channel must be byte aligned and lane aligned such that high speed multiplexing (proper reconstruction of higher rate signal) is possible. For that reason, the TLK10034 implements a special lane alignment scheme on the low speed (LS) side for 8b/10b data that does not contain XAUI alignment characters.

During lane alignment, a proprietary pattern (or a custom comma compliant data stream) is sent by the LS transmitter to the LS receiver on each active lane. This pattern allows the LS receiver to both delineate byte boundaries within a lower speed lane and align bytes across the lanes (2 or 4) such that the original higher rate data ordering is restored.

Lane alignment completes successfully when the LS receiver asserts a “Link Status OK” signal monitored by the LS transmitter on the link partner device such as an FPGA. The TLK10034 sends out the “Link Status OK” signals through the LS_OK_OUT_A/B/C/D output pins, and monitors the “Link Status OK” signals from the link partner device through the LS_OK_IN_A/B/C/D input pins. If the link partner device does not need the TLK10034 LAM to send proprietary lane alignment pattern, LS_OK_IN_A/B/C/D can be tied high on the application board or set through MDIO register bits.

The lane alignment scheme is activated under any of the following conditions:

- Device/System power up (after configuration/provisioning)
- Loss of channel synchronization assertion on any enabled LS lane
- Loss of signal assertion on any enabled LS lane
- LS SERDES PLL Lock indication deassertion
- After software determined LS 8B/10B decoder error rate threshold exceeded
- After device reset is deasserted
- Any time the LS receiver deasserts “Link Status OK”.
- Presence of reoccurring higher level / protocol framing errors

All the above conditions are selectable through MDIO register provisioning.

The block diagram of the lane alignment scheme is shown in Figure 5-12.

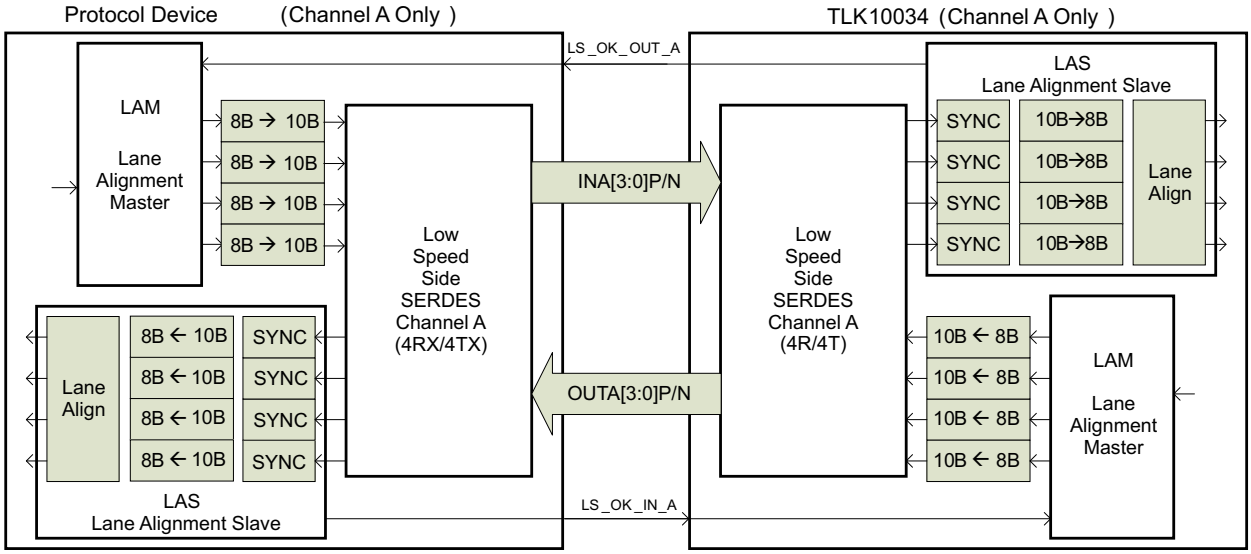


Figure 5-12. Block Diagram of the Lane Alignment Scheme

5.3.3.6 Lane Alignment Components

- Lane Alignment Master (LAM)
  - Responsible for generating proprietary LS lane alignment initialization pattern
  - Resides in the TLK10034 receive path (one instance per channel)
    - Responsible for bringing up LS receive link for the data sent from the TLK10034 to a link partner device
    - Monitors the LS_OK_IN pins for *Link Status OK* signals sent from the Lane Alignment Slave (LAS) of the link partner device
  - Resides in the link partner device (one instance per channel)
    - Responsible for bringing up LS transmit link for the data sent from the link partner device to the TLK10034
    - Monitors the *Link Status OK* signals sent from the LS_OK_OUT pins of the Lane Alignment Slave (LAS) of the TLK10034
- Lane Alignment Slave (LAS)
  - Responsible for monitoring the LS lane alignment initialization pattern
  - Performs channel synchronization per lane (2 or 4 lanes) through byte rotation
  - Performs lane alignment and realignment of bytes across lanes
  - Resides in the TLK10034 transmit path (one instance per channel)
    - Generates the *Link Status OK* signal for the LAM on the link partner device
  - Resides in the link partner device (one instance per channel)
    - Generates the *Link Status OK* signal for the LAM on the TLK10034 device.

5.3.3.7 Lane Alignment Operation (General Purpose Serdes Mode)

During lane alignment, the LAM sends a repeating pattern of 49 characters (control + data) simultaneously across all enabled LS lanes. These simultaneous streams are then encoded by 8B/10B encoders in parallel. The proprietary lane alignment pattern consists of the following characters:

/K28.5/ (CTL=1, Data=0xBC)

Repeat the following sequence of 12 characters four times:

/D30.5/ (CTL=0, Data=0xBE)
/D23.6/ (CTL=0, Data=0xD7)

/D3.1/ (CTL=0, Data=0x23)
/D7.2/ (CTL=0, Data=0x47)
/D11.3/ (CTL=0, Data=0x6B)
/D15.4/ (CTL=0, Data=0x8F)
/D19.5/ (CTL=0, Data=0xB3)
/D20.0/ (CTL=0, Data=0x14)
/D30.2/ (CTL=0, Data=0x5E)
/D27.7/ (CTL=0, Data=0xFB)
/D21.1/ (CTL=0, Data=0x35)
/D25.2/ (CTL=0, Data=0x59)

The above 49-character sequence is repeated until LS_OK_IN is asserted. Once LS_OK_IN is asserted, the LAM resumes transmitting traffic received from the high speed side SERDES immediately.

The TLK10034 performs lane alignment across the lanes similar in fashion to the IEEE 802.3-2008 (XAUI) specification. XAUI only operates across 4 lanes while LAS operates with 2 or 4 lanes. The lane alignment state machine is shown in Figure 5-13. The TLK10034 uses the comma (K28.5) character for lane to lane alignment by default, but can be provisioned to use XAUI's /A/ character as well.

Lane alignment checking is not performed by the LAS after lane alignment is achieved. After LAM detects that the LS_OK_IN signal is asserted, normal system traffic is carried instead of the proprietary lane alignment pattern.

Channel synchronization is performed during lane alignment and normal system operation.

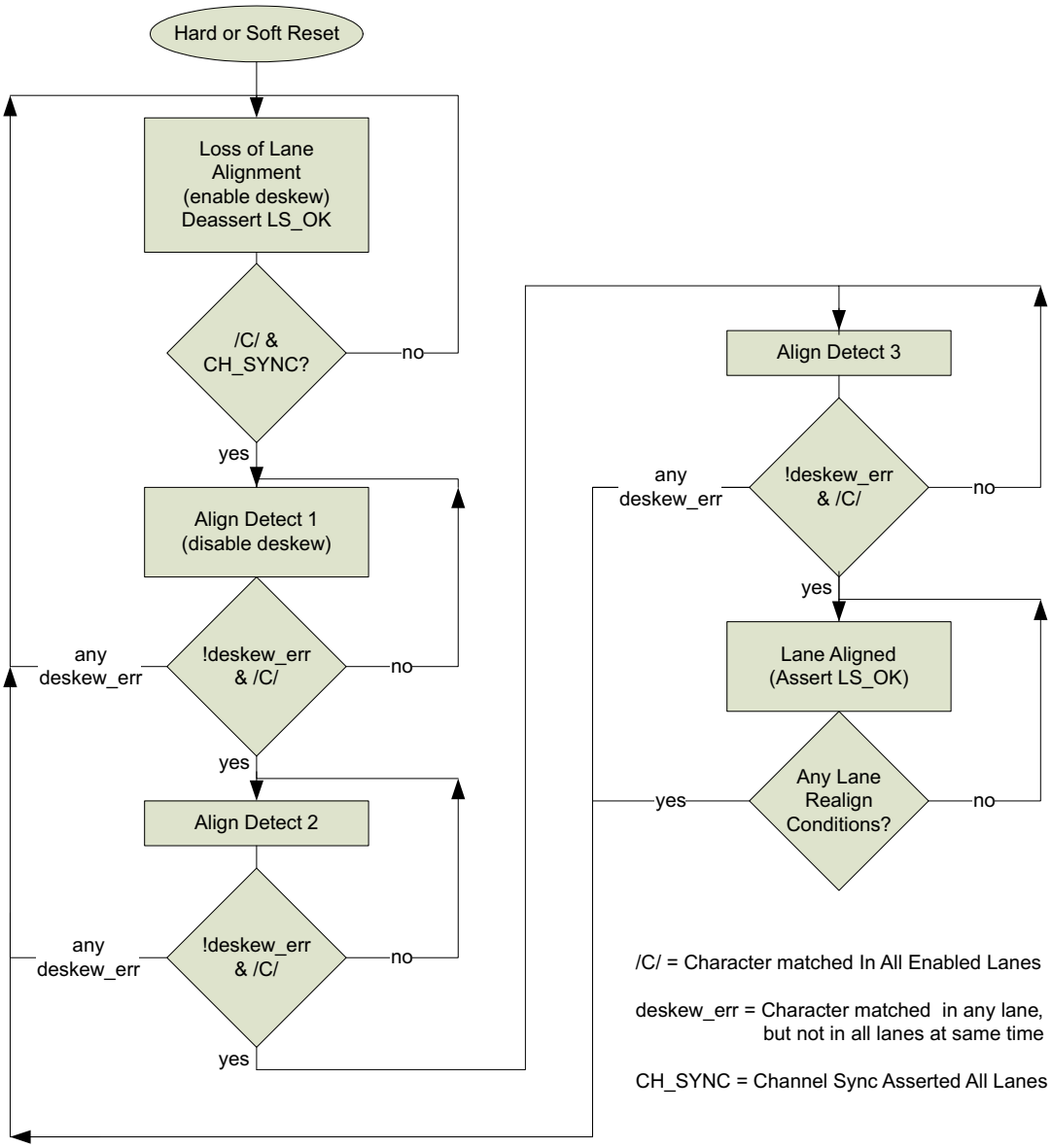


Figure 5-13. Lane Alignment State Machine

5.3.3.8 Line Rate, SERDES PLL Settings, and Reference Clock Selection for the General Purpose SERDES Mode

When the TLK10034 is set to operate in the General Purpose SERDES mode, the following tables show a summary of line rates and reference clock frequencies used for CPRI/OBSAI for 1:1, 2:1 and 4:1 operation modes.

Table 5-3. Specific Line Rate Selection for the 1:1 General Purpose Operation Mode

LOW SPEED SIDE				HIGH SPEED SIDE			
Line Rate (Mbps)	SERDES PLL Multiplier	Rate	REFCLKP/N (MHz)	Line Rate (Mbps)	SERDES PLL Multiplier	Rate	REFCLKP/N (MHz)
4915.2	20	Full	122.88	4915.2	20	Half	122.88
3840	12.5	Full	153.6	3840	12.5	Half	153.6
3125	10	Full	156.25	3125	10	Half	156.25
3125	5	Full	312.5	3125	5	Half	312.5
3072	10	Full	153.6	3072	10	Half	153.6
2457.6	8/10	Full	153.6/122.88	2457.6	16/20	Quarter	153.6/122.88
1920	12.5	Half	153.6	1920	12.5	Quarter	153.6
1536	10	Half	153.6	1536	10	Quarter	153.6
1228.8	8/10	Half	153.6/122.88	1228.8	16/20	Eighth	153.6/122.88

Table 5-4. Specific Line Rate and Reference Clock Selection for the 2:1 General Purpose Operation Mode

LOW SPEED SIDE				HIGH SPEED SIDE			
Line Rate (Mbps)	SERDES PLL Multiplier	Rate	REFCLKP/N (MHz)	Line Rate (Mbps)	SERDES PLL Multiplier	Rate	REFCLKP/N (MHz)
4915.2	20	Full	122.88	9830.4	20	Full	122.88
3840	12.5	Full	153.6	7680	12.5	Full	153.6
3072	10	Full	153.6	6144	10	Full	153.6
2457.6	8/10	Full	153.6/122.88	4915.2	16/20	Half	153.6/122.88
1920	12.5	Half	153.6	3840	12.5	Half	153.6
1536	10	Half	153.6	3072	10	Half	153.6
1228.8	8/10	Half	153.6/122.88	2457.6	16/20	Quarter	153.6/122.88
768	10	Quarter	153.6	1536	10	Quarter	153.6
614.4	8/10	Quarter	153.6/122.88	1228.8	16/20	Eighth	153.6/122.88

Table 5-5. Specific Line Rate and Reference Clock Selection for the 4:1 General Purpose Operation Mode

LOW SPEED SIDE				HIGH SPEED SIDE			
Line Rate (Mbps)	SERDES PLL Multiplier	Rate	REFCLKP/N (MHz)	Line Rate (Mbps)	SERDES PLL Multiplier	Rate	REFCLKP/N (MHz)
2457.6	8/10	Full	153.6/122.88	9830.4	16/20	Full	153.6/122.88
1536	10	Half	153.6	6144	10	Full	153.6
1228.8	8/10	Half	153.6/122.88	4915.2	16/20	Half	153.6/122.88
768	10	Quarter	153.6	3072	10	Half	153.6
614.4	8/10	Quarter	153.6/122.88	2457.6	16/20	Quarter	153.6/122.88

Table 5-3, Table 5-4, and Table 5-5 indicate two possible reference clock frequencies for CPRI/OBSAI applications: 153.6MHz and 122.88MHz, which can be used based on the application preference. The SERDES PLL Multiplier (MPY) has been given for each reference clock frequency respectively. For each channel, the low speed side and the high speed side SERDES use the same reference clock frequency. Note that Channel A, B, C and D are independent and their application rates and references clocks are separate.

For other line rates not shown in Table 5-3, Table 5-4, or Table 5-5, valid reference clock frequencies can be selected with the help of the information provided in Table 5-6 and Table 5-7 for the low speed and high speed side SERDES. The reference clock frequency has to be the same for the two SERDES and must be within the specified valid ranges for different PLL multipliers.

Table 5-6. Line Rate and Reference Clock Frequency Ranges for the Low Speed Side SERDES (General Purpose Mode)

SERDES PLL MULTIPLIER (MPY)	REFERENCE CLOCK (MHz)		FULL RATE (Gbps)		HALF RATE (Gbps)		QUARTER RATE (Gbps)	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
4	250	425	2	3.4	1	1.7	0.5	0.85
5	200	425	2	4.25	1	2.125	0.5	1.0625
6	166.667	416.667	2	5	1	2.5	0.5	1.25
8	125	312.5	2	5	1	2.5	0.5	1.25
10	122.88	250	2.4576	5	1.2288	2.5	0.6144	1.25
12	122.88	208.333	2.94912	5	1.47456	2.5	0.73728	1.25
12.5	122.88	200	3.072	5	1.536	2.5	0.768	1.25
15	122.88	166.667	3.6864	5	1.8432	2.5	0.9216	1.25
20	122.88	125	4.9152	5	2.4576	2.5	1.2288	1.25
RateScale: Full Rate = 0.5, Half Rate = 1, Quarter Rate = 2								

Table 5-7. Line Rate and Reference Clock Frequency Ranges for the High Speed Side SERDES (General Purpose Mode)

SERDES PLL MULTIPLIER (MPY)	REFERENCE CLOCK (MHz)		FULL RATE (Gbps)		HALF RATE (Gbps)		QUARTER RATE (Gbps)		EIGHTH RATE (Gbps)	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
4	375	425	6	6.8	3	3.4	1.5	1.7		
5	300	425	6	8.5	3	4.25	1.5	2.125	1.0	1.0625
6	250	416.667	6	10	3	5	1.5	2.5	1.0	1.25
8	187.5	312.5	6	10	3	5	1.5	2.5	1.0	1.25
10	150	250	6	10	3	5	1.5	2.5	1.0	1.25
12	125	208.333	6	10	3	5	1.5	2.5	1.0	1.25
12.5	153.6	200	7.68	10	3.84	5	1.92	2.5	1.0	1.25
15	122.88	166.667	7.3728	10	3.6864	5	1.8432	2.5	1.0	1.25
16	122.88	156.25	7.86432	10	3.932	5	1.966	2.5	1.0	1.25
20	122.88	125	9.8304	10	4.9152	5	2.4576	2.5	1.2288	1.25
RateScale: Full Rate = 0.25, Half Rate = 0.5, Quarter Rate = 1, Eighth Rate = 2										

For example, in the 2:1 operation mode, if the low speed side line rate is 1.987Gbps, the high-speed side line rate will be 3.974Gbps. The following steps can be taken to make a reference clock frequency selection:

1. Determine the appropriate SERDES rate modes that support the required line rates. Table 5-6 shows that the 1.987Gbps line rate on the low speed side is only supported in the half rate mode (RateScale = 1). Table 5-7 shows that the 3.974Gbps line rate on the high speed side is only supported in the half rate mode (RateScale = 1).
2. For each SERDES side, and for all available PLL multipliers (MPY), compute the corresponding reference clock frequencies using the formula:

   Reference Clock Frequency = (LineRate x RateScale)/MPY

The computed reference clock frequencies are shown in Table 5-8 along with the valid minimum and maximum frequency values.

3. Mark all the common frequencies that appear on both SERDES sides. Note and discard all those that fall outside the allowed range. In this example, the common frequencies are highlighted in Table 5-8. The highest and lowest computed reference clock frequencies must be discarded because they exceed the recommended range.
4. Select any of the remaining marked common reference clock frequencies. Higher reference clock frequencies are generally preferred. In this example, any of the following reference clock frequencies can be selected: 397.4MHz, 331.167MHz, 248.375MHz, 198.7MHz, 165.583MHz, 158.96MHz, and 132.467MHz

Table 5-8. Reference Clock Frequency Selection Example

LOW SPEED SIDE SERDES					HIGH SPEED SIDE SERDES			
SERDES PLL MULTIPLIER	REFERENCE CLOCK FREQUENCY (MHz)				SERDES PLL MULTIPLIER	REFERENCE CLOCK FREQUENCY (MHz)		
	COMPUTED	MIN	MAX			COMPUTED	MIN	MAX
4	~~496.750~~	250	425		4	~~496.750~~	375	425
5	397.400	200	425		5	397.400	300	425
6	331.167	166.667	416.667		6	331.167	250	416.667
8	248.375	125	312.5		8	248.375	187.5	312.5
10	198.700	122.88	250		10	198.700	150	250
12	165.583	122.88	208.333		12	165.583	125	208.333
12.5	158.960	122.88	200		12.5	158.960	153.6	200
15	132.467	122.88	166.667		15	132.467	122.88	166.667
20	~~99.350~~	122.88	125		20	~~99.350~~	122.88	125

5.3.3.9 General Purpose (10G) Loopback Modes

In General Purpose (10G) mode, the TLK10034 supports looping back of data on both the LS (local) side and HS (remote) side. The loopback point can be chosen to be either prior to serialization (shallow) or after serialization (deep). The various loopback modes can be activated and configured through the MDIO interface.

The datapath for deep remote loopback mode is shown in Figure 5-14. The data is accepted on the high speed side receive SERDES pins (HSRX*P/N), traverses the entire receive data path, is returned through the entire transmit data path and sent out through the high speed side transmit SERDES pins (HSTX*P/N). The low speed side outputs on OUT*P/N pins are still available for monitoring and should be correctly terminated. The low speed side inputs on IN*P/N should be electrically idle (floating).

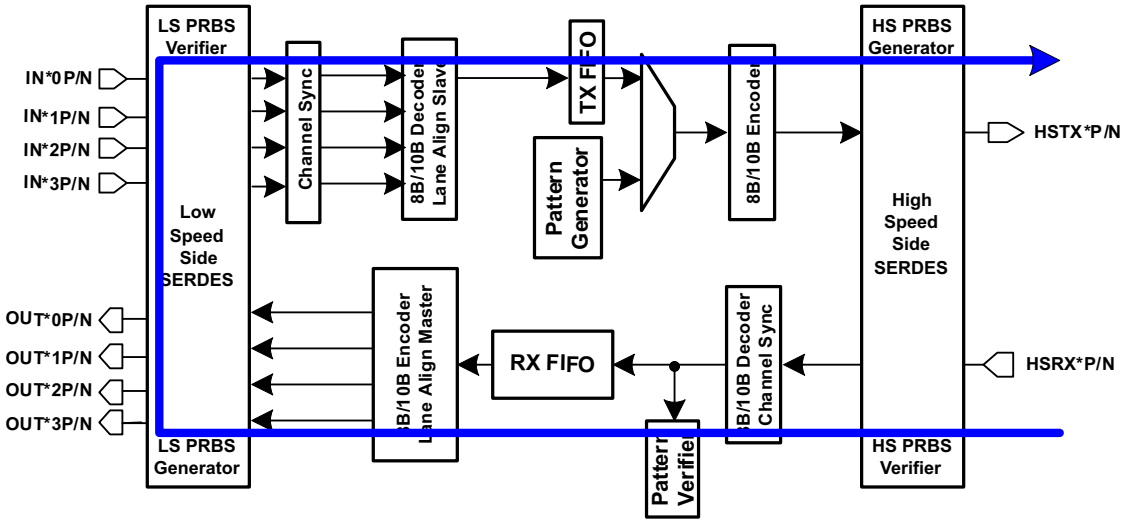


Figure 5-14. Deep Remote Loopback for the General Purpose SERDES Mode

Note that in deep remote loopback mode, the the LS serial transmitter is internally connected directly to the LS serial receiver. This short, low-loss interconnect will have different properties than a typical PCB interconnect, so different transmit and receive link settings should be used to optimize BER.

The datapath for shallow remote loopback mode is shown in Figure 5-15. In this mode, the device functions as a high speed serial retimer. The data is accepted on the high speed side receive SERDES pins (HSRX*P/N), traverses the receive data path up to the LS SERDES, and is looped back through the transmit data path to be sent out through the high speed side transmit SERDES pins (HSTX*P/N).

In shallow remote loopback mode, the low speed side transmit path SERDES can be optionally enabled or disabled, but the PLL needs to be enabled to provide the required clock. The low speed side outputs on OUTA*P/N pins are available for monitoring and must be correctly terminated. The internal LAS's link status is automatically routed to the LAM so that lane alignment can take place.

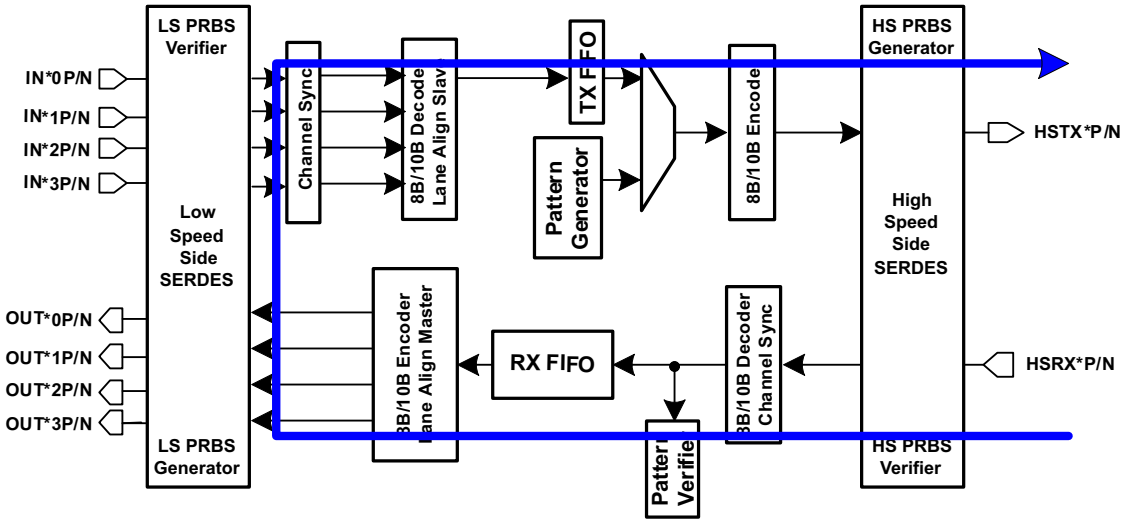


Figure 5-15. Shallow Remote Loopback for the General Purpose SERDES Mode

The datapath for deep local loopback mode is shown in Figure 5-16. Data is accepted on the low speed side SERDES pins (IN*P/N), traverses the entire transmit data path, is returned through the entire receive data path to be sent out through the low speed side receive SERDES pins (OUT*P/N). Note that lane alignment still must occur before passing traffic. The high speed side outputs on the HSTX*P/N pins are available for monitoring. The high speed side inputs on HSRX*P/N should be electrically idle (floating).

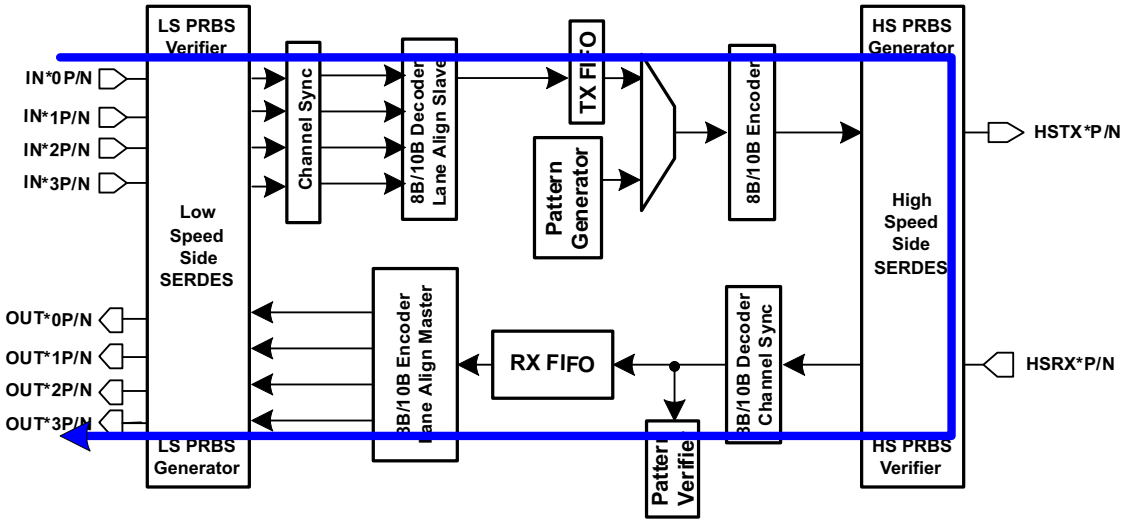


Figure 5-16. Deep Local Loopback for the General Purpose SERDES Mode

Note that in deep local loopback mode, the the HS serial transmitter is internally connected directly to the HS serial receiver. This short, low-loss interconnect will have different properties than a typical PCB interconnect, so different transmit and receive link settings should be used to optimize BER.

In shallow local loopback mode, the data is accepted on the low speed side SERDES pins (IN*P/N), traverses the transmit data path up to the HS SERDES, is looped back before through the receive data path, and sent out through the low speed side receive SERDES pins (OUT*P/N). The high speed side outputs on HSRX*P/N pins are available for monitoring.

5.3.3.10 General Purpose (10G) Latency Measurement Function

The TLK10034 includes a latency measurement function to support CPRI and OBSAI type applications. There are two start and two stop locations for the latency counter as shown in Figure 5-17 for Channel A. The start and stop locations are selectable through MDIO register bits. The elapsed time from a comma detected at an assigned counter start location of a particular channel to a comma detected at an assigned counter stop location of the same channel is measured and reported through the MDIO interface. The function may operate independently on each channel. The following three control characters (containing commas) are monitored:

1. K28.1 (control = 1, data = 0x3C)
2. K28.5 (control = 1, data = 0xBC)
3. K28.7 (control = 1, data = 0xFC).

The first comma found at the assigned counter start location will start up the latency counter. The first comma detected at the assigned counter stop location will stop the latency counter. The 20-bit latency counter result of this measurement is readable through the MDIO interface. The accuracy of the measurement is a function of the serial bit rate at which the channel being measured is operating. The register will return a value of 0xFFFFF if the duration between transmit and receive comma detection exceeds the depth of the counter. Only one measurement value is stored internally until the 20-bit results counter is read. The counter will return zero in cases where a transmit comma was never detected (indicating the results counter never began counting).

It is also possible to start and stop the counter using the PRTAD1 pin. This allows the stopwatch circuit to be triggered from an external device such as the low speed side link partner.

For a detailed description of the latency measurement procedure, please refer to the application note *TLK10034 Latency Measurement Function*.

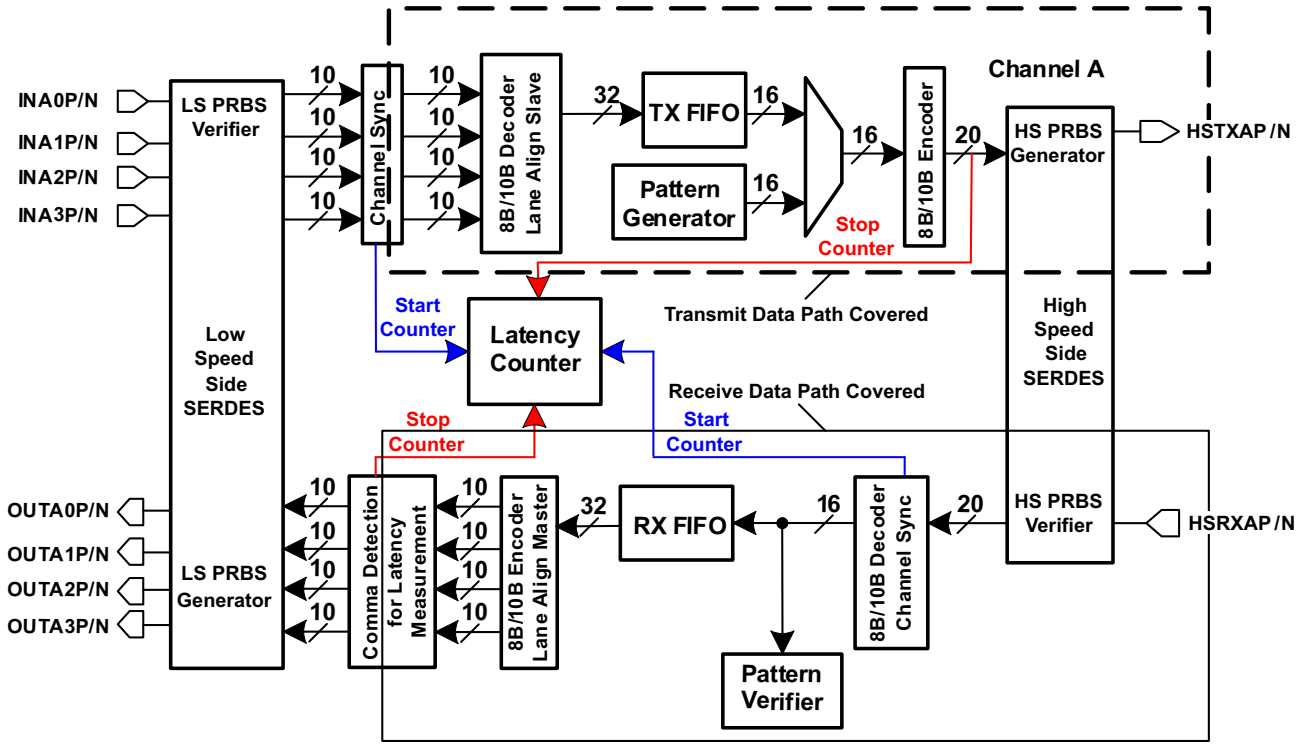


Figure 5-17. Location of TX and RX Comma Character Detection (Only Channel A Shown)

In high speed side SERDES full rate mode, the latency measurement function runs off of an internal clock which is equal to the frequency of the transmit serial bit rate divided by 8. In half rate mode, the latency measurement function runs off of an internal clock which is equal to the serial bit rate divided by 4. In quarter rate mode, the latency measurement function runs off of an internal clock which is equal to the serial bit rate divided by 2. In eighth rate mode, the latency measurement function runs off of a clock which is equal to the serial bit rate.

The latency measurement does not include the low speed side transmit SERDES contribution as well as part of the channel synchronization block. The latency introduced by those two is up to (18 + 10) x N high speed side unit intervals (UIs), where N = 2, 4 is the multiplex factor. The latency measurement also doesn't account for the low speed side receive SERDES contribution which is estimated to be up to 20 x N high speed side UIs.

The latency measurement accuracy in all cases is equal to plus or minus one latency measurement clock period. The measurement clock can be divided down if a longer duration measurement is required, in which case the accuracy of the measurement is accordingly reduced. The high speed latency measurement clock is divided by either 1, 2, 4, or 8 via register settings. The measurement clock used is always selected by the channel under test. The high speed latency measurement clock may only be used when operating at one of the serial rates specified in the CPRI/OBSAI specifications. It is also possible to run the latency measurement function off of the recovered byte clock for the channel under test (giving a latency measurement clock frequency equal to the serial bit rate divided by 20).

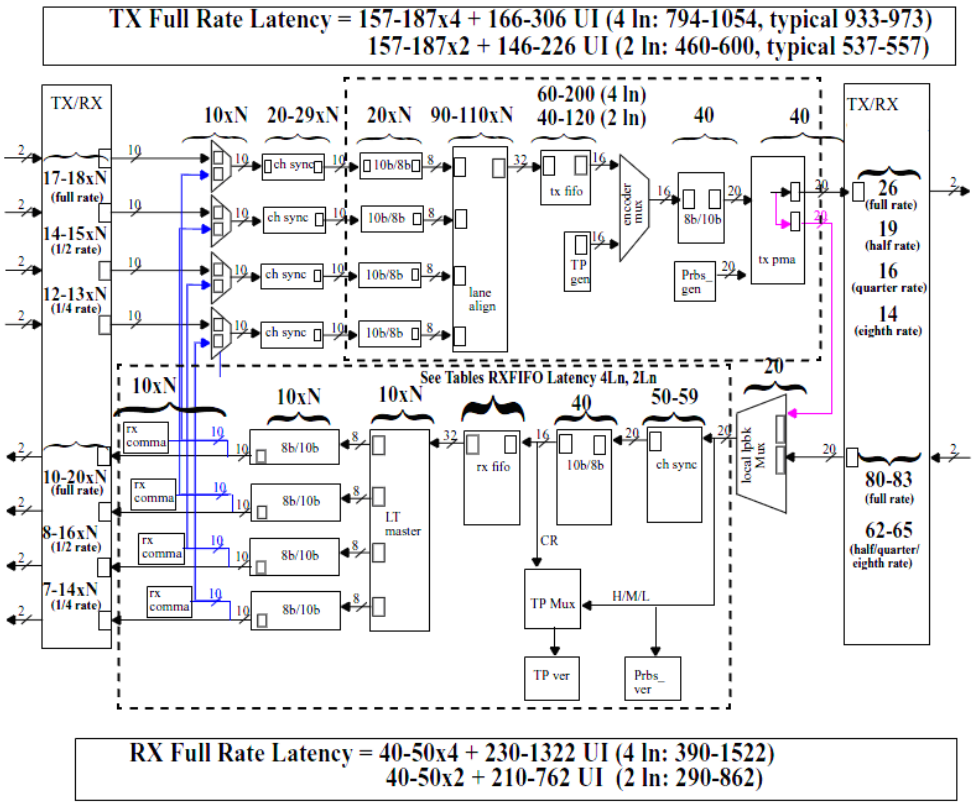
The accuracy for the standard based CPRI/OBSAI application rates is shown in Table 5-9, and assumes the latency measurement clock is not divided down per user selection (division is required to measure a duration greater than 682us). For each division of 2 in the measurement clock, the accuracy is also reduced by a factor of two.

Table 5-9. CPRI/OBSAI Latency Measurement Function Accuracy (Undivided Measurement Clock)

LINE RATE (Gbps)	RATE	LATENCY CLOCK FREQUENCY (GHz)	ACCURACY (± ns)
1.2288	Eighth	1.2288	0.8138
1.536	Quarter	0.768	1.302
2.4576	Quarter	1.2288	0.8138
3.072	Half	0.768	1.302
3.84	Half	0.96	1.0417
4.9152	Half	1.2288	0.8138
6.144	Full	0.768	1.302
7.68	Full	0.96	1.0417
9.8304	Full	1.2288	0.8138

5.3.3.11 General Purpose (10G) Mode Latency

The latency through the TLK10034 in general purpose (10G) mode is as shown in Figure 5-18. Note that the latency ranges shown indicate static rather than dynamic latency variance, i.e., the range of possible latencies when the serial link is initially established. During normal operation, the latency through the device is fixed.



NOTE: Latency numbers represent no external skew between lanes. External lane skew will increase overall latency. TX Datapath latency includes 20xN UI of variance due to deserialization and channel sync.

Figure 5-18. General Purpose Mode Latency

Table 5-10. RX FIFO Latency in 4LN Mode

RX FIFO TYPE	FIFO_DEPTH_SEL	MIN LATENCY (UI)	MAX LATENCY (UI)
REGULAR FIFO (No CTC)	4	100	220
RATE MATCH FIFO (No CTC)	8	40	280
RATE MATCH FIFO (With CTC)	12	120	360
	16	120	520
	24	160	800
	32	160	1120

Table 5-11. RX FIFO Latency in 2LN Mode

RX FIFO TYPE	FIFO_DEPTH_SEL	MIN LATENCY (UI)	MAX LATENCY (UI)
REGULAR FIFO (No CTC)	4	40	100
RATE MATCH FIFO (No CTC)	8	20	140
RATE MATCH FIFO(With CTC	12	60	180
	16	60	260
	24	80	400
	32	80	560

5.3.3.12 TLK10034 Clocks: REFCLK, CLKOUT

5.3.3.12.1 General Information

The TLK10034 device requires a low-jitter reference clock to work. The reference clock can be provided on the REFCLK0P/N or REFCLK1P/N pins. Both reference clock input pins have internal 100-Ω differential terminations, so they do not need any external terminations. Both reference clock inputs must be AC-coupled with preferably 0.1-uF capacitors. The two channels (A and B) can have same or different reference clocks. Refer to the TLK10034 datasheet for more information on reference clock selection and jitter requirements.

The TLK10034 serial receiver recovers clock and data from the incoming serial data. The recovered byte clock is made available on the CLKOUTAP/N and/or CLKOUTBP/N pins. The CLKOUTxP/N CML output pins must be AC-coupled with 0.1-uF AC-coupling capacitors.

5.3.3.13 TLK10034 Control Pins and Interfaces

The TLK10034 device features a number of control pins and interfaces, some of which are described below.

5.3.3.14 MDIO Interface

The TLK10034 supports the Management Data Input/Output (MDIO) Interface as defined in Clause 22 of the IEEE 802.3 Ethernet specification. The MDIO allows register-based management and control of the serial links.

The MDIO Management Interface consists of a bi-directional data path (MDIO) and a clock reference (MDC). The port address is determined by the PRTAD[4:0] control pins.

The MDIO pin requires a pullup to VDDO[1:0]. No pullup is needed on the MDC pin if driven with a push-pull MDIO master, but a pullup to VDDO[1:0] is needed if driven with an open-drain MDIO master.

5.3.3.15 JTAG Interface

The JTAG interface is mostly used for device test. The JTAG interface operates through the TDI, TDO, TMS, TCK, and TRST_N pins. If not used, all the pins can be left unconnected except TDI and TCK which have to be grounded.

5.3.3.16 Unused Pins

As a general guideline, any unused LVCMOS input pin needs to be grounded and any unused LVCMOS output pin can be left unconnected. Unused CML differential output pins can be left unconnected. Unused CML differential input pins should be tied to ground through a shared 100-Ω resistor.

5.3.4 Provisionable XAUI Clock Tolerance Compensation

The XAUI interface is defined to allow for separate clock domains on each side of the link. Though the reference clocks for two devices on a XAUI/KR link have the same specified frequencies, there are slight differences that, if not compensated for, will lead to over or under run of the FIFOs on the receive/transmit data paths.

The XAUI CTC block performs the clock domain transition and rate compensation by utilizing a FIFO that is 32 deep and 40-bits wide. The usable FIFO size in the RX and TX directions is dependent upon the RX_FIFO_DEPTH and TX_FIFO_DEPTH MDIO fields, respectively. The word format is illustrated in Figure 5-19.

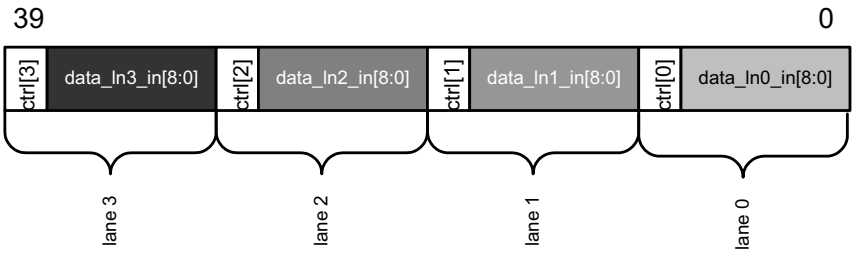


Figure 5-19. XAUI CTC FIFO Word Format

The XAUI CTC performs one of the following operations to compensate the clock rate difference:

1. Delete Idle column from the data stream
2. Delete Sequence column from the data stream (enabled via MDIO)
3. Insert Idle column to the data stream.

The following rules apply for insertion/removal:

- Idle insertion/deletion occurs in groups of 4 idle characters (i.e., in columns)
- Idle characters are added following Idle or Sequence ordered_set
- Idle characters are not added while data is being received
- When deleting Idle characters, minimum IPG of 5 characters is maintained. /T/ characters are counted towards IPG.
- The first Idle column after /T/ is never deleted
- Sequence ordered_sets are deleted only when two consecutive Sequence columns are received. In this case, only one of the two Sequence columns will be deleted.

Insertion: When the FIFO fill level is ***at or below LOW watermark (insertion is triggered)***, the XAUI CTC needs to insert an IDLE column. It does so by skipping a read from the FIFO and inserting IDLE column to the data stream. It continues the insertion until the FIFO fill level is above the mid point. This occurs on the read side of the FIFO.

Removal: When the FIFO fill level is ***at or above HIGH watermark (deletion is triggered),*** the XAUI CTC needs to remove an IDLE column. It does so by skipping a write to the FIFO and discarding the IDLE column or Sequence ordered_set. It continues the deletion until the FIFO fill level is below the mid point. This occurs on the write side of the FIFO.

On the write side of the XAUI CTC FIFO a 40-bit write is performed at every cycle of the 312.5 MHz clock except during removal when it discards the IDLE or sequence ordered_set. On the read side of the XAUI CTC FIFO a 40-bit read is performed at every cycle of the 312.5 MHz clock except during insertion when it generates IDLE columns to the output while not reading the FIFO at all.

In IEEE 802.3ae the XAUI clock rate tolerance is given as 3.125 GHz ± 100 ppm, the XGMII clock rate tolerance is given as 156.25 MHz ± 0.02% (which is equivalent to 200ppm), and the Jumbo packet size is 9600 bytes which is equivalent to 2400 cycles of 312.5 MHz clock. The average inter-frame gap is 12 bytes (3 columns), which implies that there is one opportunity to insert/delete a column in between every packet on average. This gives one column deletion/insertion in every 2400 columns which results in a 400 ppm tolerance capability. If the IPG increases, then more clock rate variance or larger packet size can be supported. Note that the maximum frequency tolerance is limited by the frequency accuracy requirement of the reference clock.

The number of words in the FIFO (fifo_depth[2:0]) and the HIGH/LOW watermark levels (wmk_sel[1:0]) are set through MDIO register 1.32769, and determine the allowable difference between the write clock and the read clock as well as the maximum packet size that can be processed without FIFO collision. At these watermarks the drop and insert start respectively and must happen before it hits overflow/underflow condition. Although the FIFO is supposed to never overflow/underflow given the average IPG, if it ever happens the overflow/underflow indications signal the error to the MDIO interface and the FIFO is reset. Note that the overflow/underflow status indications are latched high and cleared when read.

Table 5-12Thshows XAUI CTC FIFO configuration and capabilities:

Table 5-12. XAUI CTC FIFO Configurations

fifo_depth[2:0]	FIFO Depth	wmk_sel[1:0]	LOW Watermark	HIGH Watermark	Max Latency (Cycles)	Nom Latency (Cycles)	Min Latency (Cycles)	Max pkt size (400ppm)	Max pkt size (200ppm)	Max pkt size (100ppm)	Max pkt size (50ppm)	Min #of removable columns in IPG to support the max pkt size	
1xx	32	11	15	18	28	16	4	100KB	200KB	400KB	800KB	10	default
		10	13	20	28	16	4	80KB	160KB	320KB	640KB	8	
		01	10	23	28	16	4	50KB	100KB	200KB	400KB	5	
		00	6	27	28	16	4	10KB	20KB	40KB	80KB	1	
011	24	11	11	14	20	12	4	60KB	120KB	240KB	480KB	6	
		10	9	16	20	12	4	40KB	80KB	160KB	320KB	4	
		0x	6	19	20	12	4	10KB	20KB	40KB	80KB	1	
010	16	1x	7	10	13	8	3	30KB	60KB	120KB	240KB	3	
		0x	5	12	13	8	3	10KB	20KB	40KB	80KB	1	
001	12	xx	5	8	9	6	3	10KB	20KB	40KB	80KB	1	
000	8	Plain FIFO, No CTC			7	4	1	No limit on pkt size (needs 0 ppm to work)					

NOTE

To support the max packet sizes as shown in Table 5-12, it is assumed that there are enough IDLE columns in IPG for deletion. Below is one example:

Configure the FIFO to be 32-deep (fifo_depth[2:0] = 3'b1xx) and set the LOW/HIGH Watermarks to 10/23 (wmk_sel[1:0] = 2'b01). If the write clock is faster than the read clock by 200ppm, to support the max packet size of 100KB, a minimum of 5 removable columns in IPG is required (either IDLE columns or Sequence ordered_sets). If there are only 4 removable columns in IPG, the max packet size supported is dropped to 80KB. If there are only 3 removable columns in IPG, the max packet size supported is dropped to 60KB, and so on. As a rule of thumb, one removable column in IPG corresponds to 10KB at 400ppm, 20KB at 200ppm, 40KB at 100ppm, and 80KB at 50ppm

Figure 5-20 through Figure 5-30 illustrate XAUI CTC FIFO configuration and capabilities. The green region (the middle of the FIFO fill level) indicates that the FIFO is operating stably without insertion or deletion. The more green bars in the figure, the more clock wander it can tolerate. The more yellow bars in the figure, the bigger packet size it can support.

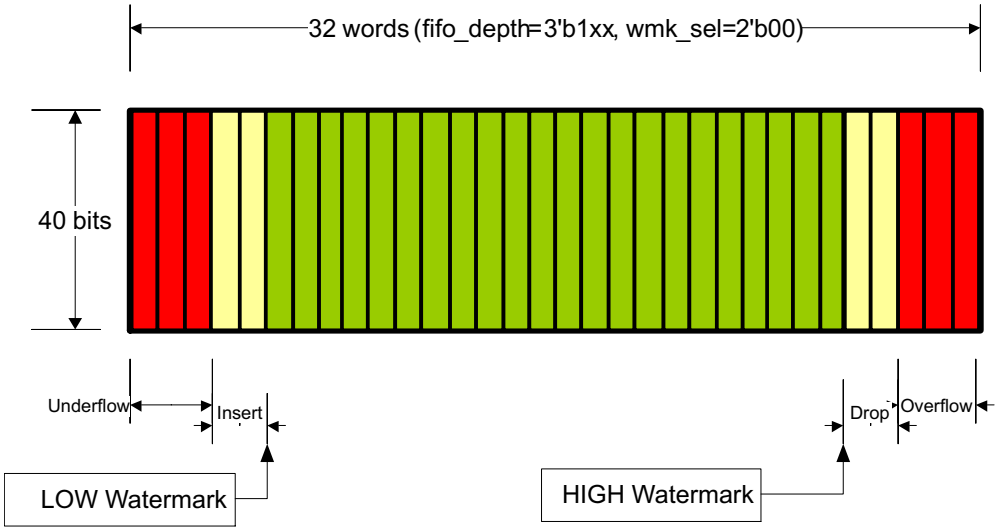


Figure 5-20. Organization of the XAUI CTC FIFO (32-Deep, Low Watermark)

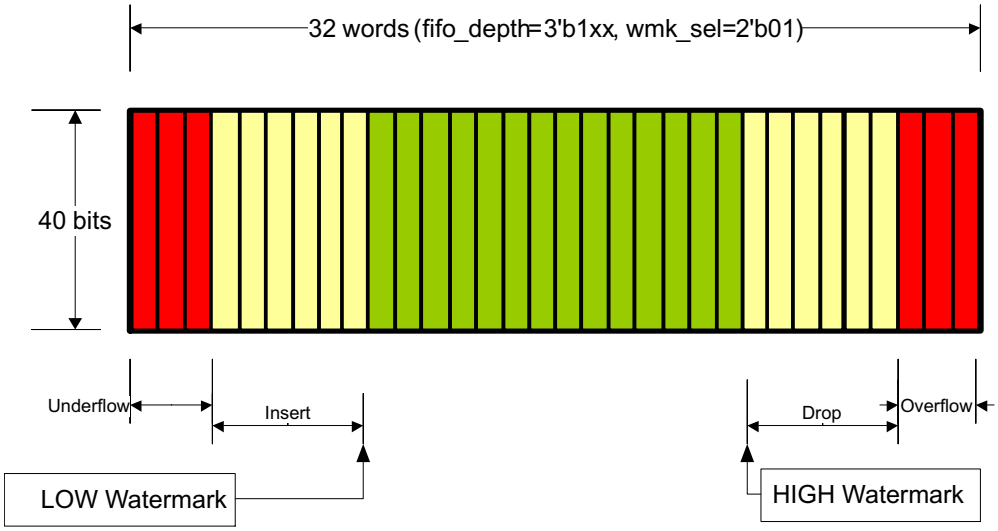


Figure 5-21. Organization of the XAUI CTC FIFO (32-Deep, Mid Watermark)

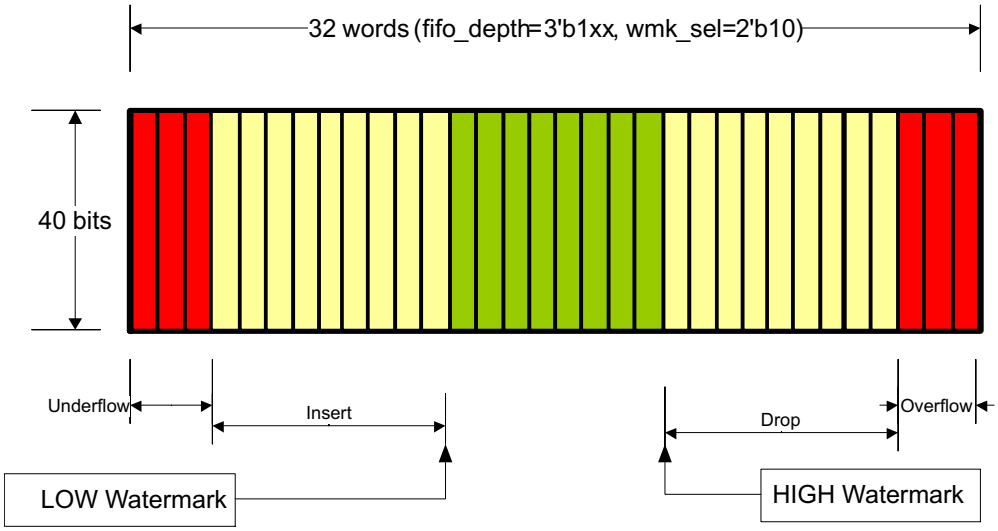


Figure 5-22. Organization of the XAUI CTC FIFO (32-Deep, Mid-High Watermark)

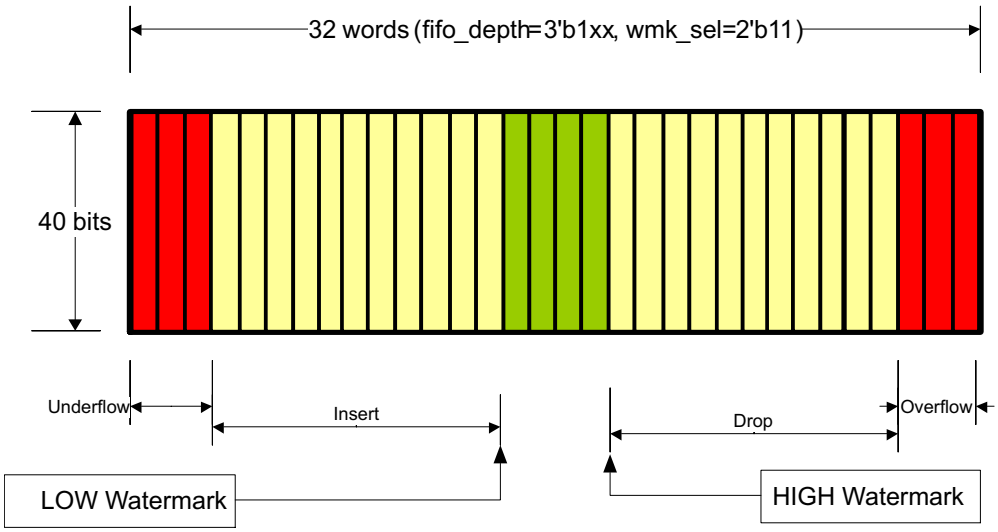


Figure 5-23. Organization of the XAUI CTC FIFO (32-Deep, High Watermark)

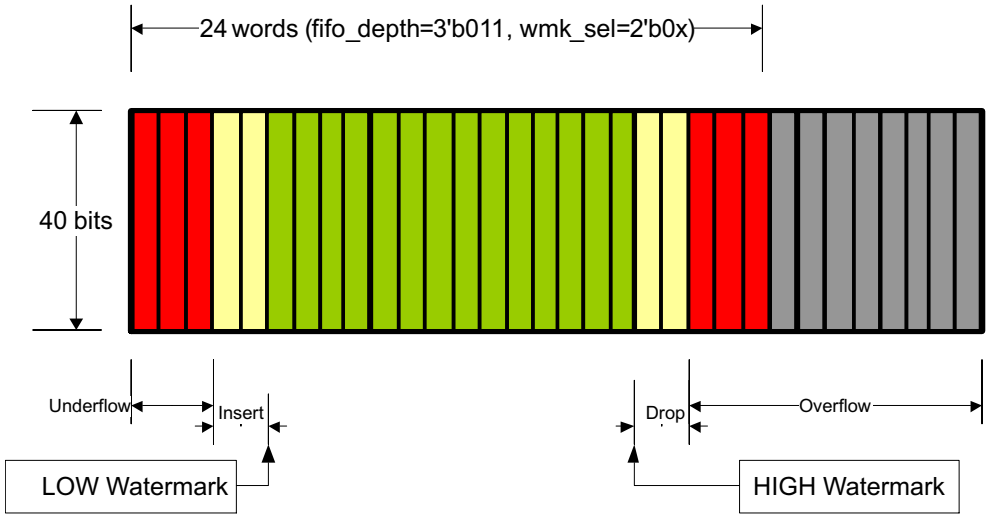


Figure 5-24. Organization of the XAUI CTC FIFO (24-Deep, Low Watermark)

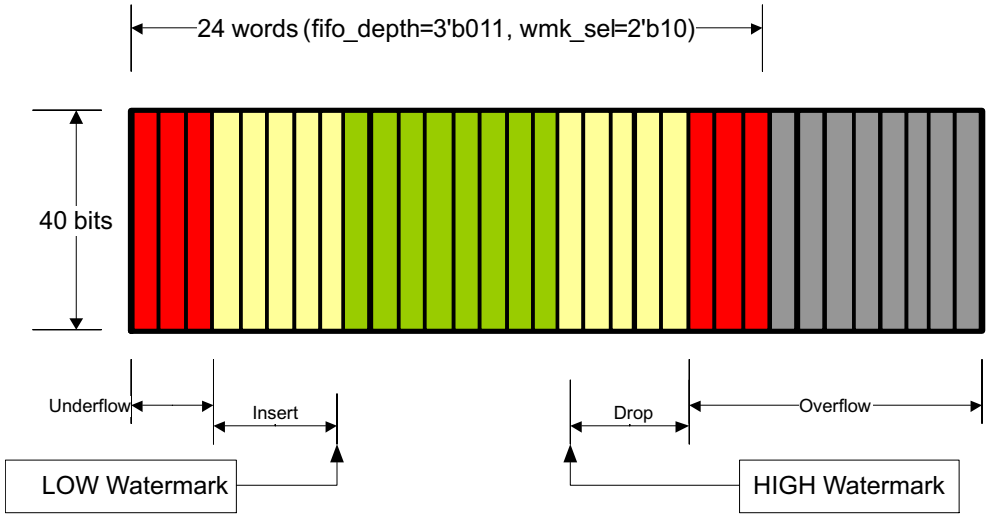


Figure 5-25. Organization of the XAUI CTC FIFO (24-Deep, Mid Watermark)

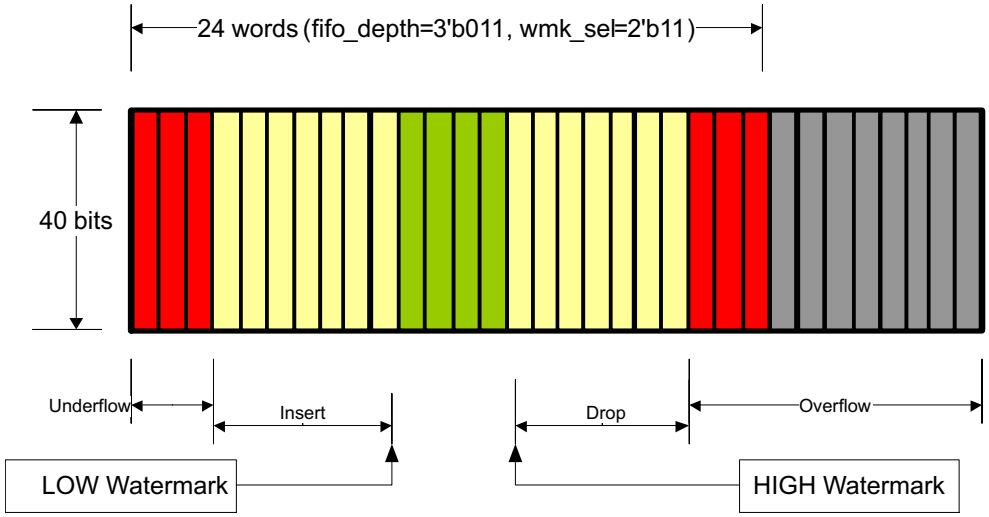


Figure 5-26. Organization of the XAUI CTC FIFO (24-Deep, High Watermark)

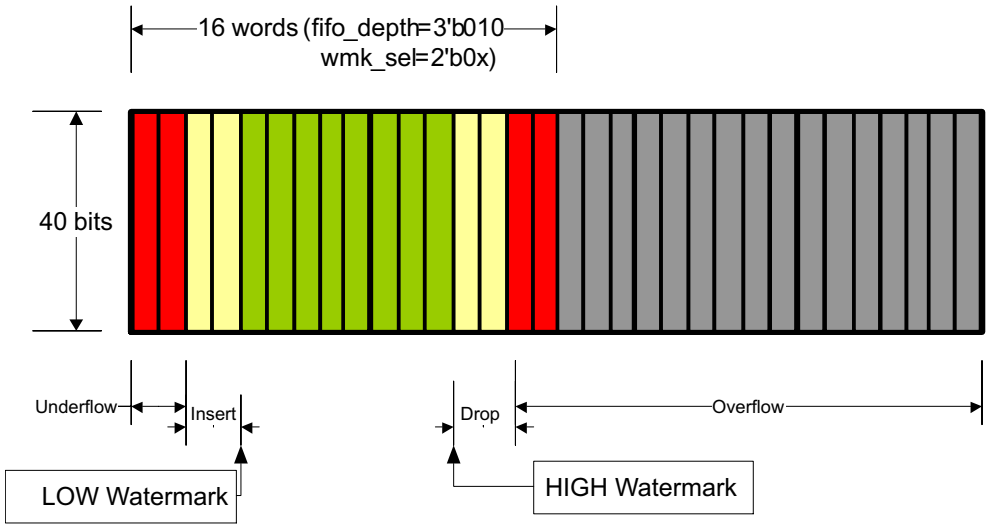


Figure 5-27. Organization of the XAUI CTC FIFO (16-Deep, Low Watermark)

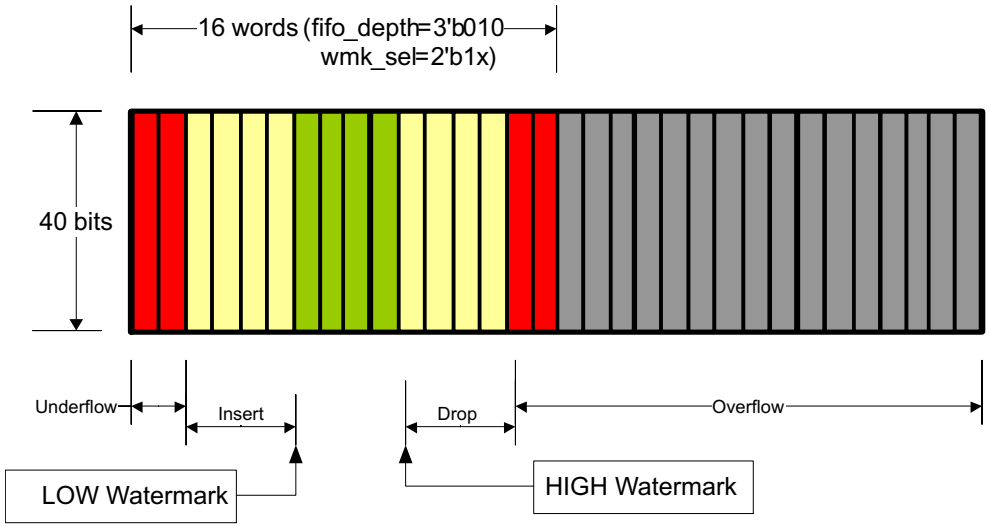


Figure 5-28. Organization of the XAUI CTC FIFO (16-Deep, High Watermark)

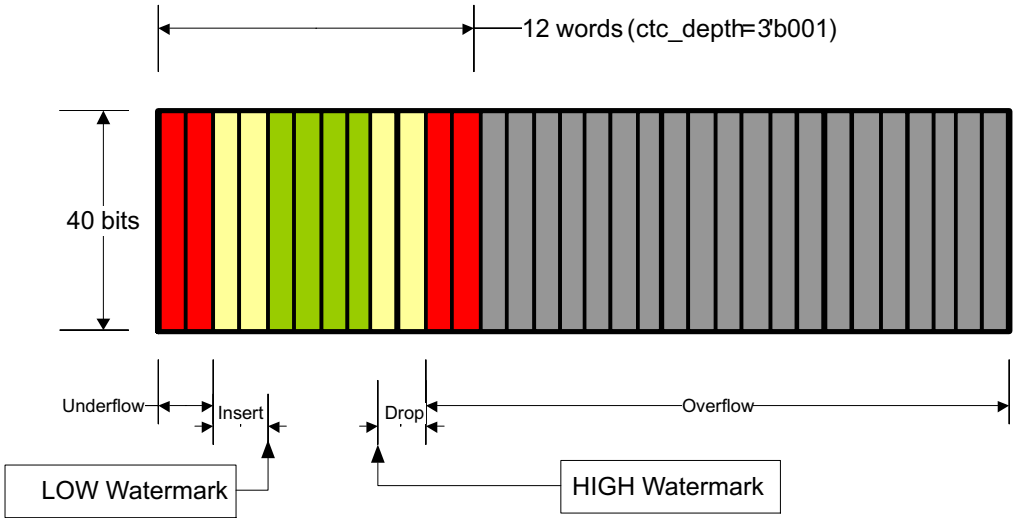


Figure 5-29. Organization of the XAUI CTC FIFO (12-Deep)

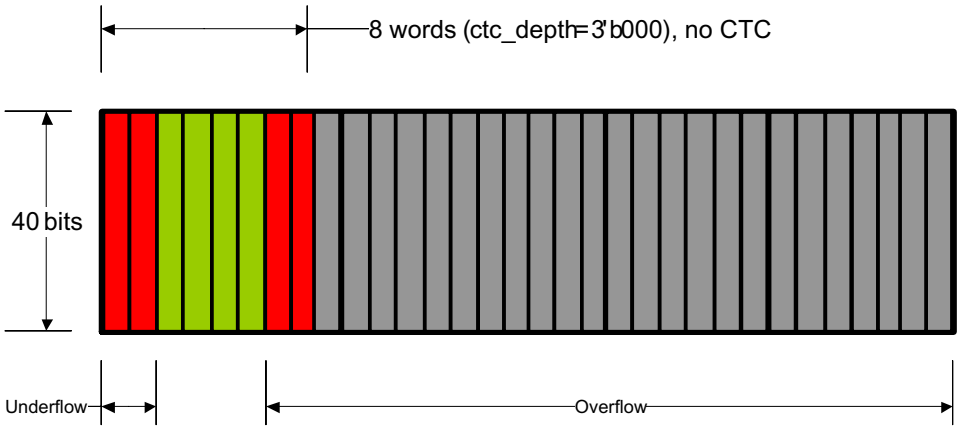


Figure 5-30. Organization of the XAUI CTC FIFO (8-Deep)

5.4 Device Functional Modes

5.4.1 Operating Modes

The TLK10034 is a versatile high-speed transceiver device that is designed to perform various physical layer functions in three operating modes: 10GBASE-KR Mode, 1G-KX Mode, and General Purpose (10G) SERDES Mode. The three modes are described in three separate sections. The device operating mode is determined by the MODE_SEL and ST pin settings, as well as bit MDIO bit 30.1.10.

Table 5-13. TLK10034 Operating Mode Selection

	ST = 0 (Clause 45)	ST = 1 (Clause 22)
{MODE_SEL pin, SW bit (30.1.10)}		
1x	10G	10G
01	10G	10G
00	10G-KR/1G-KX (Determined by Auto Neg)	1G-KX (No Auto Neg)

5.4.2 10GBASE-KR Mode

A simplified block diagram of the transmit and receive data paths in 10GBASE-KR mode is shown in Figure 5-31. This section gives a high-level overview of how data moves through these paths, then gives a more detailed description of each block's functionality.

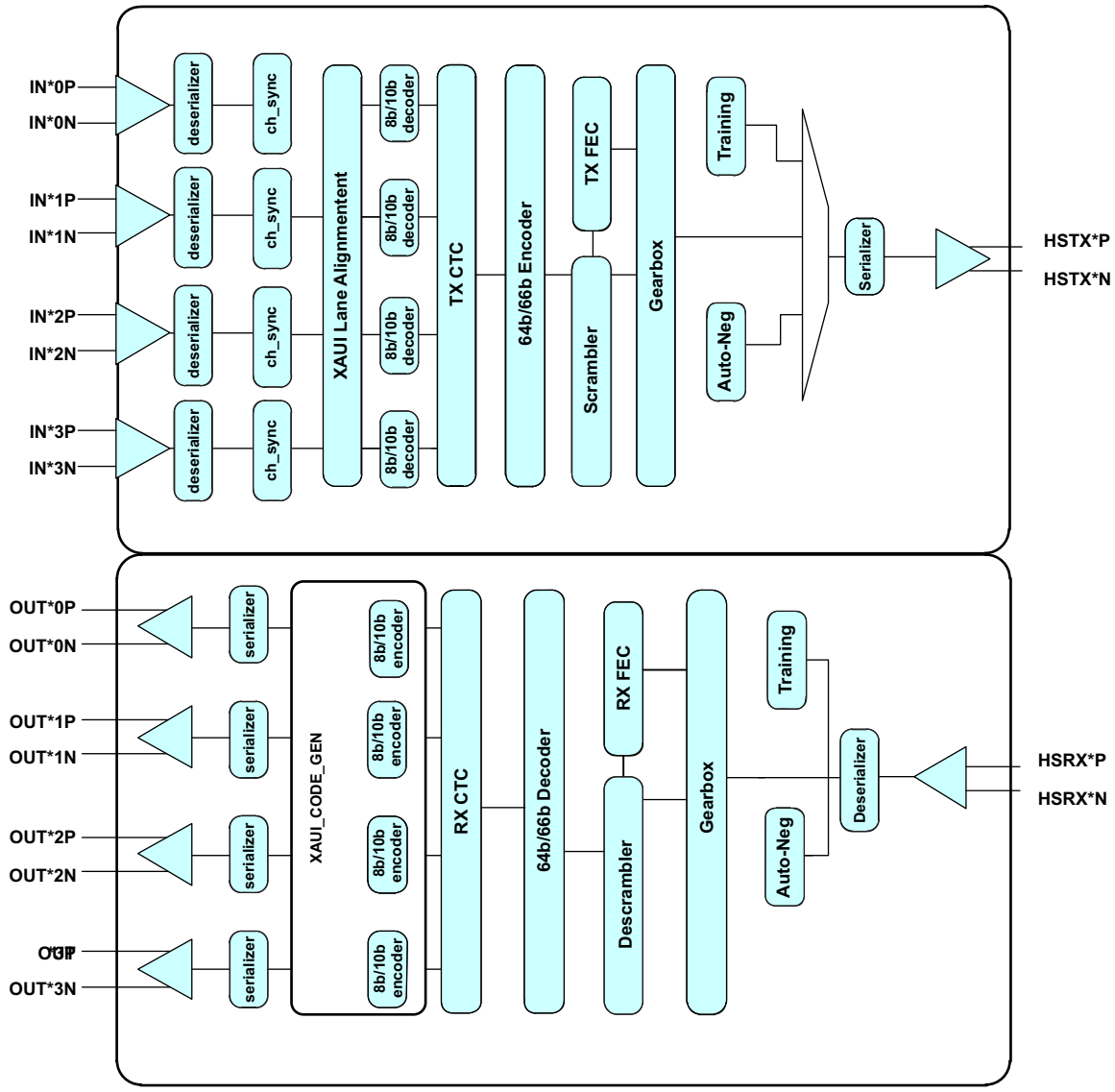


Figure 5-31. A Simplified One Channel KR Data Path Block Diagram

5.4.3 1GBASE-KX Mode

A simplified block diagram of the 1GBASE-KX data path is shown in Figure 5-32.

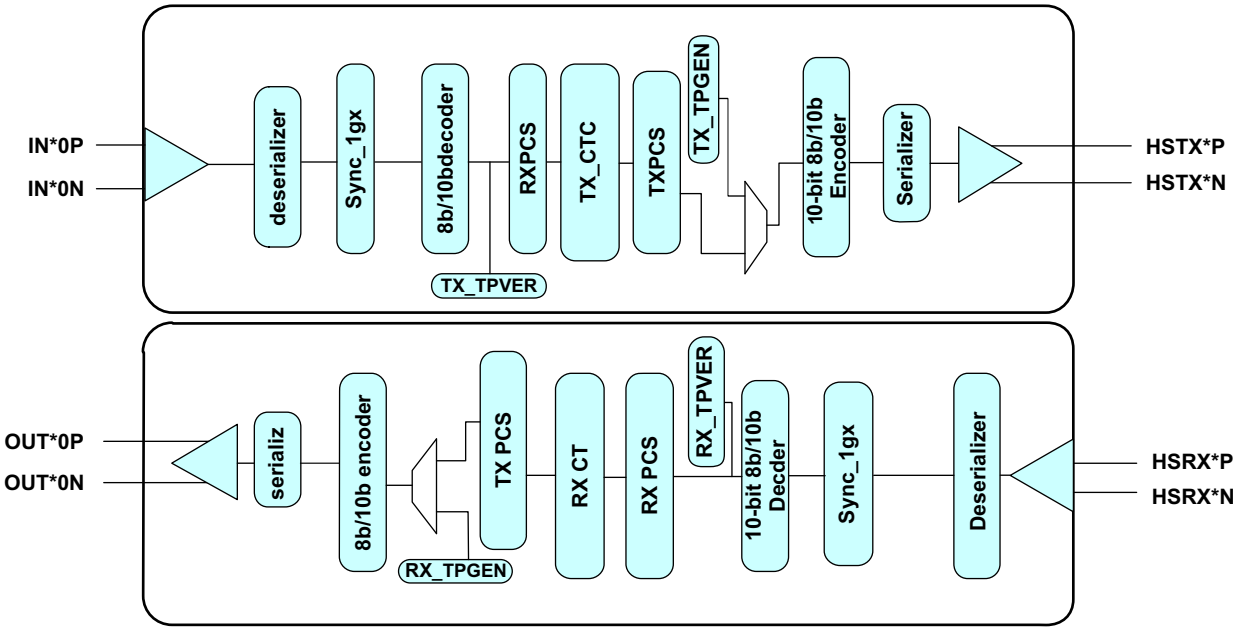


Figure 5-32. A Simplified One Channel Block Diagram of the 1GKX Data Path

5.4.4 General Purpose (10G) SerDes Mode

A block diagram showing the transmit and receive data paths of the TLK10034 operating in General Purpose (10G) SerDes mode is shown in Figure 5-33.

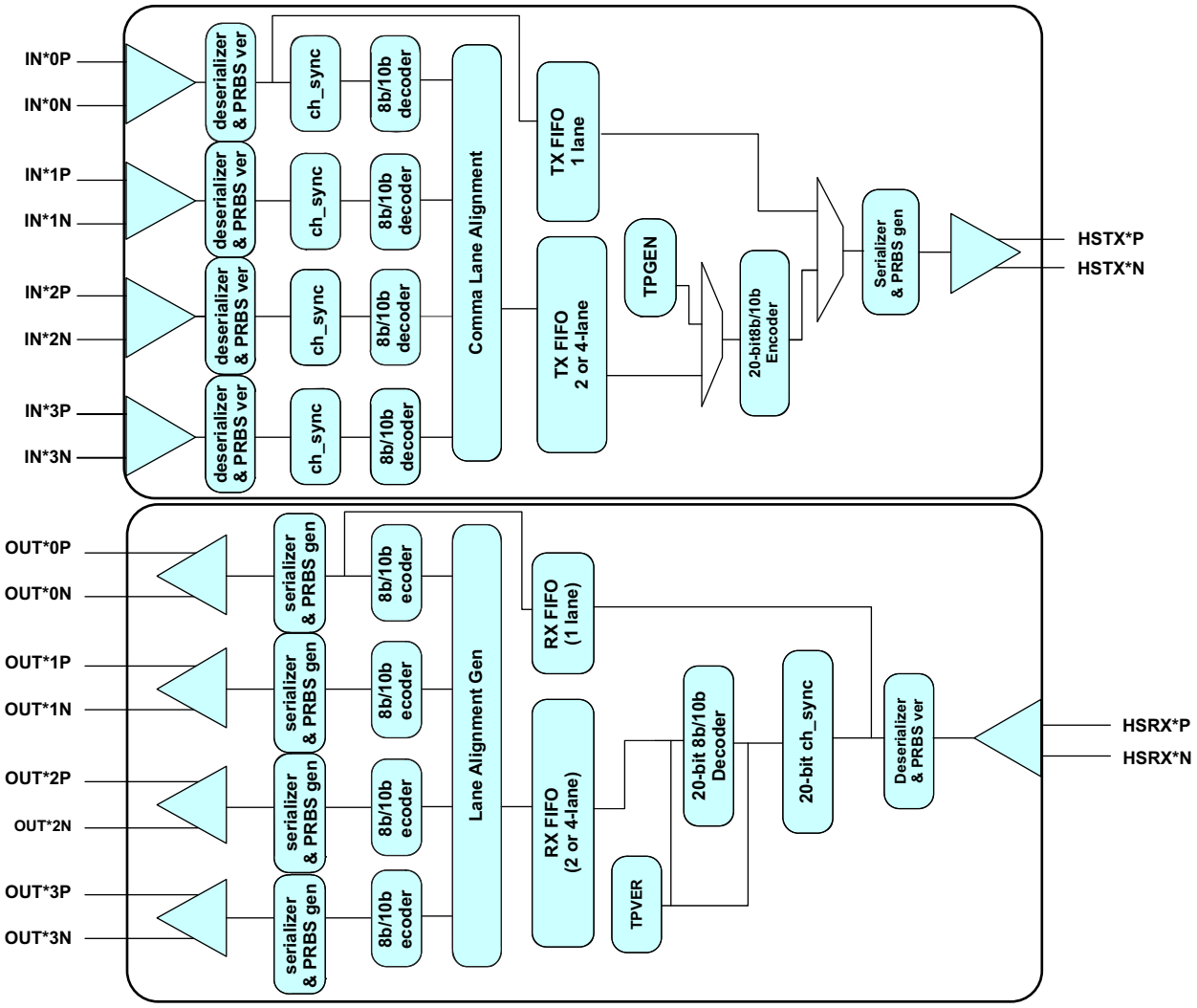


Figure 5-33. Block Diagram Showing General Purpose SerDes Mode

5.5 Memory

5.5.1 Clocking Architecture (All Modes)

A simplified clocking architecture for the TLK10034 is captured in Figure 5-34. Each channel has an option of operating with a differential reference clock provided either on pins REFCLK0P/N or REFCLK1P/N. The choice is made either through MDIO or through REFCLK_SEL pins. The reference clock frequencies for each channel can be chosen independently. For each channel, the low speed side SERDES, high speed side SERDES and the associated part of the digital core operate from the same reference clock.

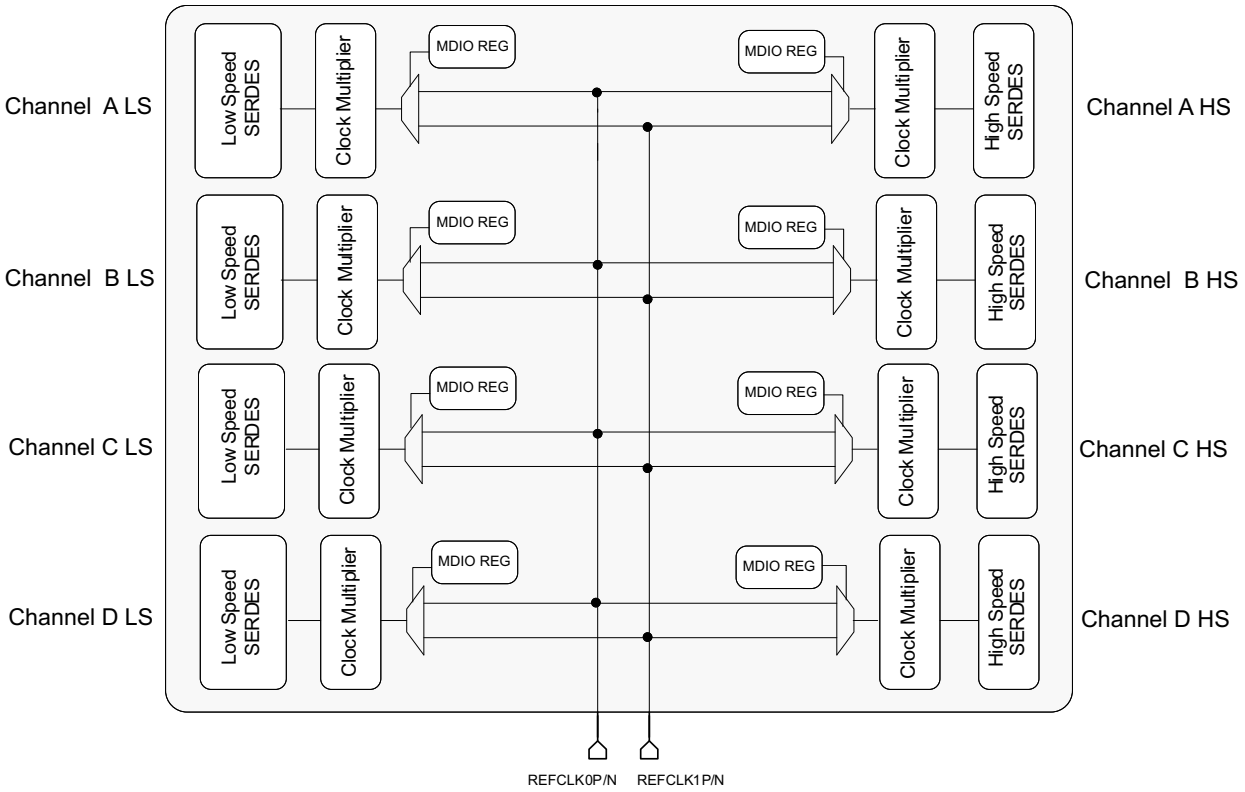


Figure 5-34. Reference Clock Architecture

The architecture of the output clocks is shown in Figure 5-35. The clock and data recovery (CDR) function of the high speed side receiver recovers the clock from the incoming serial data. The high speed side SERDES receiver makes available two versions of clocks for further processing:

- HS_RXBCLK_A/B/C/D: recovered byte clock synchronous with incoming serial data and with a frequency matching the incoming line rate divided by 16 (in the 10GBASE-KR mode), 10 (in the 1G-KX mode), or 20 (in the General Purpose SERDES mode).
- VCO_CLOCK_A/B/C/D_DIV2: VCO frequency divided by 2. (VCO frequency = REFCLK x PLL Multiplier).

(Note: For full rates, VCO/2 pre divided clocks will be equivalent to the line rate divided by 8, for sub-rates, VCO/2 pre divided clocks will be equivalent to the line rate divided by 4)

The above-mentioned clocks can be output through the differential pins HSRXA/B/C/D_CLKOUTP/N with optional frequency division ratios of 1, 2, 4, 5, 8, 10, 16, 20, or 25.

The high speed transmit side clock can also be made available on the HSTX0/1_CLKOUTP/N pins with optional frequency division ratios of 1, 2, 4, 5, 8, 10, 16, 20, or 25.

From the low speed side SERDES, the recovered byte clock from the receive CDR as well as the transmit byte clock (both equal to the low speed side line rate divided by 10) can be made available on the LS0/1_CLKOUTP/N pins with optional frequency division ratios of 1, 2, 4, 5, 8, 10, 16, 20, or 25.

The clock output options may be software controlled through the MDIO interface. The maximum CLKOUT frequency is 500 MHz.

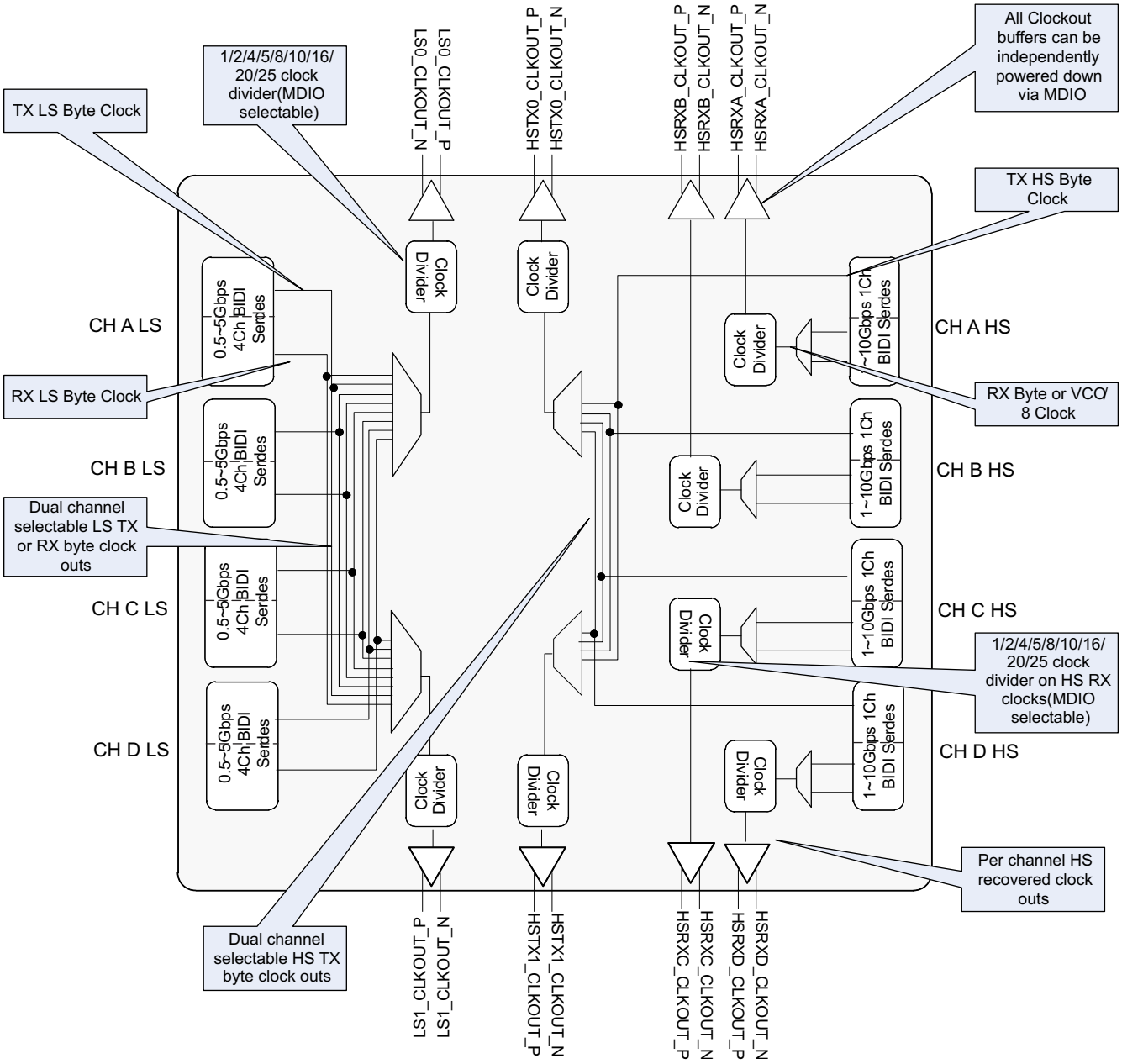


Figure 5-35. Output Clock Architecture

To minimize power consumption, the unused output clock ports can be selectively powered down or disabled. Details on the settings required for various output clock power down modes can be found in Table 5-14, Table 5-15, Table 5-16, Table 5-17, and Table 5-18. Note that when powered down, the clock outputs are held at differential high level. When flat lined, the clock outputs can be either differential high or differential low.

Table 5-14. HSRX*_CLKOUTP/N Power Down Settings(1)

PDTRX*_N	30.1.15	1.0.11(2)	30.32801.2	30.1.14	30.32801.3	30.1.3	HSRXA_CLKOUTP/N
0	x	X	x	x	x	x	Power down
1	1	x	x	x	x	x	Power down

(1) HSRX*_CLKOUTP/N settings are per channel basis
(2) This bit is valid only in 10GKR/1GKX modes.

Table 5-14. HSRX*_CLKOUTP/N Power Down Settings[1] (continued)

PDTRX*_N	30.1.15	1.0.11[2]	30.32801.2	30.1.14	30.32801.3	30.1.3	HSRXA_CLKOUTP/N
1	0	1	x	x	x	x	Power down
1	0	0	1	x	x	x	Power down if PLL lock is lost or LOS detected on HS side else active
1	0	0	0	1	x	x	Power down
1	0	0	0	1	x	x	Power down
1	0	0	0	0	1	x	Flat lined if PLL lock is lost or LOS detected on HS side else active
1	0	0	0	0	0	1	Flat lined
1	0	0	0	0	0	0	Active
Note: When active, HSRX*_CLKOUT frequency depends on HSRX_CLKOUT_SEL (30.1.2) and HSRX_CLKOUT_DIV(30.1.7:4)							

Table 5-15. LS0_CLKOUTP/N Power Down Settings

PDTRXA_N | PDTRXB_N | PDTRXC_N | PDTRXD_N	Ch A 30.1.15 & Ch B 30.1.15 & Ch C 30.1.15 & Ch D 30.1.15	Ch A 1.0.11[1] & Ch B 1.0.11[1] & Ch C 1.0.11[1] & Ch D 1.0.11[1]	30.27.0	30.25.3	LS0_CLKOUTP/N
0	x	x	x	x	Power down
1	1	x	x	x	Power down
1	0	1	x	x	Power down
1	0	0	1	x	Power down
1	0	0	0	1	Flat lined
1	0	0	0	0	Active
Note: When active, LS0_CLKOUT frequency depends on LS0_CLKOUT_SEL (30.25.2:0) and LS0_CLKOUT_DIV(30.25.7:4)					

(1) This bit is valid only in 10GKR/1GKX modes.

Table 5-16. LS1_CLKOUTP/N Power Down Settings

PDTRXA_N | PDTRXB_N | PDTRXC_N | PDTRXD_N	Ch A 30.1.15 & Ch B 30.1.15 & Ch C 30.1.15 & Ch D 30.1.15	Ch A 1.0.11[1] & Ch B 1.0.11[1] & Ch C 1.0.11[1] & Ch D 1.0.11[1]	30.27.1	30.25.11	LS0_CLKOUTP/N
0	x	x	x	x	Power down
1	1	x	x	x	Power down
1	0	1	x	x	Power down
1	0	0	1	x	Power down
1	0	0	0	1	Flat lined
1	0	0	0	0	Active
Note: When active, LS1_CLKOUT frequency depends on LS1_CLKOUT_SEL (30.25.10:8) and LS1_CLKOUT_DIV(30.25.15:12)					

(1) This bit is valid only in 10GKR/1GKX modes.

Table 5-17. HSTX0_CLKOUTP/N Power Down Settings

PDTRXA_N | PDTRXB_N | PDTRXC_N | PDTRXD_N	Ch A 30.1.15 & Ch B 30.1.15 & Ch C 30.1.15 & Ch D 30.1.15	Ch A 1.0.11(1) & Ch B 1.0.11 & (1) Ch C 1.0.11(1) & Ch D 1.0.11(1)	30.26.2	30.26.3	HSTX0_CLKOUTP/N
0	x	x	x	x	Power down
1	1	x	x	x	Power down
1	0	1	x	x	Power down
1	0	0	1	x	Power down
1	0	0	0	1	Flat lined
1	0	0	0	0	Active
Note: When active, HSTX0_CLKOUT frequency depends on HSTX0_CLKOUT_SEL (30.26.1:0) and HSTX0_CLKOUT_DIV(30.26.7:4)					

(1) This bit is valid only in 10GKR/1GKX modes.

Table 5-18. HSTX1_CLKOUTP/N Power Down Settings

PDTRXA_N | PDTRXB_N | PDTRXC_N | PDTRXD_N	Ch A 30.1.15 & Ch B 30.1.15 & Ch C 30.1.15 & Ch D 30.1.15	Ch A 1.0.11(1) & Ch B 1.0.11(1) & Ch C 1.0.11(1) & Ch D 1.0.11(1)	30.26.10	30.26.11	HSTX1_CLKOUTP/N
0	x	x	x	x	Power down
1	1	x	x	x	Power down
1	0	1	x	x	Power down
1	0	0	1	x	Power down
1	0	0	0	1	Flat lined
1	0	0	0	0	Active
Note: When active, HSTX1_CLKOUT frequency depends on HSTX1_CLKOUT_SEL (30.26.9:8) and HSTX0_CLKOUT_DIV(30.26.15:12)					

(1) This bit is valid only in 10GKR/1GKX modes.

5.5.2 Power Down Mode

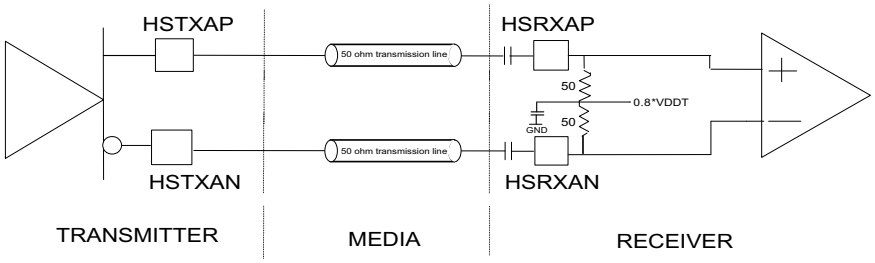
The TLK10034 can be put in power down either through MDIO control bits 30.1.15 and 1.0.11 or via hardware control pins:

- PDTRXA_N: Active low, powers down channel A.
- PDTRXB_N: Active low, powers down channel B.
- PDTRXC_N: Active low, powers down channel C.
- PDTRXD_N: Active low, powers down channel D.

The MDIO management serial interface remains operational when in register based power down mode, but status bits may not be valid since the clocks are disabled. Refer to the detailed per pin description for the behavior of each device I/O signal during pin based and register based power down.

5.5.2.1 High Speed CML Output

The high speed data output driver is implemented using Current Mode Logic (CML) with integrated pull up resistors, requiring no external components. The transmit outputs must be AC coupled.



NOTE: Channel A HS Side is Shown

Figure 5-36. Example of High Speed I/O AC Coupled Mode

Current Mode Logic (CML) drivers often require external components. The disadvantage of the external component is a limited edge rate due to package and line parasitic. The CML driver on TLK10034 has on-chip 50Ω termination resistors terminated to VDDT, providing optimum performance for increased speed requirements. The transmitter output driver is highly configurable allowing output amplitude and de-emphasis to be tuned to a channel's individual requirements. Software programmability allows for very flexible output amplitude control. Only AC coupled output mode is supported.

When transmitting data across long lengths of PCB trace or cable, the high frequency content of the signal is attenuated due to the skin effect of the media. This causes a “smearing” of the data eye when viewed on an oscilloscope. The net result is reduced timing margins for the receiver and clock recovery circuits. In order to provide equalization for the high frequency loss, 3-tap finite impulse response (FIR) transmit de-emphasis is implemented. A highly configurable output driver maximizes flexibility in the end system by allowing de-emphasis and output amplitude to be tuned to a channel’s individual requirements. Output swing control is via MDIO.

See Figure 4-2 for output waveform flexibility. The level of de-emphasis is programmable via the MDIO interface through control registers through pre-cursor and post-cursor settings. Users can control the strength of the de-emphasis to optimize for a specific system requirement.

5.5.2.2 High Speed Receiver

The high speed receiver is differential CML with internal termination resistors. The receiver requires AC coupling. The termination impedances of the receivers are configured as 100 Ω with the center tap weakly tied to 0.7×VDDT with a capacitor to create an AC ground (see Figure 5-36).

TLK10034 serial receivers incorporate adaptive equalizers. This circuit compensates for channel insertion loss by amplifying the high frequency components of the signal, reducing inter-symbol interference. Equalization can be enabled or disabled per register settings.

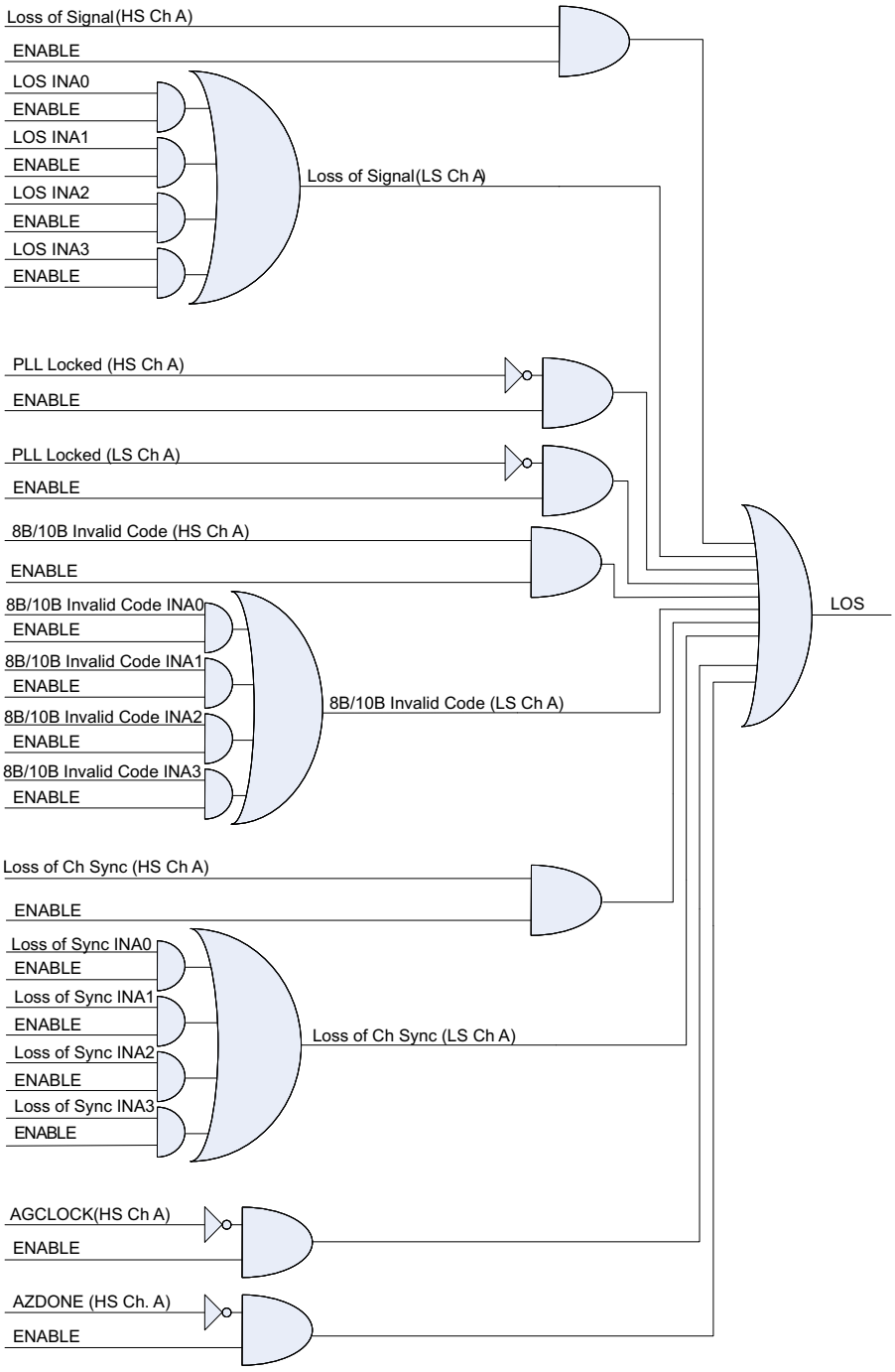
5.5.2.3 Loss of Signal Output Generation (LOS)

Loss of input signal detection is based on the voltage level of each serial input signal IN*P/N, HSRX*P/N. When LOS indication is enabled and a channel's differential serial receive input level is < 65 mVpp, that channel's respective LOS indicator will be asserted (high true). If the input signal is > 175 mVpp, the LOS indicator will be deasserted (low false). Outside of these ranges, the LOS indication is undefined. The LOS indications are also directly readable through the MDIO interface in respective registers.

The following additional critical status conditions can be combined with the loss of signal condition enabling additional real-time status signal visibility on the LOS* outputs per channel:

1. Loss of Channel Synchronization Status – Logically OR'd with LOS condition(s) when enabled. Loss of channel synchronization can be optionally logically OR'd (disabled by default) with the internally generated LOS condition (per channel).
2. Loss of PLL Lock Status on LS and HS sides – Logically OR'd with LOS condition(s) when enabled. The internal PLL loss of lock status bit is optionally OR'd (disabled by default) with the other internally generated loss of signal conditions (per channel).
3. Receive 8B/10B Decode Error (Invalid Code Word or Running Disparity Error) – Logically OR'd with LOS condition(s) when enabled. The occurrence of an 8B/10B decode error (invalid code word or disparity error) is optionally OR'd (disabled by default) with the other internally generated loss of signal conditions (per channel).
4. AGCLOCK (Active Gain Control Currently Locked) – Inverted and Logically OR'd with LOS condition(s) when enabled. HS RX SERDES adaptive gain control unlocked indication is optionally OR'd (disabled by default) with the other internally generated loss of signal conditions (per channel).
5. AZDONE (Auto Zero Calibration Done) - Inverted and Logically OR'd with LOS conditions(s) when enabled. HS RX SERDES auto-zero not done indication is optionally OR'd (disabled by default) with the other internally generated loss of signal conditions (per channel).

Refer to Figure 5-37, which shows the detailed implementation of the LOSA signal along with the associated MDIO control registers for the General Purpose SERDES mode. More details about LOS settings including configurations related to the 10GBASE-KR mode can be found in the Programmers Reference section.



Note: LOSA is asserted (driven high) during a failing condition, and deasserted (driven low) otherwis . Any combinations of status signals may be enabled onto LOSA/B/C/D based on MDIO register bits indicated above. LOSB/C/D circuits are similar.

Figure 5-37. LOSA – Logic Circuit Implementation

5.5.3 MDIO Management Interface

The TLK10034 supports the Management Data Input/Output (MDIO) Interface as defined in Clauses 22 and 45 of the IEEE 802.3ae Ethernet specification. The MDIO allows register-based management and control of the serial links. Whether Clause 22 or Clause 45 is used will depend on the ST pin settings. If ST is low, Clause 45 is used. If ST is high, Clause 22 is used.

The MDIO Management Interface consists of a bi-directional data path (MDIO) and a clock reference (MDC). The device identification and port address are determined by control pins (see Table 3-1). Also, whether the device responds as a Clause 22 or Clause 45 device is also determined by control pin ST (see Table 3-1).

In Clause 45 (ST = 0) and Clause 22 (ST = 1), the top 3 control pins PRTAD[4:2] determine the device port address. In this mode, TLK10034 will respond if the PHY address field on the MDIO protocol (PA[4:2]) matches PRTAD[4:2] pin value. In both these modes the 4 individual channels in TLK10034 are classified as 4 different ports. So for any PRTAD[4:2] value there will be 4 ports per TLK10034. 2 MSB's of PHY address field (PA[1:0]) will determine which channel/port within TLK10034 to respond.

If PA[1:0] = 2'b00, TLK10034 Channel A will respond.
If PA[1:0] = 2'b01, TLK10034 Channel B will respond.
If PA[1:0] = 2'b10, TLK10034 Channel C will respond.
If PA[1:0] = 2'b11, TLK10034 Channel D will respond.

In Clause 22 (ST = 1) mode, only 32 (5'b00000 to 5'b11111) register addresses can be accessed through standard protocol. Due to this limitation, an indirect addressing method (More description in Clause 22 Indirect Addressing section) is implemented to provide access to all device specific control/status registers that cannot be accessed through the standard Clause 22 register address space.

Write transactions which address an invalid register or device or a read only register will be ignored. Read transactions which address an invalid register or device will return a 0.

5.5.4 MDIO Protocol Timing

Timing for a Clause 45 address transaction is shown in Figure 5-38. The Clause 45 timing required to write to the internal registers is shown in Figure 5-39. The Clause 45 timing required to read from the internal registers is shown in Figure 5-40. The Clause 45 timing required to read from the internal registers and then increment the active address for the next transaction is shown in Figure 5-41. The Clause 22 timing required to read from the internal registers is shown in Figure 5-42. The Clause 22 timing required to write to the internal registers is shown in Figure 5-43.

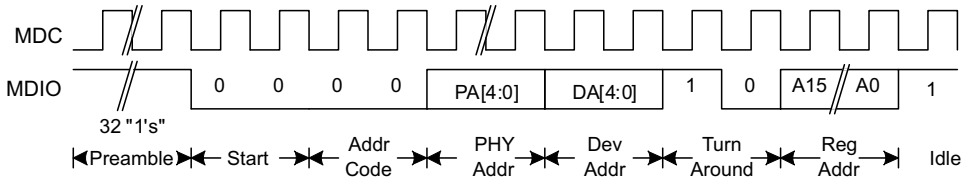


Figure 5-38. CL45 - Management Interface Extended Space Address Timing

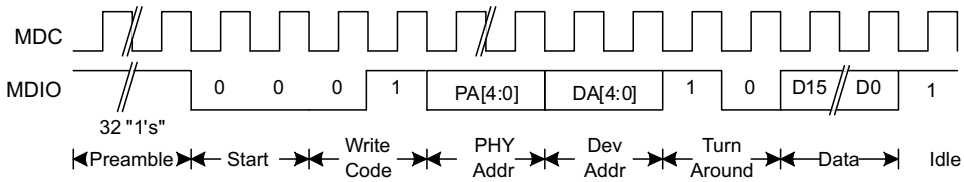


Figure 5-39. CL45 - Management Interface Extended Space Write Timing

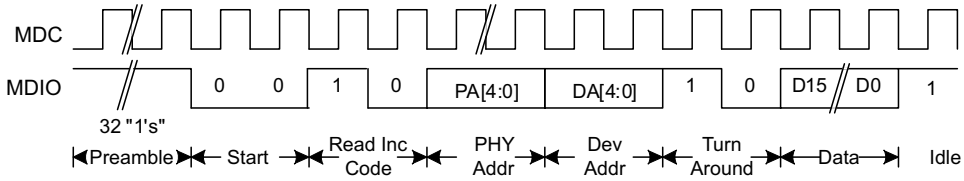


Figure 5-40. CL45 - Management Interface Extended Space Read Timing

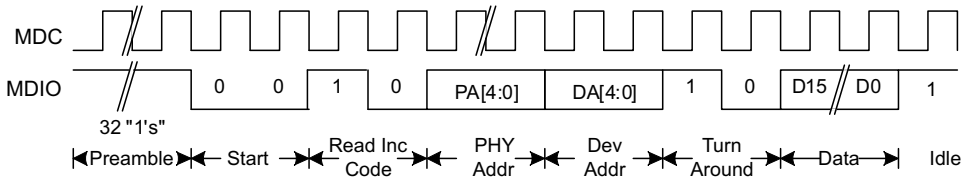


Figure 5-41. CL45 - Management Interface Extended Space Read And Increment Timing

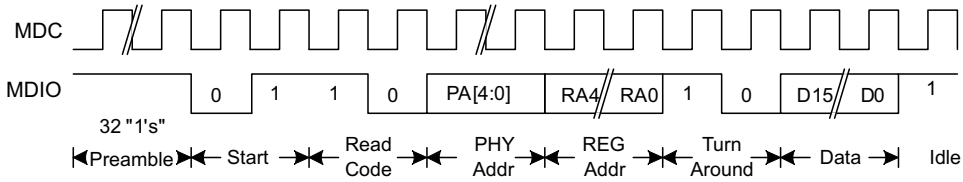


Figure 5-42. CL22 - Management Interface Read Timing

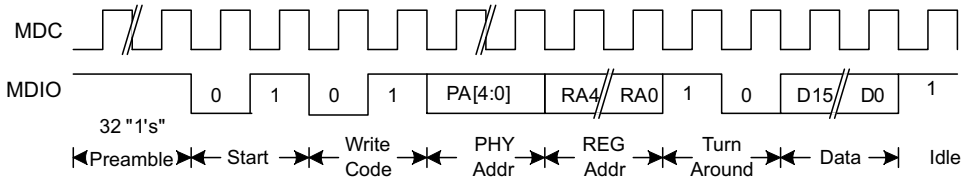


Figure 5-43. CL22 - Management Interface Write Timing

The IEEE 802.3 Clause 22/45 specification defines many of the registers, and additional registers have been implemented for expanded functionality.

5.5.5 Clause 22 Indirect Addressing

Due to Clause 22 register space limitations, an indirect addressing method is implemented so that the extended register space can be accessed through Clause 22. All the device specific control and status registers that cannot be accessed through Clause 22 direct addressing can be accessed through this indirect addressing method. To access this register space, an address control register (Reg 30, 5'h1E) should be written with the register address followed by a read/write transaction to address content register (Reg 31, 5'h1F) to access the contents of the address specified in address control register. Following timing diagrams illustrate an example write transaction to Register 16'h9000 using indirect addressing in Clause 22.

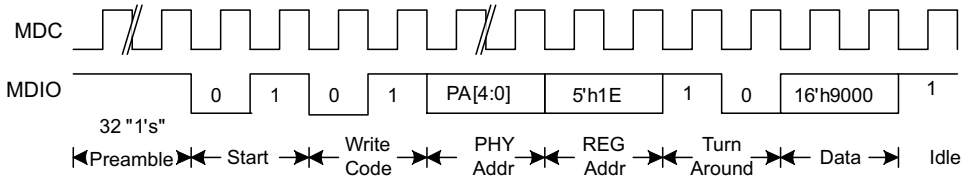


Figure 5-44. CL22 – Indirect Address Method – Address Write

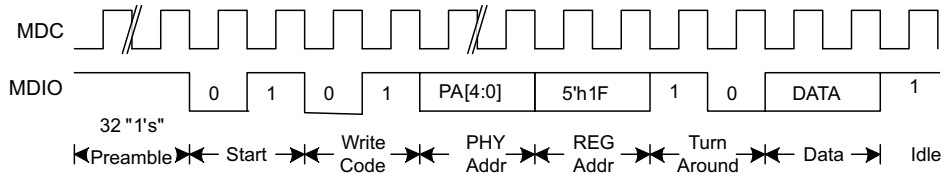


Figure 5-45. CL22 - Indirect Address Method – Data Write

Following timing diagrams illustrate an example read transaction to read contents of Register 16'h9000 using indirect addressing in Clause 22.

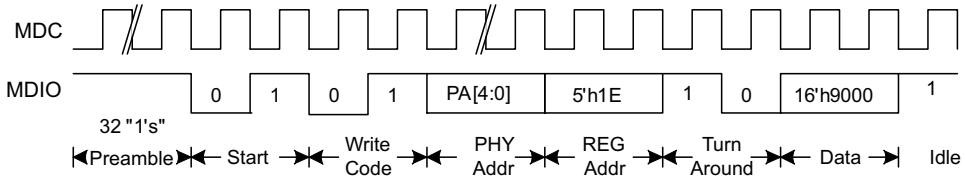


Figure 5-46. CL22 - Indirect Address Method – Address Write

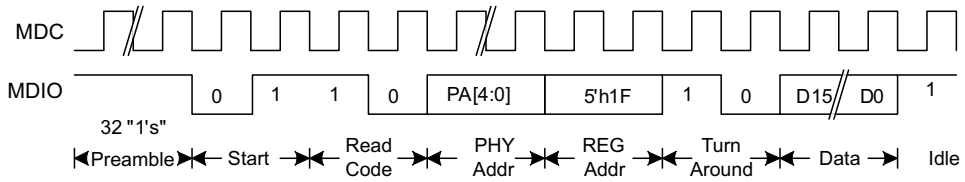


Figure 5-47. CL22 - Indirect Address Method – Data Read

5.5.6 Programmers Reference

The top 3 control pins PRTAD[4:2] determine the device port address. In this mode, TLK10034 will respond if the PHY address field on the MDIO protocol (PA[4:2]) matches PRTAD[4:2] pin value. In both Clause 45 and Clause 22 modes, the 4 individual channels in TLK10034 are classified as 4 different ports. So for any PRTAD[4:2] value there will be 4 ports per TLK10034. 2 LSB's of PHY address field (PA[1:0]) will determine which channel/port within TLK10034 to respond.

- Channel A can be accessed by setting 2 LSB bits of PHY address to 2'b00.
- Channel B can be accessed by setting 2 LSB bits of PHY address to 2'b01.
- Channel C can be accessed by setting 2 LSB bits of PHY address to 2'b10.
- Channel D can be accessed by setting 2 LSB bits of PHY address to 2'b11.

Table 5-19 illustrates device modes with respect to ST and MODE_SEL pins. 10G mode referenced in below table and in the rest of programmer's reference is equivalent to General purpose SERDES mode.

Table 5-19. Mode Selection

	ST = 0 (Clause 45)	ST = 1 (Clause 22)
{MODE_SEL pin, SW bit (30.1.10)}		
1x	10G	10G
01	10G	10G
00	10G-KR/1G-KX (Determined by Auto Neg)	1G-KX (No Auto Neg)

Following programmer's reference is divided into 3 sections. 10G-KR PROGRAMMERS REFERENCE is applicable in 10GKR mode only, 1G-KX PROGRAMMERS REFERENCE is applicable in 1G-KX mode only and 10G PROGRAMMERS REFERENCE applicable is in 10G mode only. Control register bits (RW) specified as NA in each section are not applicable in that specific mode and should not be changed from their default value. Read values of status register bits (RO/LH/LL/COR) that are specified as NA in each section are not valid and not applicable in that specific mode and should be left at their default or recommended values.

5.5.7 Register Bit Definitions

RW: Read-Write
User can write 0 or 1 to this register bit. Reading this register bit returns the same value that has been written.

RW/SC: Read-Write Self-Clearing
User can write 0 or 1 to this register bit. Writing a 1 to this register creates a high pulse. Reading this register bit always returns 0.

RO: Read-Only
This register can only be read. Writing to this register bit has no effect. Reading from this register bit returns its current value.

RO/LH: Read-Only Latched High
This register can only be read. Writing to this register bit has no effect. Reading a 1 from this register bit indicates that either the condition is occurring or it has occurred since the last time it was read. Reading a 0 from this register bit indicates that the condition is not occurring presently, and it has not occurred since the last time the register was read. A latched high register, when read high, should be read again to distinguish if a condition occurred previously or is still occurring. If it occurred previously, the second read will read low. If it is still occurring, the second read will read high. Reading this register bit automatically resets its value to 0.

RO/LL: Read-Only Latched Low
This register can only be read. Writing to this register bit has no effect. Reading a 0 from this register bit indicates that either the condition is occurring or it has occurred since the last time it was read. Reading a 1 from this register bit indicates that the condition is not occurring presently, and it has not occurred since the last time the register was read. A latched low register, when read low, should be read again to distinguish if a condition occurred previously or is still occurring. If it occurred previously, the second read will read high. If it is still occurring, the second read will read low. Reading this register bit automatically sets its value to 1.

COR: Clear-On-Read counter
This register can only be read. Writing to this register bit has no effect. Reading from this register bit returns its current value, then resets its value to 0. Counter value freezes at Max.

5.6 Register Map

5.6.1 10G-KR Programmers Reference

5.6.1.1 Vendor Specific Device Registers

These registers can be accessed by setting device address field to 0x1E (DA[4:0] = 5'b11110).

Table 5-20. GLOBAL_CONTROL_1(1)

Device Address: 0x1E Register Address:0x0000 Default: 0x0020			
Bit	**Name**	**Description**	**Access**
15	GLOBAL_RESET	Global reset. 0 = Normal operation (Default 1'b0) 1 = Resets TX and RX data path including MDIO registers. Equivalent to asserting RESET_N.	RW SC(2)
11	GLOBAL_WRITE	Global write enable. 0 = Control settings are specific to channel addressed (Default 1'b0) 1 = Control settings in channel specific registers are applied to all 4 channels regardless of channel addressed	RW

(1) This global register is channel independent.
(2) After reset bit is set to one, it automatically sets itself back to zero on the next MDC clock cycle.

Table 5-20. GLOBAL_CONTROL_1[(1)] (continued)

Device Address: 0x1E Register Address:0x0000 Default: 0x0020			
Bit	**Name**	**Description**	**Access**
5:0	PRBS_PASS_OVERLAY[5:0]	PRBS_PASS pin status selection. Applicable only when PRBS test pattern verification is enabled on HS side or LS side. PRBS_PASS pin reflects PRBS verification status on selected Channel HS/LS side 1xx000 = PRBS_PASS reflects combined status of Channel A/B/C/D HS serdes PRBS verification. If PRBS verification fails on any channel HS serdes, PRBS_PASS will be asserted low. (Default 6'b100000) 000000 = Status from Channel A HS Serdes side 000001 = NA 00001x = Reserved 000100 = Status from Channel A LS Serdes side Lane 0000101 = Status from Channel A LS Serdes side Lane 1000110 = Status from Channel A LS Serdes side Lane 2000111 = Status from Channel A LS Serdes side Lane 3001000 = Status from Channel B HS Serdes side 001001 = NA 00101x = Reserved 001100 = Status from Channel B LS Serdes side Lane 0001101 = Status from Channel B LS Serdes side Lane 1001110 = Status from Channel B LS Serdes side Lane 2001111 = Status from Channel B LS Serdes side Lane 3010000 = Status from Channel C HS Serdes side 010001 = NA 01001x = Reserved 010100 = Status from Channel C LS Serdes side Lane 0010101 = Status from Channel C LS Serdes side Lane 1010110 = Status from Channel C LS Serdes side Lane 2 010111 = Status from Channel C LS Serdes side Lane 3011000 = Status from Channel D HS Serdes side 011001 = NA 01101x = Reserved 011100 = Status from Channel D LS Serdes side Lane 0011101 = Status from Channel D LS Serdes side Lane 1011110 =Status from Channel D LS Serdes side Lane 2011111 = Status from Channel D LS Serdes side Lane 3	RW

Table 5-21. CHANNEL_CONTROL_1

Device Address: 0x1E Register Address:0x0001 Default: 0x0B88			
Bit	**Name**	**Description**	**Access**
15	POWERDOWN	Setting this bit high powers down entire data path with exception that MDIO interface stays active. 0 = Normal operation (Default 1'b0) 1 = Power Down mode is enabled.	RW
14	HSRX_CLKOUT_POWERDOWN	0 = Normal operation (Default 1'b0) 1 = Enable HSRXx_CLKOUTP/N Power Down.	RW
13	10G_RX_MODE_SEL	NA. This bit must be left at its default value (1'b0) for proper 10GKR operation.	RW
12	10G_TX_MODE_SEL	NA. This bit must be left at its default value (1'b0) for proper 10GKR operation.	RW
11	SW_PCS_SEL	Valid only when MODE_SEL pin is 0, AN_ENABLE (7.0.12) is 0 and SW_DEV_MODE_SEL (30.1.10) is 0. 1 = Set device to 10G-KR mode(Default 1'b1) 0 = NA This bit must be left at its default value (1'b1) for proper 10GKR operation.	RW
10	SW_DEV_MODE_SEL	Valid only when MODE_SEL pin is 0 1 = NA 0 = Device mode is set using Auto negotiation. (Default 1'b0) This bit must be left at its default value (1'b0) for proper 10GKR operation.	RW
9	10G_RX_DEMUX_SEL	NA. This bit must be left at its default value (1'b1) for proper 10GKR operation.	RW
8	10G_TX_MUX_SEL	NA. This bit must be left at its default value (1'b1) for proper 10GKR operation.	RW
7:4	HSRX_CLKOUT_DIV[3:0]	Output clock divide setting. This value is used to divide selected clock (Selected using HSRX_CLKOUT_SEL) before giving it out onto respective channel HSRXx_CLKOUTP/N. 0000 = Divide by 1 0001 = RESERVED 0010 = RESERVED 0011 = RESERVED 0100 = Divide by 2 0101 = RESERVED 0110 = RESERVED 0111 = RESERVED 1000 = Divide by 4 (Default 4'b1000) 1001 = Divide by 8 1010 = Divide by 16 1011 = RESERVED 1100 = Divide by 5 1101 = Divide by 10 1110 = Divide by 20 1111 = Divide by 25	RW
3	HSRX_CLKOUT_ EN	Output clock enable. 0 = Holds HSRXx_CLKOUTP/N output to a fixed value. 1 = Allows HSRXx_CLKOUTP/N output to toggle normally (Default 1'b1)	RW
2	HSRX_CLKOUT_SEL	Output clock select. Selected Recovered clock sent out on HSRXx_CLKOUTP/N pins 0 = Selects respective Channel HSRX recovered byte clock as output clock (Default 1'b0) 1 = Selects respective Channel HSRX VCO divide by 2 clock as output clock	RW
1	REFCLK_SW_SEL	Channel HS Reference clock selection. Applicable only when REFCLK_SEL pin is LOW. 0 = Selects REFCLK_0_P/N as clock reference to Channel x HS side serdes macro(Default 1'b0) 1 = Selects REFCLK_1_P/N as clock reference to Channel x HS side serdes macro	RW
0	LS_REFCLK_SEL	Channel LS Reference clock selection. 0 = LS side serdes macro reference clock is same as HS side serdes reference clock (E.g. If REFCLK_0_P/N is selected as HS side serdes macro reference clock, REFCLK_0_P/N is selected as LS side serdes macro reference clock and vice versa) (Default 1'b0) 1 = Alternate reference clock is selected as clock reference to Channel x LS side serdes macro (E.g. If REFCLK_0_P/N is selected as HS side serdes macro reference clock, REFCLK_1_P/N is selected as LS side serdes macro reference clock and vice versa)	RW

Table 5-22. HS_SERDES_CONTROL_1

Device Address: 0x1E Register Address:0x0002 Default: 0x811D			
Bit	**Name**	**Description**	**Access**
15:10	RESERVED	For TI use only (Default 9'b100000)	RW
9:8	HS_LOOP_BANDWIDTH[1:0]	HS Serdes PLL Loop Bandwidth settings 00 = Rserved 01 = Narrow bandwidth (Default 2'b01) 11 = Highest bandwidth. Recommended for 10GBASE-KR.	RW
7	RESERVED	For TI use only (Default 1'b1)	
6	HS_VRANGE	HS Serdes PLL VCO range selection. 0 = VCO runs at higher end of frequency range (Default 1'b0) 1 = VCO runs at lower end of frequency range This bit needs to be set HIGH if VCO frequency (REFCLK *HS_PLL_MULT) is below 2.5 Ghz.	RW
5	RESERVED	For TI use only (Default 1'b0)	RW
4	HS_ENPLL	HS Serdes PLL enable control. HS Serdes PLL is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 30.1.15 is set HIGH. 0 = Disables PLL in HS serdes 1 = Enables PLL in HS serdes (Default 1'b1)	RW
3:0	HS_PLL_MULT[3:0]	HS Serdes PLL multiplier setting (Default 4'b1101). This setting is automatically controlled and value set through these register bits is ignored unless REFCLK_FREQ_SEL_1 or related OVERRIDE bit is set. Refer 10GKR supported rates for valid PLL Multiplier values. Refer Table 5-23.	RW

Table 5-23. HS PLL Multiplier Control

30.2.3:0		30.2.3:0	
Value	**PLL Multiplier factor**	**Value**	**PLL Multiplier factor**
0000	Reserved	1000	12x
0001	Reserved	1001	12.5x
0010	4x	1010	15x
0011	5x	1011	16x
0100	6x	1100	16.5x
0101	8x	1101	20x
0110	8.25x	1110	25x
0111	10x	1111	Reserved

Table 5-24. HS_SERDES_CONTROL_2

Device Address: 0x1E Register Address:0x0003 Default:0x8848			
Bit	**Name**	**Description**	**Access**
15:12	HS_SWING[3:0]	Transmitter Output swing control for HS Serdes. (Default 4'b1000) Refer Table 5-25.	RW
11	HS_ENTX	HS Serdes transmitter enable control. HS Serdes transmitter is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 30.1.15 is set HIGH. 0 = Disables HS serdes transmitter 1 = Enables HS serdes transmitter (Default 1'b1)	RW
10	HS_EQHLD	HSRX Equalizer hold control. This setting is automatically controlled through link training and value set through this register bit is ignored unless related OVERRIDE bit is set. 0 = Normal operation (Default 1'b0) 1 = Holds equalizer and long tail correction in its current state	RW

Table 5-24. HS_SERDES_CONTROL_2 (continued)

Device Address: 0x1E Register Address:0x0003 Default:0x8848			
Bit	**Name**	**Description**	**Access**
9:8	HS_RATE_TX [1:0]	HS Serdes TX rate settings. This setting is automatically controlled and value set through these register bits is ignored unless REFCLK_FREQ_SEL_1 or related OVERRIDE bit is set. 00 = Full rate (Default 2'b00) 01 = Half rate 10 = Quarter rate 11 = Eighth rate	RW
7:4	RESERVED	For TI use only (Default 4'b0100)	RW
3	HS_ENRX	HS Serdes receiver enable control. This setting is automatically controlled and value set through this register bit is ignored unless related OVERRIDE bit is set. HS Serdes receiver is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 30.1.15 is set HIGH. 0 = Disables HS serdes receiver 1 = Enables HS serdes receiver (Default 1'b1)	RW
2:0	HS_RATE_RX [2:0]	HS Serdes RX rate settings. This setting is automatically controlled and value set through these register bits is ignored unless REFCLK_FREQ_SEL_1 or related OVERRIDE bit is set. 000 = Full rate (Default 3'b000) 101 = Half rate 110 = Quarter rate 111 = Eighth rate 001 = Reserved 01x = Reserved 100 = Reserved	RW

Table 5-25. HSTX AC Mode Output Swing Control

VALUE 30.3[15:12]	AC MODE
	TYPICAL AMPLITUDE (mVdfpp)
0000	130
0001	220
0010	300
0011	390
0100	480
0101	570
0110	660
0111	750
1000	830
1001	930
1010	1020
1011	1110
1100	1180
1101	1270
1110	1340
1111	1400

Table 5-26. HS_SERDES_CONTROL_3

Device Address: 0x1E Register Address:0x0004 Default:0x1400			
Bit	**Name**	**Description**	**Access**
15	HS_ENTRACK	HSRX ADC Track mode. This setting is automatically controlled through link training and value set through this register bit is ignored unless related OVERRIDE bit is set. 0 = Normal operation (Default 1'b0) 1 = Forces ADC into track mode	RW
14:12	HS_EQPRE[2:0]	Serdes Rx precursor equalizer selection 000 = 1/9 cursor amplitude 001 = 3/9 cursor amplitude (Default 3'b001) 010 = 5/9 cursor amplitude 011 = 7/9 cursor amplitude 100 = 9/9 cursor amplitude 101 =11/9 cursor amplitude 110 = 13/9 cursor amplitude 111 = Disable	RW
11:10	HS_CDRFMULT[:10]	Clock data recovery algorithm frequency multiplication selection 00 = First order. Frequency offset tracking disabled 01 = Second order. 1x mode 10 = Second order. 2x mode (Default 2'b10) 11 = Reserved	RW
9:8	HS_CDRTHR[1:0]	Clock data recovery algorithm threshold selection 00 = Four vote threshold (Default 2'b00) 01 = Eight vote threshold 10 = Sixteen vote threshold 11 = Thirty two vote threshold	RW
7	RESERVED	For TI use only (Default 1'b0)	RW
6	HS_PEAK_DISABLE	HS Serdes PEAK_DISABLE control 0 = Normal operation (Default 1'b0) 1 = Disables high frequency peaking. Suitable for <6 Gbps operation	RW
5	HS_H1CDRMODE	0 = Normal operation (Default 1'b0) 1 = Enables CDR mode suitable for short channel operation.	RW
4:0	HS_TWCRF[4:0]	Cursor Reduction Factor (Default 5'b00000). This setting is automatically controlled through link training and value set through this register bits is ignored unless related OVERRIDE bit is set. Refer to Table 5-27.	RW

Table 5-27. HSTX Cursor Reduction Factor Weights

30.4.4:0		30.4.4:0	
Value	**Cursor reduction (%)**	**Value**	**Cursor reduction (%)**
00000	0	10000	17
00001	2.5	10001	20
00010	5.0	10010	22
00011	7.5	10011	25
00100	10.0	10100	27
00101	12	10101	30
00110	15	10110	32
00111	Reserved	10111	35
01000		11000	37
01001		11001	40
01010		11010	42
01011		11011	45
01100		11100	47
01101		11101	50
01110		11110	52
01111		11111	55

Table 5-28. HS_SERDES_CONTROL_4

Device Address: 0x1E Register Address:0x0005 Default:0x2000			
Bit	**Name**	**Description**	**Access**
15	HS_RX_INVPAIR	Receiver polarity. 0 = Normal polarity. HSRXxP considered positive data. HSRXxN considered negative data (Default 1'b0) 1 = Inverted polarity. HSRXxP considered negative data. HSRXxN considered positive data	RW
14	HS_TX_INVPAIR	Transmitter polarity. 0 = Normal polarity. HSTXxP considered positive data and HSTXxN considered negative data (Default 1'b0) 1 = Inverted polarity. HSTXxP considered negative data and HSTXxN considered positive data	RW
13	RESERVED	For TI use only (Default 1'b1)	RW
12:8	HS_TWPOST1[4:0]	Adjacent post cursor1 Tap weight. Selects TAP settings for TX waveform. This setting is automatically controlled through link training and value set through this register bits is ignored unless related OVERRIDE bit is set. (Default 5'b00000) Refer Table 5-29.	RW
7:4	HS_TWPRE[3:0]	Precursor Tap weight. Selects TAP settings for TX waveform. This setting is automatically controlled through link training and value set through this register bits is ignored unless related OVERRIDE bit is set. (Default 4'b0000) Refer Table 5-31.	RW
3:0	HS_TWPOST2[3:0]	Adjacent post cursor2 Tap weight. Selects TAP settings for TX waveform. This setting is automatically controlled through link training and value set through this register bits is ignored unless related OVERRIDE bit is set.(Default 4'b0000) Refer Table 5-30.	RW

Table 5-29. HSTX Post-Cursor1 Transmit Tap Weights

30.5.12:8		30.5.12:8	
Value	**Tap weight (%)**	**Value**	**Tap weight (%)**
00000	0	10000	0
00001	+2.5	10001	–2.5
00010	+5.0	10010	–5.0
00011	+7.5	10011	–7.5
00100	+10.0	10100	–10.0
00101	+12.5	10101	–12.5
00110	+15.0	10110	–15.0
00111	+17.5	10111	–17.5
01000	+20.0	11000	–20.0
01001	+22.5	11001	–22.5
01010	+25.0	11010	–25.0
01011	+27.5	11011	–27.5
01100	+30.0	11100	–30.0
01101	+32.5	11101	–32.5
01110	+35.0	11110	–35.0
01111	+37.5	11111	-37.5

Table 5-30. HSTX Post-Cursor2 Transmit Tap Weights

30.5.3:0		30.5.3:0	
Value	**Tap weight (%)**	**Value**	**Tap weight (%)**
0000	0	1000	0
0001	+2.5	1001	–2.5
0010	+5.0	1010	–5.0

Table 5-30. HSTX Post-Cursor2 Transmit Tap Weights (continued)

30.5.3:0		30.5.3:0	
Value	Tap weight (%)	Value	Tap weight (%)
0011	+7.5	1011	–7.5
0100	+10.0	1100	–10.0
0101	+12.5	1101	–12.5
0110	+15.0	1110	–15.0
0111	+17.5	1111	–17.5

Table 5-31. HSTX Pre-Cursor Transmit Tap Weights

30.5.7:4		30.5.7:4	
Value	Tap weight (%)	Value	Tap weight (%)
0000	0	1000	0
0001	+2.5	1001	–2.5
0010	+5.0	1010	–5.0
0011	+7.5	1011	–7.5
0100	+10.0	1100	–10.0
0101	+12.5	1101	–12.5
0110	+15.0	1110	–15.0
0111	+17.5	1111	–17.5

Table 5-32. LS_SERDES_CONTROL_1

Device Address: 0x1E Register Address:0x0006 Default:0xF115			
Bit	**Name**	**Description**	**Access**
15:12	LS_LN_CFG_EN[3:0]	Configuration control for LS Serdes Lane settings (Default 4'b1111) [3] corresponds to LN3, [2] corresponds to LN2 [1] corresponds to LN1, [0] corresponds to LN0 0 = Writes to LS_SERDES_CONTROL_2 and LS_SERDES_CONTROL_3 and LS_CH_CONTROL_1 control registers do not affect respective LS Serdes lane 1 = Writes to LS_SERDES_CONTROL_2 and LS_SERDES_CONTROL_3 and LS_CH_CONTROL_1 control registers affect respective LS Serdes lane For example, if subsequent writes to LS_SERDES_CONTROL_2 and LS_SERDES_CONTROL_3 and LS_CH_CONTROL_1 registers need to affect the settings in Lanes 0 and 1, LS_LN_CFG_EN[3:0] should be set to 4'b0011 Read values in LS_SERDES_CONTROL_2 and LS_SERDES_CONTROL_3 and LS_CH_CONTROL_1 reflect the settings value for Lane selected through LS_LN_CFG_EN[3:0]. To read Lane 0 settings, LS_LN_CFG_EN[3:0] should be set to 4'b0001 To read Lane 1 settings, LS_LN_CFG_EN[3:0] should be set to 4'b0010 To read Lane 2 settings, LS_LN_CFG_EN[3:0] should be set to 4'b0100 To read Lane 3 settings, LS_LN_CFG_EN[3:0] should be set to 4'b1000 Read values of LS_SERDES_CONTROL_2 and LS_SERDES_CONTROL_3 and LS_CH_CONTROL_1 registers are not valid for any other LS_LN_CFG_EN[3:0] combination	RW
11:10	RESERVED	For TI use only (Default 2'b00)	
9:8	LS_LOOP_BANDWIDTH[1:0]	LS Serdes PLL Loop Bandwidth settings 00 = Reserved 01 = Applicable when external JC_PLL is NOT used (Default 2'b01) 10 = Applicable when external JC_PLL is used 11 = Reserved	
7:5	RESERVED	For TI use only (Default 3'b000)	
4	LS_ENPLL	LS Serdes PLL enable control. LS Serdes PLL is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 30.1.15 is set HIGH. 0 = Disables PLL in LS serdes 1 = Enables PLL in LS serdes (Default 1'b1)	

Table 5-32. LS_SERDES_CONTROL_1 (continued)

Device Address: 0x1E Register Address:0x0006 Default:0xF115			
Bit	**Name**	**Description**	**Access**
3:0	LS_MPY[3:0]	LS Serdes PLL multiplier setting (Default 4'b0101). This setting is automatically controlled and value set through these register bits is ignored unless REFCLK_FREQ_SEL_1 or related OVERRIDE bit is set. Refer 10GKR supported rates for valid PLL Multiplier values. Refer to Table 5-33.	

Table 5-33. LS PLL Multiplier Control

30.6.3:0		30.6.3:0	
Value	**PLL Multiplier factor**	**Value**	**PLL Multiplier factor**
0000	4x	1000	15x
0001	5x	1001	20x
0010	6x	1010	25x
0011	Reserved	1011	Reserved
0100	8x	1100	Reserved
0101	10x	1101	50x
0110	12x	1110	65x
0111	12.5x	1111	Reserved

Table 5-34. LS_SERDES_CONTROL_2

Device Address: 0x1E Register Address:0x0007 Default:0xDC04			
Bit	**Name**	**Description**	**Access**
15	RESERVED	For TI use only.	RW
14:12	LS_SWING[2:0]	Output swing control on LS Serdes side. (Default 3'b101) Refer to Table 5-35.	RW
11	LS_LOS	LS Serdes LOS detector control 0 = Disable Loss of signal detection on LS serdes lane inputs 1 = Enable Loss of signal detection on LS serdes lane inputs (Default 1'b1)	RW
10	LS_TX_ENRX	LS Serdes enable control on the transmit channel. LS Serdes per lane on transmitter channel is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 30.1.15 is set HIGH. 0 = Disables LS serdes lane 1 = Enables LS serdes lane (Default 1'b1)	RW
9:8	LS_TX_RATE [1:0]	LS Serdes lane rate settings on transmit channel. This setting is automatically controlled and value set through this register bits is ignored unless REFCLK_FREQ_SEL_1 or related OVERRIDE bit is set. 00 = Full rate (Default 2'b00) 01 = Half rate 10 = Quarter rate 11 = Reserved	RW
7:4	LS_DE[3:0]	LS Serdes De-emphasis settings. (Default 4'b0000) Refer to Table 5-36.	RW
3	RESERVED	For TI use only.	RW
2	LS_RX_ENTX	LS Serdes lane enable control on receive channel. LS Serdes per lane on receiver channel is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 30.1.15 is set HIGH. 0 = Disables LS serdes lane 1 = Enables LS serdes lane (Default 1'b1)	RW
1:0	LS_RX_RATE [1:0]	LS Serdes lane rate settings on receive channel. This setting is automatically controlled and value set through this register bits is ignored unless REFCLK_FREQ_SEL_1 or related OVERRIDE bit is set. 00 = Full rate (Default 2'b00) 01 = Half rate 10 = Quarter rate 11 = Reserved	RW

Table 5-35. LSRX Output AC Mode Output Swing Control

VALUE 30.3[15:12]	AC MODE
	TYPICAL AMPLITUDE (mVdfpp)
000	190
001	380
010	560
011	710
100	850
101	950
110	1010
111	1050

Table 5-36. LSRX Output De-emphasis

30.7.7:4			30.7.7:4		
Value	Amplitude reduction		Value	Amplitude reduction	
	(%)	dB		(%)	dB
0000	0	0	1000	38.08	–4.16
0001	4.76	–0.42	1001	42.85	–4.86
0010	9.52	–0.87	1010	47.61	–5.61
0011	14.28	–1.34	1011	52.38	–6.44
0100	19.04	–1.83	1100	57.14	–7.35
0101	23.8	–2.36	1101	61.9	–8.38
0110	28.56	–2.92	1110	66.66	–9.54
0111	33.32	–3.52	1111	71.42	–10.87

Table 5-37. LS_SERDES_CONTROL_3

Device Address: 0x1E Register Address:0x0008 Default:0x000D			
Bit	**Name**	**Description**	**Access**
15	LS_RX_INVPAIR	LS Serdes lane outputs polarity on the receive channel. (x = Channel A or B or C or D, y = Lane 0 or 1 or 2 or 3) 0 = Normal polarity. OUTxyP considered positive data. OUTxyN considered negative data (Default 1'b0) 1 = Inverted polarity. OUTxyP considered negative data. OUTxyN considered positive data	RW
14	LS_TX_INVPAIR	LS Serdes lane inputs polarity on the transmit channel. (x = Channel A or B or C or D, y = Lane 0 or 1 or 2 or 3) 0 = Normal polarity. INxyP considered positive data and INxyN considered negative data (Default 1'b0) 1 = Inverted polarity. INxyP considered negative data and INxyP considered positive data	RW
13:12	RESERVED	For TI use only (Default 2'b00)	RW
11:8	LS_EQ[3:0]	LS Serdes Equalization control (Default 4'b0000). Table 5-38	RW
7:0	RESERVED	For TI use only (Default 8'b00001101)	RW

Table 5-38. LS_EQ Serdes Equalization

30.8.11:8			30.8.11:8		
Value	Low Freq Gain	Zero Freq	Value	Low Freq Gain	Zero Freq
0000	Maximum		1000	Adaptive	365 MHz
0001	Adaptive		1001		275 MHz
0010	Reserved		1010		195 MHz
0011			1011		140 MHz
0100			1100		105 MHz
0101			1101		75 MHz
0110			1110		55 MHz
0111			1111		50 MHz

Table 5-39. HS_OVERLAY_CONTROL

Device Address: 0x1E Register Address:0x0009 Default:0x0380			
Bit	**Name**	**Description**	**Access**
11:8	RESERVED	For TI use only. (Default 4'b0011)	RW
5	HS_CH_SYNC_OVERLAY	0 = LOSx pin does not reflect receive channel loss of block lock (Default 1'b0) 1 = Allows channel loss of block lock to be reflected on LOSx pin	RW
4	HS_INVALID_CODE_OVERLAY	0 = LOSx pin does not reflect receive channel invalid code word error (Default 1'b0) 1 = Allows invalid code word error to be reflected on LOSx pin	RW
3	HS_AGCLOCK_OVERLAY	0 = LOSx pin does not reflect HS Serdes AGC unlock status (Default 1'b0) 1 = Allows HS Serdes AGC unlock status to be reflected on LOSx pin	RW
2	HS_AZDONE_OVERLAY	0 = LOSx pin does not reflect HS Serdes auto zero calibration not done status (Default 1'b0) 1 = Allows auto zero calibration not done status to be reflected on LOSx pin	RW
1	HS_PLL_LOCK_OVERLAY	0 = LOSx pin does not reflect loss of HS Serdes PLL lock status (Default 1'b0) 1 = Allows HS Serdes loss of PLL lock status to be reflected on LOSx pin	RW
0	HS_LOS_OVERLAY	0 = LOSx pin does not reflect HS Serdes Loss of signal condition (Default 1'b0) 1 = Allows HS Serdes Loss of signal condition to be reflected on LOSx pin	RW

Table 5-40. LS_OVERLAY_CONTROL

Device Address: 0x1E Register Address:0x000A Default:0x4000			
Bit	**Name**	**Description**	**Access**
12	LS_PLL_LOCK_OVERLAY	0 = LOSx pin does not reflect loss of LS SERDES PLL lock status (Default 1'b0) 1 = Allows LS SERDES loss of PLL lock status to be reflected on LOSx pin	RW
11:8	LS_CH_SYNC_OVERLAY_LN[3:0]	[3] Corresponds to Lane 3, [2] Corresponds to Lane 2 [1] Corresponds to Lane 1, [0] Corresponds to Lane 0 0 = LOSx pin does not reflect LS Serdes lane loss of synchronization condition (Default 1'b0) 1 = Allows LS serdes lane loss of synchronization condition to be reflected on LOSx pin	RW
7:4	LS_INVALID_CODE_OVERLAY_LN[3:0]	[3] Corresponds to Lane 3, [2] Corresponds to Lane 2 [1] Corresponds to Lane 1, [0] Corresponds to Lane 0 0 = LOSx pin does not reflect LS Serdes lane invalid code condition (Default 1'b0) 1 = Allows LS serdes lane invalid code condition to be reflected on LOSx pin	RW
3:0	LS_LOS_OVERLAY_LN[3:0]	[3] Corresponds to Lane 3, [2] Corresponds to Lane 2 [1] Corresponds to Lane 1, [0] Corresponds to Lane 0 0 = LOSx pin does not reflect LS Serdes lane Loss of signal condition (Default 1'b0) 1 = Allows LS serdes lane Loss of signal condition to be reflected on LOSx pin	RW

Table 5-41. LOOPBACK_TP_CONTROL

Device Address: 0x1E Register Address:0x000B Default:0x0F30			
Bit	**Name**	**Description**	**Access**
15:14	RESERVED	For TI use only.	RW
13	HS_TP_GEN_EN	0 = Normal operation (Default 1'b0) 1 = Activates test pattern generation selected by bits 30.11.10:8	RW
12	HS_TP_VERIFY_EN	0 = Normal operation (Default 1'b0) 1 = Activates test pattern verification selected by bits 30.11.10:8	RW
11	LS_TEST_PATT_SEL[2]	See selection in 30.11.5:4	RW
10:8	HS_TEST_PATT_SEL[2:0]	Test Pattern Selection. Refer Test pattern procedures section for more information. For KR standard pattern generation and verification, please refer Register 3.42 0xx = NA 100 = NA 101 = 27 - 1 PRBS pattern 110 = 223 - 1 PRBS pattern 111 = 231 - 1 PRBS pattern(Default 3'b111) Errors can be checked by reading HS_ERROR_COUNT register	RW
7	LS_TP_GEN_EN	0 = Normal operation (Default 1'b0) 1 = Activates test pattern generation selected by bits {30.11.11, 30.11.5:4} on the LS side	RW
6	LS_TP_VERIFY_EN	0 = Normal operation (Default 1'b0) 1 = Activates test pattern verification selected by bits {30.11.11, 30.11.5:4} on the LS side	RW
5:4	LS_TEST_PATT_SEL[1:0]	LS Test Pattern Selection LS_TEST_PATT_SEL[2:0]. For KR standard pattern generation and verification, refer 1.32770 and 1.32771 LS_TEST_PATT_SEL[2] is 30.11.11 0xx = NA 100 = NA 101 = 2^7 - 1 PRBS pattern 110 = 2^{23} - 1 PRBS pattern 111 = 2^{31} - 1 PRBS pattern(Default 3'b111)	RW
3	DEEP_REMOTE_LPBK	0 = Normal functional mode (Default 1'b0) 1 = Enable deep remote loopback mode	RW
2	SHALLOW_REMOTE_LPBK	0 = Normal functional mode (Default 1'b0) 1 = Enable shallow remote loopback mode and serial retime mode	RW
1	DEEP_LOCAL_LPBK	0 = Normal functional mode (Default 1'b0) 1 = Enable deep local loopback mode Requires Auto Negotiation and Link training to be disabled.	RW
0	SHALLOW_LOCAL_LPBK	0 = Normal functional mode (Default 1'b0) 1 = Enable shallow local loopback mode Requires Auto Negotiation and Link training to be disabled.	RW

Table 5-42. LS_CONFIG_CONTROL

Device Address: 0x1E Register Address:0x000C Default:0x03F0			
Bit	**Name**	**Description**	**Access**
14	RESERVED	For TI use only (Default 1'b0)	RW
13:12	LS_STATUS_CFG[1:0]	Selects selected lane status to be reflected in LS_STATUS_1 register 0x15 00 = Lane 0 (Default 2'b00) 01 = Lane 1 10 = Lane 2 11 = Lane 3	RW
6	RESERVED	For TI use only. (Default 1'b1)	RW

Table 5-43. RESET_CONTROL

Device Address: 0x1E Register Address:0x000E Default:0x0000			
Bit	**Name**	**Description**	**Access**
3	DATAPATH_RESET	Channel datapath reset control. Required once the desired functional mode is configured. 0 = Normal operation. (Default 1'b0) 1 = Resets channel logic excluding MDIO registers. (Resets both Tx and Rx datapath)	RW SC(1)

(1) After reset bit is set to one, it automatically sets itself back to zero on the next MDC clock cycle.

Table 5-44. CHANNEL_STATUS_1

Device Address: 0x1E Register Address:0x000F Default:0x0000			
Bit	**Name**	**Description**	**Access**
14	LS_ALIGN_STATUS	Lane alignment status 1 = Lane alignment is achieved on the LS side 0 = Lane alignment is not achieved on the LS side	RO/LL
13	HS_LOS	Loss of Signal Indicator. When high, indicates that a loss of signal condition is detected on HS serial receive inputs	RO/LH
12	HS_AZ_DONE	Auto zero complete indicator. When high, indicates auto zero calibration is complete	RO/LL
11	HS_AGC_LOCKED	Adaptive gain control loop lock indicator. When high, indicates AGC loop is in locked state	RO/LL
10	HS_CHANNEL_SYNC	Channel synchronization status indicator. When high, indicates channel synchronization has achieved	RO/LL
9	RESERVED	For TI use only	RO/LH
8	HS_DECODE_INVALID	When high, indicates decoder received an invalid code word. In functional mode, number of DECODE_INVALID errors are reflected in HS_ERROR_COUNTER register (0x10)	RO/LH
7	TX_FIFO_UNDERFLOW	When high, indicates underflow has occurred in the transmit datapath CTC FIFO.	RO/LH
6	TX_FIFO_OVERFLOW	When high, indicates overflow has occurred in the transmit datapath CTC FIFO.	RO/LH
5	RX_FIFO_UNDERFLOW	When high, indicates underflow has occurred in the receive datapath CTC FIFO.	RO/LH
4	RX_FIFO_OVERFLOW	When high, indicates overflow has occurred in the receive datapath CTC FIFO.	RO/LH
1	LS_PLL_LOCK	LS Serdes PLL lock indicator When high, indicates LS Serdes PLL achieved lock to the selected incoming REFCLK0/1_P/N	RO/LL
0	HS_PLL_LOCK	HS Serdes PLL lock indicator When high, indicates HS Serdes PLL achieved lock to the selected incoming REFCLK0/1_P/N	RO/LH

Table 5-45. HS_ERROR_COUNTER

Device Address: 0x1E Register Address:0x0010 Default:0x0000			
Bit	**Name**	**Description**	**Access**
15:0	HS_ERR_COUNT[15:0]	In functional mode, this counter reflects number of invalid code words received by decoder. Reading this register also clears value in 3.33.7:0. In HS test pattern verification mode , this counter reflects error count for the test pattern selected through 30.11.10:8 When PRBS_EN pin is set, this counter reflects error count for selected PRBS pattern. Counter value cleared to 16'h0000 when read.	COR

Table 5-46. LS_LN0_ERROR_COUNTER

Device Address: 0x1E Register Address:0x0011 Default:0xFFFD			
Bit	**Name**	**Description**	**Access**
15:0	LS_LN0_ERR_COUNT[15:0]	Lane 0 Error counter In functional mode, this counter reflects number of invalid code words received by decoder In LS test pattern verification mode , this counter reflects error count for the test pattern selected through 30.11.5:4 Counter value cleared to 16'h0000 when read.	COR

Table 5-47. LS_LN1_ERROR_COUNTER

Device Address: 0x1E Register Address:0x0012 Default:0xFFFD			
Bit	**Name**	**Description**	**Access**
15:0	LS_LN1_ERR_COUNT[15:0]	Lane 1 Error counter In functional mode, this counter reflects number of invalid code words received by decoder In LS test pattern verification mode , this counter reflects error count for the test pattern selected through 30.11.5:4 Counter value cleared to 16'h0000 when read.	COR

Table 5-48. LS_LN2_ERROR_COUNTER

Device Address: 0x1E Register Address:0x0013 Default:0xFFFD			
Bit	**Name**	**Description**	**Access**
15:0	LS_LN2_ERR_COUNT[15:0]	Lane 2 Error counter In functional mode, this counter reflects number of invalid code words received by decoder In LS test pattern verification mode , this counter reflects error count for the test pattern selected through 30.11.5:4 Counter value cleared to 16'h0000 when read.	COR

Table 5-49. LS_LN3_ERROR_COUNTER

Device Address: 0x1E Register Address:0x0014 Default:0xFFFD			
Bit	**Name**	**Description**	**Access**
15:0	LS_LN3_ERR_COUNT[15:0]	Lane 3 Error counter In functional mode, this counter reflects number of invalid code words received by decoder In LS test pattern verification mode , this counter reflects error count for the test pattern selected through 30.11.5:4 Counter value cleared to 16'h0000 when read.	COR

Table 5-50. LS_STATUS_1

Device Address: 0x1E Register Address:0x0015 Default:0x0000			
Bit	**Name**	**Description**	**Access**
14:12	RESERVED	For TI use only.	RO
10	LS_LOS	Loss of Signal Indicator. When high, indicates that a loss of signal condition is detected on LS serial receive inputs for selected lane. Lane can be selected through LS_STATUS_CFG[1:0] (Register 30.12)	RO/LH
9	LS_LN_ALIGN_FIFO_ERR	LS Lane alignment FIFO error status 1 = Lane alignment FIFO on LS side has error 0 = Lane alignment FIFO on LS side has no error	RO/LH
8	LS_CH_SYNC_STATUS	LS Channel sync status for selected lane. Lane can be selected through LS_STATUS_CFG[1:0] (Register 30.12)	RO/LL
3	LS_INVALID_DECODE	LS Invalid decode error for selected lane. Lane can be selected through LS_STATUS_CFG[1:0] (Register 30.12). Error count for each lane can also be monitored through respective LS_LNx_ERR_COUNT registers	RO/LH
2:0	RESERVED	For TI use only.	RO

Table 5-51. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address:0x016 Default:0x0000			
Bit	**Name**	**Description**	**Access**
11:8	RESERVED	For TI use only. (Default 4'b0000)	RW
6:0	RESERVED	For TI use only. (Default 7'b0000000)	

Table 5-52. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address:0x017 Default:0x0000			
Bit	**Name**	**Description**	**Access**
15:0	RESERVED	For TI use only. (Default 16'h0000)	RW

Table 5-53. TI_RESERVED_STATUS

Device Address: 0x01 Register Address:0x018 Default:0x0000			
Bit	**Name**	**Description**	**Access**
15:0	RESERVED	For TI use only. (Default 16'h0000)	RO

Table 5-54. LS_CLKOUT_CONTROL (1)

Device Address: 0x1E Register Address:0x0019 Default: 0x0808			
Bit	**Name**	**Description**	**Access**
15:12	LS1_CLKOUT_DIV[3:0]	LS1_CLKOUT Output clock divide setting. This value is used to divide selected clock (Selected using LS1_CLKOUT_SEL) before giving it out onto LS1_CLKOUTP/N. 0000 = Divide by 1 (Default 4'b0000) 0001 = RESERVED 0010 = RESERVED 0011 = RESERVED 0100 = Divide by 2 0101 = RESERVED 0110 = RESERVED 0111 = RESERVED 1000 = Divide by 4 1001 = Divide by 8 1010 = Divide by 16 1011 = RESERVED 1100 = Divide by 5 1101 = Divide by 10 1110 = Divide by 20 1111 = Divide by 25	RW
11	LS1_CLKOUT_ EN	Output clock enable. 0 = Holds LS1_CLKOUTP/N output to a fixed value. 1 = Allows LS1_CLKOUTP/N output to toggle normally. (Default 1'b1)	RW
10:8	LS1_CLKOUT_SEL[2:0]	Output clock select. Selected LS TXBCLK/RXBCLK sent out on LS1_CLKOUTP/N pins 000 = Selects Ch A LSRXBCLK0 clock as output clock (Default 3'b000) 001 = Selects Ch B LSRXBCLK0 clock as output clock 010 = Selects Ch C LSRXBCLK0 clock as output clock 011 = Selects Ch D LSRXBCLK0 clock as output clock 100 = Selects Ch A LSTXBCLK clock as output clock 101 = Selects Ch B LSTXBCLK clock as output clock 110 = Selects Ch C LSTXBCLK clock as output clock 111 = Selects Ch D LSTXBCLK clock as output clock	RW

(1) This register is channel independent.

Table 5-54. LS_CLKOUT_CONTROL[1] (continued)

Device Address: 0x1E Register Address:0x0019 Default: 0x0808			
Bit	**Name**	**Description**	**Access**
7:4	LS0_CLKOUT_DIV[3:0]	LS0_CLKOUT Output clock divide setting. This value is used to divide selected clock (Selected using LS0_CLKOUT_SEL) before giving it out onto LS0_CLKOUTP/N. 0000 = Divide by 1 (Default 4'b0000) 0001 = RESERVED 0010 = RESERVED 0011 = RESERVED 0100 = Divide by 2 0101 = RESERVED 0110 = RESERVED 0111 = RESERVED 1000 = Divide by 4 1001 = Divide by 8 1010 = Divide by 16 1011 = RESERVED 1100 = Divide by 5 1101 = Divide by 10 1110 = Divide by 20 1111 = Divide by 25	RW
3	LS0_CLKOUT_ EN	Output clock enable. 0 = Holds LS0_CLKOUTP/N output to a fixed value. 1 = Allows LS0_CLKOUTP/N output to toggle normally. (Default 1'b1)	RW
2:0	LS0_CLKOUT_SEL[2:0]	Output clock select. Selected LS TXBCLK/RXBCLK sent out on LS0_CLKOUTP/N pins 000 = Selects Ch A LSRXBCLK0 clock as output clock (Default 3'b000) 001 = Selects Ch B LSRXBCLK0 clock as output clock 010 = Selects Ch C LSRXBCLK0 clock as output clock 011 = Selects Ch D LSRXBCLK0 clock as output clock 100 = Selects Ch A LSTXBCLK clock as output clock 101 = Selects Ch B LSTXBCLK clock as output clock 110 = Selects Ch C LSTXBCLK clock as output clock 111 = Selects Ch D LSTXBCLK clock as output clock	RW

Table 5-55. HS_TX_CLKOUT_CONTROL[1]

Device Address: 0x1E Register Address:0x001A Default: 0x0C0C			
Bit	**Name**	**Description**	**Access**
15:12	HSTX1_CLKOUT_DIV[3:0]	HSTX1_CLKOUT Output clock divide setting. This value is used to divide selected clock (Selected using HSTX1_CLKOUT_SEL) before giving it out onto HSTX1_CLKOUTP/N. 0000 = Divide by 1 (Default 4'b0000) 0001 = RESERVED 0010 = RESERVED 0011 = RESERVED 0100 = Divide by 2 0101 = RESERVED 0110 = RESERVED 0111 = RESERVED 1000 = Divide by 4 1001 = Divide by 8 1010 = Divide by 16 1011 = RESERVED 1100 = Divide by 5 1101 = Divide by 10 1110 = Divide by 20 1111 = Divide by 25	RW
11	HSTX1_CLKOUT_ EN	Output clock enable.1110 = Divide by 20 0 = Holds HSTX1_CLKOUTP/N output to a fixed value.1110 = Divide by 20 1 = Allows HSTX1_CLKOUTP/N output to toggle normally. (Default 1'b1)	RW
10	HSTX1_CLKOUT_POWERDOWN	1 = Enable HSTX1_CLKOUTP/N Power Down (Default 1'b1)1110 = Divide by 20 0 = Normal operation	RW

(1) This register is channel independent.

Table 5-55. HS_TX_CLKOUT_CONTROL[1] (continued)

Device Address: 0x1E Register Address:0x001A Default: 0x0C0C			
Bit	**Name**	**Description**	**Access**
9:8	HSTX1_CLKOUT_SEL[1:0]	Output clock select. Selected HS TXBCLK sent out on HSTX1_ CLKOUTP/N pins 00 = Selects Channel A HSTXBCLK clock as output clock (Default 2'b00) 01 = Selects Channel B HSTXBCLK clock as output clock 10 = Selects Channel C HSTXBCLK clock as output clock 11 = Selects Channel D HSTXBCLK clock as output clock	RW
7:4	HSTX0_CLKOUT_DIV[3:0]	HSTX0_CLKOUT Output clock divide setting. This value is used to divide selected clock (Selected using HSTX0_CLKOUT_SEL) before giving it out onto HSTX0_CLKOUTP/N. 0000 = Divide by 1 (Default 4'b0000) 0001 = RESERVED 0010 = RESERVED 0011 = RESERVED 0100 = Divide by 2 0101 = RESERVED 0110 = RESERVED 0111 = RESERVED 1000 = Divide by 4 1001 = Divide by 8 1010 = Divide by 16 1011 = RESERVED 1100 = Divide by 5 1101 = Divide by 10 1110 = Divide by 20 1111 = Divide by 25	RW
3	HSTX0_CLKOUT_ EN	Output clock enable. 0 = Holds HSTX0_CLKOUTP/N output to a fixed value. 1 = Allows HSTX0_CLKOUTP/N output to toggle normally. (Default 1'b1)	RW
2	HSTX0_CLKOUT_POWERDOWN	0 = Normal operation 1 = Enable HSTX0_CLKOUTP/N Power Down(Default 1'b1)	RW
1:0	HSTX0_CLKOUT_SEL[1:0]	Output clock select. Selected HS TXBCLK sent out on HSTX0_ CLKOUTP/N pins 00 = Selects Channel A HSTXBCLK clock as output clock (Default 2'b00) 01 = Selects Channel B HSTXBCLK clock as output clock 10 = Selects Channel C HSTXBCLK clock as output clock 11 = Selects Channel D HSTXBCLK clock as output clock	RW

Table 5-56. LS_CLKOUT_PWRDWN_CONTROL

Device Address: 0x1E Register Address:0x001B Default: 0x0063			
Bit	**Name**	**Description**	**Access**
6:2	RESERVED	For TI use only (Default 5'b11000)	RW
1	LS1_CLKOUT_POWERDOWN	0 = Normal operation 1 = Enable LS1_CLKOUTP/N Power Down (Default 1'b1)	
0	LS0_CLKOUT_POWERDOWN	0 = Normal operation (Default 1'b1) 1 = Enable LS0_CLKOUTP/N Power Down (Default 1'b1)	

Table 5-57. LS_CH_CONTROL_1

Device Address: 0x1E Register Address:0x001C Default: 0x0000			
Bit	**Name**	**Description**	**Access**
6	RESERVED	For TI use only	RW/SC
5:2	RESERVED	For TI use only (Default 4'b0000)	RW
1:0	LS_CH_SYNC_HYS_SEL[1:0]	LS Channel synchronization hysteresis selection for selected lane. Lane can be selected in LS_SERDES_CONTROL_1. 00 = The channel synchronization, when in the synchronization state, performs the Ethernet standard specified hysteresis to return to the LOS state (Default 2'b00) 01 = A single 8b/10b invalid decode error or disparity error causes the channel synchronization state machine to immediately transition from sync to LOS 10 = Two adjacent 8b/10b invalid decode errors or disparity errors cause the channel synchronization state machine to immediately transition from sync to LOS 11 = Three adjacent 8b/10b invalid decode errors or disparity errors cause the channel synchronization state machine to immediately transition from sync to LOS	

Table 5-58. HS_CH_CONTROL_1

Device Address: 0x1E Register Address:0x001D Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15	RESERVED	For TI use only (Default 1'b0)	RW
14	RESERVED	For TI use only (Default 1'b0)	
13	REFCLK_FREQ_SEL_1	Input REFCLK frequency selection MSB. When set, HS_PLL_MULT, LS_MPY and HS/LS TX/RX RATE settings can be set through related control bits specified in registers 30.2, 30.3, 30.6 0 = HS_PLL_MULT, LS_MPY and HS/LS TX/RX RATE are set automatically based on input REFCLK frequency as specified in REFCLK_FREQ_SEL_0(30.29.12) (Default 1'b0) 1 = Set this value if HS_PLL_MULT, LS_MPY and HS/LS TX/RX RATE values are NOT to be set automatically.	RW
12	REFCLK_FREQ_SEL_0	Input REFCLK frequency selection LSB. Applicable when REFCLK_FREQ_SEL_1(30.29.13) is set to 0. 0 = Set this value if REFCLK frequency is 156.25 MHz (Default 1'b0) 1 = Set this value if REFCLK frequency is 312.5 MHz	RW
11	RX_CTC_BYPASS	0 = Normal operation. (Default 1'b0) 1 = Disables RX CTC operation.	RW
10	TX_CTC_BYPASS	0 = Normal operation. (Default 1'b0) 1 = Disables TX CTC operation.	RW

The registers below can be accessed directly through Clause 45. Contains mode specific control/status registers and implemented per channel basis.

Table 5-59. TI_RESERVED_STATUS

Device Address: 0x1E Register Address:0x8015 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	RESERVED	For TI use only	RO

Table 5-60. VS_SERDES_CFG_OVERRIDE_CTRL

Device Address: 0x1E Register Address:0x8020 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15	LS_PLL_MULT_OVERRIDE	1 = Override PLL_MULT value going into LS Serdes with MDIO configured value(Default 1'b0)	RW
14	LS_RATE_ OVERRIDE	1 = Override RATE value going into LS Serdes with MDIO configured value(Default 1'b0)	
13	HS_PLL_MULT_OVERRIDE	1 = Override PLL_MULT value going into HS Serdes with MDIO configured value(Default 1'b0)	
12	HS_RATE_OVERRIDE	1 = Override RATE value going into HS Serdes with MDIO configured value(Default 1'b0)	
10	RESERVED	For TI use only (Default 1'b0)	
9	HS_FIRUPT_OVERRIDE	1 = Override FIRUPT value going into HS Serdes with MDIO configured value(Default 1'b0). This bit should be set to 1 for proper 10GKR operation.	
8	HS_ENRX_OVERRIDE	1 = Override ENRX value going into HS Serdes with MDIO configured value(Default 1'b0)	
7	HS_AZCAL_OVERRIDE	1 = Override AZCAL value going into HS Serdes with MDIO configured value(Default 1'b0)	
6	HS_ENTRACK_OVERRIDE	1 = Override ENTRACK value going into HS Serdes with MDIO configured value(Default 1'b0)	
5	HS_EQHLD_OVERRIDE	1 = Override EQHLD value going into HS Serdes with MDIO configured value(Default 1'b0)	
4	HS_TWCRF_OVERRIDE	1 = Override TWCRF value going into HS Serdes with MDIO configured value(Default 1'b0)	
3	HS_TWPOST2_OVERRIDE	1 = Override TWPOST2 value going into HS Serdes with MDIO configured value(Default 1'b0)	
2	HS_TWPOST_OVERRIDE	1 = Override TWPOST value going into HS Serdes with MDIO configured value (Default 1'b0)	
1	HS_TWPRE_OVERRIDE	1 = Override TWPRE value going into HS Serdes with MDIO configured value(Default 1'b0)	
0	HS_SWING_OVERRIDE	1 = Override SWING value going into HS Serdes with MDIO configured value (Default 1'b0)	

Table 5-61. AUTO_CLKOUT_CONTROL

Device Address: 0x1E Register Address:0x8021 Default: 0x000F			
Bit	**Name**	**Description**	**Access**
7	RESERVED	For TI use only (Default 1'b0)	RW
6	RESERVED	For TI use only (Default 1'b0) Must be set to 1.	RW
5	RESERVED	For TI use only (Default 1'b0) Must be set to 1.	RW
4	RESERVED	For TI use only (Default 1'b0)	RW
3	RX_CLKOUT_EN_AUTO_ DISABLE	This bit controls the signal which flat lines RX CLKOUT 1 = RX CLKOUT clock flat lined if HS PLL lock is lost or if HS LOS is detected (Default 1'b1) 0 = RX CLKOUT clock not flat lined if HS PLL lock is lost or if HS LOS is detected Must be set to 1.	RW
2	RX_CLKOUT_PWRDWN_ AUTO_DISABLE	This bit controls the signal which power down RX CLKOUT output buffer 1 = RX CLKOUT output buffer powered down if HS PLL lock is lost or if HS LOS is detected (Default 1'b1) 0 = RX CLKOUT output buffer not powered down if HS PLL lock is lost or if HS LOS is detected Must be set to 1.	RW
1	RESERVED	For TI use only (Default 1'b1) Must be set to 1.	RW

Table 5-61. AUTO_CLKOUT_CONTROL (continued)

Device Address: 0x1E Register Address:0x8021 Default: 0x000F			
Bit	**Name**	**Description**	**Access**
0	RESERVED	For TI use only (Default 1'b1) Must be set to 1.	RW

Table 5-62. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address:0x8022 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	RESERVED	For TI use only (Default 16'h0000)	RW

Table 5-63. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address:0x8023 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	RESERVED	For TI use only (Default 16'h0000)	RW

Table 5-64. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address:0x8024 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	RESERVED	For TI use only (Default 16'h0000)	RW

Table 5-65. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address:0x8030 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
13:0	RESERVED	For TI use only	RO

Table 5-66. VS_HS_SERDES_STATUS_1

Device Address: 0x1E Register Address:0x8031 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:14	HS_FINAL_AZCAL[1:0]	Final HS Serdes AZCAL control	RO
13	HS_FINAL_FIRUPT	Final HS Serdes Tx pre/post cursor filter update control	
12:8	HS_ FINAL_TWPOST1[4:0]	Final Adjacent post cursor1 Tap weight. Selects TAP settings for TX waveform.	
7:4	HS_ FINAL_TWPRE[3:0]	Final Pre cursor Tap weight. Selects TAP settings for TX waveform	
3:0	HS_ FINAL_TWPOST2[3:0]	Final Adjacent post cursor2 Tap weight. Selects TAP settings for TX waveform.	

Table 5-67. VS_HS_SERDES_STATUS_2

Device Address: 0x1E Register Address:0x8032 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
11	HS_ FINAL_ENRX	Final HS Serdes enable rx control value	RO
10	HS_ FINAL_ENTRACK	Final HS Serdes entrack value	
9	HS_ FINAL_EQHLD	Final HS Serdes EQHLD value	
8:4	HS_FINAL_TWCRF[4:0]	Final cursor reduction factor weights value.	
3:0	HS_ FINAL_SWING[3:0]	Final Swing control value.	

Table 5-68. VS_HS_SERDES_STATUS_3

Device Address: 0x1E Register Address:0x8033 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
11:10	RESERVED	For TI use only	RO
9:8	HS_FINAL_RATE_TX[1:0]	Final HS Serdes TX RATE value	
6:4	HS_FINAL_RATE_RX[2:0]	Final HS Serdes RX RATE value.	
3:0	HS_ FINAL_PLL_MULT[3:0]	Final HS Serdes PLL Multipler control value.	

Table 5-69. VS_LS_SERDES_STATUS

Device Address: 0x1E Register Address:0x8034 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
9:8	LS_FINAL_RATE_TX[1:0]	Final LS Serdes TX RATE value	RO
5:4	LS_FINAL_RATE_RX[1:0]	Final LS Serdes RX RATE value.	
3:0	LS_ FINAL_PLL_MULT[3:0]	Final LS Serdes PLL Multipler control value.	

Table 5-70. TI_RESERVED_STATUS

Device Address: 0x1E Register Address:0x8035 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
7	RESERVED	For TI use only	RO
4:0	RESERVED	For TI use only	

Table 5-71. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address:0x8030 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
3:0	RESERVED	For TI use only (Default 4'b0000)	RW

Table 5-72. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address:0x8100 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
10:0	RESERVED	For TI use only (Default 11'b000000000000)	RW

Table 5-73. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address:0x8101 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
13:0	RESERVED	For TI use only (Default 11'b000000000000)	RW

The registers below can be accessed directly through Clause 45. Contains device specific debug control/status registers and not implemented per channel basis (i.e. same physical register accessed irrespective of channel addressed).

Table 5-74. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address:0x9000 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
11:8	RESERVED	For TI use only. (Default 4'b0000)	RW
5:4	RESERVED	For TI use only. (Default 2'b00)	
0	RESERVED	For TI use only. (Default 1'b0)	

5.6.1.2 PMA/PMD Registers

The registers below can be accessed only in Clause 45 mode and with device address field set to 0x01 (DA[4:0] = 5'b00001).

Table 5-75. PMA_CONTROL_1

Device Address: 0x01 Register Address:0x0000 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15	RESET	1 = Global reset. Resets datapath and MDIO registers of all channels. Equivalent to asserting RESET_N. 0 = Normal operation (Default 1'b0)	RW/SC
11	POWERDOWN	1 = Enable power down mode 0 = Normal operation (Default 1'b0)	RW
0	LOOPBACK	1 = Enables loopback on HS serial side. LS data traverses through entire Tx datapath including HS serdes and will be available at LS output side 0 = Normal operation (Default 1'b0)	RW

Table 5-76. PMA_DEV_IDENTIFIER_1

Device Address: 0x01 Register Address: 0x0001 Default: 0x0002			
Bit	**Name**	**Description**	**Access**
7	FAULT	1 = Fault condition detected 0 = No fault condition detected This bit is cleared after Register 1.8 is read and no fault condition occurs after 1.8 is read.	RO
2	RX_LINK	1 = Receive link is up 0 = Receive link is down	RO/LL
1	LOW_POWER_ABILITY	Always reads 1. 1 = Supports low power mode 0 = Does not support low power mode	RO

Table 5-77. PMA_DEV_IDENTIFIER_1

Device Address: 0x01 Register Address:0x0002 Default: 0x4000			
Bit	**Name**	**Description**	**Access**
15:0	DEV_IDENTIFIER[31:16]	16 MSB of 32 bit unique device identifier. See Table 5-79 for identifier code details.	RO

Table 5-78. PMA_DEV_IDENTIFIER_2

Device Address: 0x01 Register Address:0x0003 Default: 0x50F0			
Bit	**Name**	**Description**	**Access**
15:0	DEV_IDENTIFIER[15:0]	16 LSB of 32 bit unique device identifier. SeeTable 5-79 for identifier code details	RO

Table 5-79. UNIQUE DEVICE IDENTIFIER(1)

Register address	Value	Description
15:0	16'b0100_0000_0000_0000	OUI[3-18]
15:10	6'b010100	OUI[19-24]
9:4	6'b001111	6-bit Manufacturer device model number
3:0	4'b0000	4-bit Manufacturer device revision number

(1) The identifier code is composed of bits 3-24 of 25-bit organizationally unique identifier (OUI) assigned to Texas Instruments by IEEE. The 6-bit Manufacturer device model number is unique to TLK10034. The 4-bit Manufacturer device revision number denotes the current revision of TLK10034.

Table 5-80. PMA_SPEED_ABILITY

Device Address: 0x01 Register Address: 0x0004 Default: 0x0011			
Bit	**Name**	**Description**	**Access**
4	SPEED_1G	Always reads 1. 1 = Capable of operating at 1000 Mb/s 0 = Not capable of operating at 1000 Mb/s	RO
0	SPEED_10G	Always reads 1. 1 = Capable of operating at 10 Gb/s 0 = Not capable of operating at 10 Gb/s	RO

Table 5-81. PMA_DEV_PACKAGE_1

Device Address: 0x01 Register Address: 0x0005 Default: 0x000B			
Bit	**Name**	**Description**	**Access**
3	PCS_ PRESENT	Always reads 1. 1 = PCS present in the package 0 = PCS not present in the package	RO
1	PMA_PMD_PRESENT	Always reads 1. 1 = PMA/PMD present in the package 0 = PMA/PMD not present in the package	
0	CL22_PRESENT	Always reads 1. 1 = Clause 22 registers present in the package 0 = Clause 22 registers not present in the package	

Table 5-82. PMA_DEV_PACKAGE_2

Device Address: 0x01 Register Address: 0x0006 Default: 0x4000			
Bit	**Name**	**Description**	**Access**
15	VS_DEV2_PRESENT	Always reads 0. 1 = Vendor specific device 2 present in the package 0 = Vendor specific device 2 not present in the package	RO
14	VS_DEV1_PRESENT	Always reads 1. 1 = Vendor specific device 1 present in the package 0 = Vendor specific device 1 not present in the package	RO

Table 5-83. PMA_STATUS_2

Device Address: 0x01 Register Address: 0x0008 Default: 0xB000			
Bit	**Name**	**Description**	**Access**
15:14	DEV_PRESENT	Always reads 2'b10 0x = No device responding at this address 10 = Device responding at this address 11 = No device responding at this address	RO
13	TX_FAULT_ABILITY	Always reads 1'b1. 1 = Able to detect fault condition on Tx path 0 = Not able to detect fault condition on Tx path	RO
12	RX_FAULT_ABILITY	Always reads 1'b1. 1 = Able to detect fault condition on Rx path 0 = Not able to detect fault condition on Rx path	RO
11	TX_FAULT	1 = Fault condition detected on transmit path 0 = No fault condition detected on transmit path	RO/LH
10	RX_FAULT	1 = Fault condition detected on receive path 0 = No fault condition detected on receive path	RO/LH
8	TX_DISABLE_ABILITY	Always reads 1'b0. 1 = Able to perform transmit disable function 0 = Not able to perform transmit disable function	RO

Table 5-84. PMA_RX_SIGNAL_DET_STATUS

Device Address: 0x01 Register Address: 0x000A Default: 0x0000			
Bit	**Name**	**Description**	**Access**
0	RX_SIGNAL_DET	1 = Signal detected on serial Rx pins 0 = Signal not detected on serial Rx pins	RO

Table 5-85. PMA_EXTENDED_ABILITY

Device Address: 0x01 Register Address: 0x000B Default: 0x0050			
Bit	**Name**	**Description**	**Access**
6	KX_ABILITY	Always reads 1'b11 = Able to perform 1000BASE-KX 0 = Not able to perform 1000BASE-KX	RO
4	KR_ABILITY	Always reads 1'b11 = Able to perform 10GBASE-KR 0 = Not able to perform 10GBASE-KR	RO

Table 5-86. KR_TRAIN_CONTROL

Device Address: 0x01 Register Address: 0x0096 Default: 0x0002			
Bit	**Name**	**Description**	**Access**
1	KR_TRAINING_ENABLE	1 = Enable 10GBASE-KR start-up protocol (Default 1'b1) 0 = Disable 10GBASE-KR start-up protocol	RW
0	KR_RESTART_TRAINING	1 = Reset 10GBASE-KR start-up protocol 0 = Normal operation (Default 1'b0)	RW/SC

Table 5-87. KR_TRAIN_STATUS

Device Address: 0x01 Register Address: 0x0097 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
1.3	KR_TRAINING_FAIL	1 = Training failure has been detected 0 = Training failure has not been detected	RO
2	KR_START_PROTOCOL	1 = Start up protocol in progress 0 = Start up protocol complete	
1	KR_FRAME_LOCK	1 = Training frame delineation detected 0 = Training frame delineation not detected	
0	KR_RX_STATUS	1 = Receiver trained and ready to receive data 0 = Receiver training in progress	

Table 5-88. KR_LINK_PARTNER_CONTROL

Device Address: 0x01 Register Address: 0x0098 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
13	KR_LP_PRESET	1 = KR preset coefficients 0 = Normal operation	RO
12	KR_LP_INITIALIZE	1 = Initialize KR coefficients 0 = Normal operation	RO
9:8	KR_LP_COEFF_SWG	Swing update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold	RO
7:6	KR_LP_COEFF_PS2	Post2 tap control update 11 = Reserved01 = Increment 10 = Decrement 00 = Hold	RO
5:4	KR_LP_COEFF_P1	Coefficient K(+1) update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold	RO

Table 5-88. KR_LINK_PARTNER_CONTROL (continued)

Device Address: 0x01 Register Address: 0x0098 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
3:2	KR_LP_COEFF_0	Coefficient K(0) update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold	RO
1:0	KR_LP_COEFF_M1	Coefficient K(-1) update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold (Default 2'b00)	RO

Table 5-89. KR_LINK_PARTNER_STATUS

Device Address: 0x01 Register Address: 0x0099 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15	KR_LP_RX_READY	1 = LP receiver has determined that training is complete and prepared to receive data 0 = LP receiver is requesting that training continue	RO
9:8	KR_LP_COEFF_SWG_STAT	Swing update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	RO
7:6	KR_LP_COEFF_PS2_STAT	Post2 tap control update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	RO
5:4	KR_LP_COEFF_P1_STAT	Plus 1 update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	RO
3:2	KR_LP_COEFF_0_STAT	0 update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	RO
1:0	KR_LP_COEFF_M1_STAT	Minus 1 update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	RO

Table 5-90. KR_LOCAL_DEVICE_CONTROL

Device Address: 0x01 Register Address: 0x009A Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15	RESERVED	For TI use only (Default 1'b0)	RW
13	KR_LD_PRESET	1 = KR preset coefficients 0 = Normal operation (Default 1'b0)	RO
12	KR_ LD_INITIALIZE	1 = Initialize KR coefficients 0 = Normal operation (Default 1'b0)	RO
9:8	KR_LD_COEFF_SWG	Swing update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold (Default 2'b00)	RO

Table 5-90. KR_LOCAL_DEVICE_CONTROL (continued)

Device Address: 0x01 Register Address: 0x009A Default: 0x0000			
Bit	**Name**	**Description**	**Access**
7:6	KR_LD_COEFF_PS2	Post2 tap control update 11 = Reserved01 = Increment 10 = Decrement 00 = Hold (Default 2'b00)	RO
5:4	KR_ LD_COEFF_P1	Coefficient K(+1) update 11 = Reserved01 = Increment 10 = Decrement 00 = Hold (Default 2'b00)	RO
3:2	KR_ LD_COEFF_0	Coefficient K(0) update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold (Default 2'b00)	RO
1:0	KR_ LD_COEFF_M1	Coefficient K(-1) update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold (Default 2'b00)	RO

Table 5-91. KR_LOCAL_DEVICE_STATUS

Device Address: 0x01 Register Address: 0x009B Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15	KR_ LD_RX_READY	1 = LD receiver has determined that training is complete and prepared to receive data 0 = LD receiver is requesting that training continue	RO
5:4	KR_ LD_COEFF_P1_STAT	Plus 1 update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	RO
3:2	KR_ LD_COEFF_0_STAT	0 update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	RO
1:0	KR_ LD_COEFF_M1_STAT	Minus 1 update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	RO

Table 5-92. KR_FEC_ABILITY

Device Address: 0x01 Register Address: 0x00AA Default: 0x0003			
Bit	**Name**	**Description**	**Access**
1	KR_FEC_ERR_ABILITY	Always reads 1. 1 = Device supports 10GBASE-R FEC error indication to PCS 0 = Device does not support 10GBASE-R FEC function error indication tx PCS	RO
0	KR_FEC_ABILITY	Always reads 1. 1 = Device supports 10GBASE-R FEC function 0 = Device does not support 10GBASE-R FEC function	

Table 5-93. KR_FEC_CONTROL

Device Address: 0x01 Register Address: 0x00AB Default: 0x0000			
Bit	**Name**	**Description**	**Access**
1	KR_FEC_ERR_IND_EN	1 = Enable FEC decoder to indicate errors to PCS 0 = Disable FEC decoder error indication to PCS (Default 1'b0)	RW
0	KR_FEC_EN	1 = Enable 10GBASE-R FEC function0 = Disable 10GBASE-R FEC function (Default 1'b0)	

Table 5-94. KR_FEC_C_COUNT_1 (1)

Device Address: 0x01 Register Address: 0x00AC Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	KR_FEC_C_COUNT[15:0]	Lower 16 bits of FEC corrected blocks counter	COR

(1) To get correct 32 bit counter value of KR_FEC_C_COUNT, Register 1.172 should be read first followed by Register 1.173

Table 5-95. KR_FEC_C_COUNT_2

Device Address: 0x01 Register Address: 0x00AD Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	KR_FEC_C_COUNT[31:16]	Upper 16 bits of FEC corrected blocks counter	COR

Table 5-96. KR_FEC_UC_COUNT_1 (1)

Device Address: 0x01 Register Address: 0x00AE Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	KR_FEC_UC_COUNT[15:0]	Lower 16 bits of FEC Uncorrected blocks counter	COR

(1) To get correct 32 bit counter value of KR_FEC_UC_COUNT, Register 1.174 should be read first followed by Register 1.175

Table 5-97. KR_FEC_UC_COUNT_2

Device Address: 0x01 Register Address: 0x00AF Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	KR_FEC_UC_COUNT[31:16]	Lower 16 bits of FEC Uncorrected blocks counter	COR

Table 5-98. TI_RESERVED_CONTROL

Device Address: 0x01 Register Address: 0x8000 Default: 0x4800			
Bit	**Name**	**Description**	**Access**
15:8	RESERVED	For TI use only (Default 8'b01001000)	RW
5	RESERVED	For TI use only (Default 1'b0)	RW/SC
4	RESERVED	For TI use only (Default 1'b0)	RW
1:0	RESERVED	For TI use only (Default 2'b00)	RW

Table 5-99. KR_VS_FIFO_CONTROL_1

Device Address: 0x01 Register Address: 0x8001 Default: 0xCC4C			
Bit	**Name**	**Description**	**Access**
15	RESERVED	For TI use only (Default 1'b1)	RW
14:12	RX_FIFO_DEPTH[2:0]	Rx CTC FIFO depth selection 1xx = 32 deep (Default 3'b100) 011 = 24 deep 010 = 16 deep 001 = 12 deep 000 = 8 deep (No CTC function)	RW

Table 5-99. KR_VS_FIFO_CONTROL_1 (continued)

Device Address: 0x01 Register Address: 0x8001 Default: 0xCC4C			
Bit	**Name**	**Description**	**Access**
11:10	RX_CTC_WMK_SEL[1:0]	Water mark selection for receive CTC Works in conjunction with RX_FIFO_DEPTH_SEL setting (Default 2'b11) Depth-> 32 / 24 / 26 / 12/8 11: High / High / High / NA 10: Mid-high / Mid / High 01: Mid / Low / Low 00: Low / Low / Low	RW
9	RX_Q_CNT_IPG	0 = Normal operation. (Default 1'b0) 1 = Sequence columns are counted as IPG.	RW
8	RX_CTC_Q_DROP_EN	0 = Normal operation. (Default 1'b0) 1 = Enable Q column drop in RX CTC.	RW
7	XMIT_IDLE	1 = Transmit idle pattern onto LS side 0 = Normal operation (Default 1'b0)	RW
6:4	TX_FIFO_DEPTH[2:0]	Tx CTC FIFO depth selection 1xx = 32 deep (Default 3'b100)011 = 24 deep 010 = 16 deep001 = 12 deep 000 = 8 deep (No CTC function)	RW
3:2	TX_CTC_WMK_SEL[1:0]	Water mark selection for receive CTC Works in conjunction with TX_FIFO_DEPTH_SEL setting (Default 2'b11) Depth-> 32 / 24 / 26 / 12/8 11: High / High / High / NA 10: Mid-high / Mid / High 01: Mid / Low / Low 00: Low / Low / Low	RW
1	TX_Q_CNT_IPG	0 = Normal operation. (Default 1'b0) 1 = Sequence columns are counted as IPG.	RW
0	TX_CTC_Q_DROP_EN	0 = Normal operation. (Default 1'b0) 1 = Enable Q column drop in TX CTC.	RW

Table 5-100. KR_VS_TP_GEN_CONTROL

Device Address: 0x01 Register Address:0x8002 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
5:4	RX_TPG_HLM_TEST_SEL[1:0]	XAUI based test pattern selection on LS side. See Test procedures for more information. 00 = High Frequency test pattern(Default 2'b00) 01 = Low Frequency test pattern 10 = Mixed Frequency test pattern 11 = Normal operation	RW
3	RX_TPG_CRPAT_TEST_EN	XAUI based test pattern selection on LS side. See Test procedures for more information. 0 = Normal operation. (Default 1'b0) 1 = Enables CRPAT test pattern generation	
2	RX_TPG_CJPAT_TEST_EN	XAUI based test pattern selection on LS side. See Test procedures for more information. 0 = Normal operation. (Default 1'b0) 1 = Enables CJPAT test pattern generation	
1	RESERVED	For TI use only (Default 1'b0)	
0	RX_TPG_HLM_TEST_EN	XAUI based test pattern selection on LS side. See Test procedures for more information. 0 = Normal operation. (Default 1'b0) 1 = Enables H/L/M test pattern generation	

Table 5-101. KR_VS_TP_VER_CONTROL

Device Address: 0x01 Register Address:0x8003 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
13:12	TX_TPV_HLM_TEST_SEL[1:0]	XAUI based test pattern selection on LS side. See Test procedures for more information. 00 = High Frequency test pattern(Default 2'b00) 01 = Low Frequency test pattern 10 = Mixed Frequency test pattern 11 = Normal operation	RW
11	TX_TPV_CRPAT_TEST_EN	XAUI based test pattern selection on LS side. See Test procedures for more information. 0 = Normal operation. (Default 1'b0) 1 = Enables CRPAT test pattern verification	RW
10	TX_TPV_CJPAT_TEST_EN	XAUI based test pattern selection on LS side. See Test procedures for more information. 0 = Normal operation. (Default 1'b0) 1 = Enables CJPAT test pattern verification	RW
9	RESERVED	For TI use only(Default 1'b0)	RW
8	TX_TPV_HLM_TEST_EN	XAUI based test pattern selection on LS side. See Test procedures for more information. 0 = Normal operation. (Default 1'b0) 1 = Enables HL/M test pattern verification	RW
5:0	RESERVED	For TI use only(Default 6'b000000)	RW

Table 5-102. KR_VS_CTC_ERR_CODE_LN0

Device Address: 0x01 Register Address: 0x8005 Default: 0xCE00			
Bit	**Name**	**Description**	**Access**
15:7	KR_CTC_ERR_CODE_LN0	XGMII code to be transmitted in case of error condition. This applies to both TX and RX data paths. The msb is the control bit; remaining 8 bits constitute the error code. The default value for lane 0 corresponds to 8'h9C with the control bit being 1'b1. The default values for lanes 0~3 correspond to ||LF||	RW

Table 5-103. KR_VS_CTC_ERR_CODE_LN1

Device Address: 0x01 Register Address: 0x8006 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:7	KR_CTC_ERR_CODE_LN1	XGMII code to be transmitted in case of error condition. This applies to both TX and RX data paths. The msb is the control bit; remaining 8 bits constitute the error code. The default value for lane 1 corresponds to 8'h00 with the control bit being 1'b0. The default values for lanes 0~3 correspond to ||LF||	RW

Table 5-104. KR_VS_CTC_ERR_CODE_LN2

Device Address: 0x01 Register Address: 0x8007 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:7	KR_CTC_ERR_CODE_LN2	XGMII code to be transmitted in case of error condition. This applies to both TX and RX data paths. The msb is the control bit; remaining 8 bits constitute the error code. The default value for lane 2 corresponds to 8'h00 with the control bit being 1'b0. The default values for lanes 0~3 correspond to ||LF||	RW

Table 5-105. KR_VS_CTC_ERR_CODE_LN3

Device Address: 0x01 Register Address: 0x8008 Default: 0x0080			
Bit	**Name**	**Description**	**Access**
15:7	KR_CTC_ERR_CODE_LN3	XGMII code to be transmitted in case of error condition. This applies to both TX and RX data paths. The msb is the control bit; remaining 8 bits constitute the error code. The default value for lane 3 corresponds to 8'h01 with the control bit being 1'b0. The default values for lanes 0~3 correspond to ||LF||	RW

Table 5-106. KR_VS_LN0_EOP_ERROR_COUNTER

Device Address: 0x01 Register Address: 0x8010 Default: 0xFFFD			
Bit	**Name**	**Description**	**Access**
15:0	KR_LN0_EOP_ERR_COUNT	Lane 0 End of packet Error counter. End of packet error is detected when Terminate character is in lane 0 and one or both of the following holds: ● Terminate character is not followed by /K/ characters in lanes 1, 2 and 3 ● The column following the terminate column is neither ||K|| nor ||A||. Counter value cleared to 16'h0000 when read.	COR

Table 5-107. KR_VS_LN1_EOP_ERROR_COUNTER

Device Address: 0x01 Register Address: 0x8011 Default: 0xFFFD			
Bit	**Name**	**Description**	**Access**
15:0	KR_LN1_EOP_ERR_COUNT	Lane 1 End of packet Error counter. End of packet error is detected when Terminate character is in lane 1 and one or both of the following holds: ● Terminate character is not followed by /K/ characters in lanes 2 and 3 ● The column following the terminate column is neither ||K|| nor ||A||. Counter value cleared to 16'h0000 when read.	COR

Table 5-108. KR_VS_LN2_EOP_ERROR_COUNTER

Device Address: 0x01 Register Address: 0x8012 Default: 0xFFFD			
Bit	**Name**	**Description**	**Access**
15:0	KR_LN2_EOP_ERR_COUNT	Lane 2 End of packet Error counter. End of packet error is detected when Terminate character is in lane 2 and one or both of the following holds: ● Terminate character is not followed by /K/ characters in lane 3 ● The column following the terminate column is neither ||K|| nor ||A||. Counter value cleared to 16'h0000 when read.	COR

Table 5-109. KR_VS_LN3_EOP_ERROR_COUNTER

Device Address: 0x01 Register Address: 0x8013 Default: 0xFFFD			
Bit	**Name**	**Description**	**Access**
15:0	KR_LN3_EOP_ERR_COUNT	Lane 3 End of packet Error counter. End of packet error is detected when Terminate character is in lane 3 and the column following the terminate column is neither ||K|| nor ||A||. Counter value cleared to 16'h0000 when read.	COR

Table 5-110. KR_VS_TX_CTC_DROP_COUNT

Device Address: 0x01 Register Address: 0x8014 Default: 0xFFFD			
Bit	**Name**	**Description**	**Access**
15:0	TX_CTC_DROP_COUNT	Counter for number of idle drops in the transmit CTC.	COR

Table 5-111. KR_VS_TX_CTC_INSERT_COUNT

Device Address: 0x01 Register Address: 0x8015 Default: 0xFFFD			
Bit	**Name**	**Description**	**Access**
15:0	TX_CTC_INS_COUNT	Counter for number of idle inserts in the transmit CTC.	COR

Table 5-112. KR_VS_RX_CTC_DROP_COUNT

Device Address: 0x01 Register Address: 0x8016 Default: 0xFFFD			
Bit	**Name**	**Description**	**Access**
15:0	RX_CTC_DROP_COUNT	Counter for number of idle drops in the receive CTC.	COR

Table 5-113. KR_VS_RX_CTC_INSERT_COUNT

Device Address: 0x01 Register Address: 0x8017 Default: 0xFFFD			
Bit	**Name**	**Description**	**Access**
15:0	RX_CTC_INS_COUNT	Counter for number of idle inserts in the receive CTC.	COR

Table 5-114. KR_VS_STATUS_1

Device Address: 0x01 Register Address: 0x8018 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15	TX_TPV_TP_SYNC	0 = Test pattern sync is not achieved on on Tx side 1 = Test pattern sync is achieved on on Tx side	RO
11	RESERVED	For TI use only	
5	INVALID_S_COL_ERR	1 = Indicates invalid start (S) column error detected	RO/LH
4	INVALID_T_COL_ERR	1 = Indicates invalid terminate (T) column error detected	
3	INVALID_XGMII_LN3	1 = Indicates invalid XGMII character detected in Lane 3	
2	INVALID_XGMII_LN2	1 = Indicates invalid XGMII character detected in Lane 2	
1	INVALID_XGMII_LN1	1 = Indicates invalid XGMII character detected in Lane 1	
0	INVALID_XGMII_LN0	1 = Indicates invalid XGMII character detected in Lane 0	

Table 5-115. KR_VS_TX_CRCJ_ERR_COUNT_1

Device Address: 0x01 Register Address: 0x8019 Default: 0xFFFF			
Bit	**Name**	**Description**	**Access**
15:0	TX_TPV_CR_CJ_ERR_COUNT[31:16]	Error Counter for CR/CJ test pattern verification on Tx side. MSBs [31:16]	COR

Table 5-116. KR_VS_TX_CRCJ_ERR_COUNT_2

Device Address: 0x01 Register Address: 0x801A Default: 0xFFFD			
Bit	**Name**	**Description**	**Access**
15:0	TX_TPV_CR_CJ_ERR_COUNT[15:0]	Error Counter for CR/CJ test pattern verification on Tx side LSBs [15:0]	COR

Table 5-117. KR_VS_TX_LN0_HLM_ERR_COUNT

Device Address: 0x01 Register Address: 0x801B Default: 0xFFFD			
Bit	**Name**	**Description**	**Access**
15:0	TX_TPV_LN0_ERR_COUNT[15:0]	Error Counter for H/L/M test pattern verification on Lane 0 of Tx side	COR

Table 5-118. KR_VS_TX_LN1_HLM_ERR_COUNT

Device Address: 0x01 Register Address: 0x801C Default: 0xFFFD			
Bit	**Name**	**Description**	**Access**
1.32796.15:0	TX_TPV_LN1_ERR_COUNT[15:0]	Error Counter for H/L/M test pattern verification on Lane 1 of Tx side	COR

Table 5-119. KR_VS_TX_LN2_HLM_ERR_COUNT

Device Address: 0x01 Register Address: 0x801D Default: 0xFFFD			
Bit	**Name**	**Description**	**Access**
15:0	TX_TPV_LN2_ERR_COUNT[15:0]	Error Counter for H/L/M test pattern verification on Lane 2 of Tx side	COR

Table 5-120. KR_VS_TX_LN3_HLM_ERR_COUNT

Device Address: 0x01 Register Address: 0x801E Default: 0xFFFD			
Bit	**Name**	**Description**	**Access**
15:0	TX_TPV_LN3_ERR_COUNT[15:0]	Error Counter for H/L/M test pattern verification on Lane 3 of Tx side	COR

Table 5-121. TI_RESERVED_CONTROL

Device Address: 0x01 Register Address: 0x9000 Default: 0x0241			
Bit	**Name**	**Description**	**Access**
9:0	RESERVED	For TI use only (Default 10'b1001000001)	RW

Table 5-122. TI_RESERVED_CONTROL

Device Address: 0x01 Register Address: 0x9001 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
12	RESERVED	For TI use only (Default 1'b0)	RW/SC
10:0	RESERVED	For TI use only (Default 11'b00000000000)	RW

Table 5-123. TI_RESERVED_CONTROL

Device Address: 0x01 Register Address: 0x9002 Default: 0x1335			
Bit	**Name**	**Description**	**Access**
12:0	RESERVED	For TI use only (Default 13'h1335)	RW

Table 5-124. TI_RESERVED_CONTROL

Device Address: 0x01 Register Address: 0x9003 Default: 0x5E29			
Bit	**Name**	**Description**	**Access**
152:0	RESERVED	For TI use only (Default 16'h5E29)	RW

Table 5-125. TI_RESERVED_CONTROL

Device Address: 0x01 Register Address: 0x9004 Default: 0x007F			
Bit	**Name**	**Description**	**Access**
12:0	RESERVED	For TI use only (Default 7'h7F)	RW

Table 5-126. TI_RESERVED_CONTROL

Device Address: 0x01 Register Address: 0x9005 Default: 0x0200			
Bit	**Name**	**Description**	**Access**
15:0	RESERVED	For TI use only (Default 16'h0200)	RW

Table 5-127. TI_RESERVED_CONTROL

Device Address: 0x01 Register Address: 0x9006 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	RESERVED	For TI use only (Default 16'h0000)	RW

Table 5-128. TI_RESERVED_STATUS

Device Address: 0x01 Register Address: 0x9010 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
0	RESERVED	For TI use only	RO/LH

Table 5-129. TI_RESERVED_STATUS

Device Address: 0x01 Register Address: 0x9011 Default: 0xFFFD			
Bit	**Name**	**Description**	**Access**
15:0	RESERVED	For TI use only	COR

Table 5-130. TI_RESERVED_STATUS

Device Address: 0x01 Register Address: 0x9012 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	RESERVED	For TI use only	RO

5.6.1.3 PCS Registers

The registers below can be accessed only in Clause 45 mode and with device address field set to 0x03 (DEVADD [4:0] = 5'b00011). Valid only when device is in 10GBASE-KR mode.

Table 5-131. PCS_CONTROL

Device Address: 0x03 Register Address: 0x0000 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15	PCS_RESET	1 = Resets datapath and MDIO registers of all channels. Equivalent to asserting RESET_N. 0 = Normal operation (Default 1'b0)	RW/SC
14	PCS_LOOPBACK	1 = Enables PCS loopback 0 = Normal operation (Default 1'b0) Requires Auto Negotiation and Link Training to be disabled.	RW
11	PCS_LP_MODE	1 = Enable power down mode 0 = Normal operation (Default 1'b0)	RW

Table 5-132. PCS_STATUS_1

Device Address: 0x03 Register Address: 0x0001 Default: 0x0002			
Bit	**Name**	**Description**	**Access**
7	PCS_FAULT	1 = Fault condition detected on either PCS TX or PCS RX 0 = No fault condition detected This bit is cleared after Register 3.8 is read and no fault condition occurs after 3.8 is read.	RO
2	PCS_RX_LINK	1 = PCS receive link is up 0 = PCS receive link is down	RO/LL
1	PCS_LP_ABILITY	Always reads 1. 1 = Supports low power mode 0 = Does not support low power mode	RO

Table 5-133. PCS_STATUS_2

Device Address: 0x03 Register Address: 0x0001 Default: 0x0002			
Bit	**Name**	**Description**	**Access**
15:14	DEV_PRESENT	Always reads 2'b10. 0x = No device responding at this address 10 = Device responding at this address 11 = No device responding at this address	RO
11	PCS_TX_FAULT	1 = Fault condition detected on transmit path 0 = No fault condition detected on transmit path	RO/LH
10	PCS_RX_FAULT	1 = Fault condition detected on receive path 0 = No fault condition detected on receive path	RO/LH
0	PCS_10GBASER_CAPABLE	Always reads 1. 1 = PCS is able to support 10GBASE-R PCS type 0 = PCS not able to support 10GBASE-R PCS type	RO

Table 5-134. KR_PCS_STATUS_1

Device Address: 0x03 Register Address: 0x0020 Default: 0x0004			
Bit	**Name**	**Description**	**Access**
12	PCS_RX_LINK_STATUS	1 = 10GBASE-R PCS receive link up 0 = 10GBASE-R PCS receive link down	RO
2	PCS_PRBS31_ABILITY	Always reads 1. 1 = PCS is able to support PRBS31 pattern testing 0 = PCS is not able to support PRBS31 testing	RO
1	PCS_HI_BER	1 = High BER condition detected 0 = High BER condition not detected	RO
0	PCS_BLOCK_LOCK	1 = PCS locked to receive blocks 0 = PCS not locked to receive blocks	RO

Table 5-135. KR_PCS_STATUS_2

Device Address: 0x03 Register Address: 0x0021 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15	PCS_BLOCK_LOCK_LL	1 = PCS locked to receive blocks 0 = PCS not locked to receive blocks	RO/LL
14	PCS_HI_BER_LH	1 = High BER condition detected 0 = High BER condition not detected	RO/LH
13:8	PCS_BER_COUNT[5:0]	Value indicating number of times BER state machine enters BER_BAD_SH state	COR
7:0	PCS_ERR_BLOCK_COUNT[7:0]	Value indicating number of times RX decode state machine enters RX_E state. Same value is also reflected in 30.16 and reading either register clears the counter value.	COR

Table 5-136. PCS_TP_SEED_A0

Device Address: 0x03 Register Address: 0x0022 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	PCS_TP_SEED_A[15:0]	Test pattern seed A bits 15-0	RW

Table 5-137. PCS_TP_SEED_A1

Device Address: 0x03 Register Address: 0x0023 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
3.35.15:0	PCS_TP_SEED_A[31:16]	Test pattern seed A bits 31-16	RW

Table 5-138. PCS_TP_SEED_A2

Device Address: 0x03 Register Address: 0x0024 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	PCS_TP_SEED_A[47:32]	Test pattern seed A bits 47-32	RW

Table 5-139. PCS_TP_SEED_A3

Device Address: 0x03 Register Address: 0x0025 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
9:0	PCS_TP_SEED_A[57:48]	Test pattern seed A bits 57-48	RW

Table 5-140. PCS_TP_SEED_B0

Device Address: 0x03 Register Address: 0x0026 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	PCS_TP_SEED_B[15:0]	Test pattern seed B bits 15-0	RW

Table 5-141. PCS_TP_SEED_B1

Device Address: 0x03 Register Address: 0x0027 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	PCS_TP_SEED_B[31:16]	Test pattern seed B bits 31-16	RW

Table 5-142. PCS_TP_SEED_B2

Device Address: 0x03 Register Address: 0x0028 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	PCS_TP_SEED_B[47:32]	Test pattern seed B bits 47-32	RW

Table 5-143. PCS_TP_SEED_B3

Device Address: 0x03 Register Address: 0x0029 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
9:0	PCS_TP_SEED_B[57:48]	Test pattern seed B bits 57-48	RW

Table 5-144. PCS_TP_CONTROL

Device Address: 0x03 Register Address: 0x002A Default: 0x0000			
Bit	**Name**	**Description**	**Access**
5	PCS_PRBS31_RX_TP_EN	1 = Enable PRBS31 test pattern verification on receive path 0 = Normal operation (Default 1'b0)	RW
4	PCS_PRBS31_TX_TP_EN	1 = Enable PRBS31 test pattern generation on transmit path 0 = Normal operation (Default 1'b0)	RW
3	PCS_TX_TP_EN	1 = Enable transmit test pattern generation 0 = Normal operation (Default 1'b0)	RW
2	PCS_RX_TP_EN	1 = Enable receive test pattern verification 0 = Normal operation (Default 1'b0)	RW
1	PCS_TP_SEL	1 = Square wave test pattern 0 = Pseudo random test pattern (Default 1'b0)	RW
0	PCS_DP_SEL	1 = 0'S data pattern 0 = LF data pattern (Default 1'b0)	RW

Table 5-145. PCS_TP_ERR_COUNT

Device Address: 0x03 Register Address: 0x002B Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	PCS_TP_ERR_COUNT[15:0]	Test pattern error counter. This counter reflects number of errors occurred during the test pattern mode selected through PCS_TP_CONTROL. In PRBS31 test pattern verification mode, counter value indicates the number of received bytes that have 1 or more bit errors.	COR

Table 5-146. PCS_VS_CONTROL

Device Address: 0x03 Register Address: 0x8000 Default: 0x00B0			
Bit	**Name**	**Description**	**Access**
7:4	PCS_SQWAVE_N	Sets number of repeating 0's followed by repeating 1's during square wave test pattern generation mode (Default 4'1011)	RW
3	RESERVED	For TI use only (Default 1'b0)	RW
2	PCS_RX_DEC_CTRL_CHAR	PCS RX Decode control character selection. Determines what control characters are passed 0 = A/K/R control characters are changed to Idles. Reserved characters passed through (Default 1'b0) 1 = A/K/R control characters are passed through as is RW	RW
1	PCS_DESCR_DISABLE	De-scrambler control in 10GKR RX PCS 1 = Disable descrambler 0 = Enable descrambler (Default 1'b0)	RW
0	PCS_SCR_DISABLE	Scrambler control in 10GKR TX PCS 1 = Disable scrambler 0 = Enable scrambler (Default 1'b0)	RW

Table 5-147. PCS_VS_STATUS

Device Address: 0x03 Register Address: 0x8010 Default: 0x00FD			
Bit	**Name**	**Description**	**Access**
13	UNCORR_ERR_STATUS	1 = Uncorrectable block error found	RO/LH
12	CORR_ERR_STATUS	1 = Correctable block error found	RO/LH
8	PCS_TP_ERR	PCS test pattern verification status PCS_SCR_DISABLE 1 = Error occurred during pseudo random test pattern verification Number of errors can be checked by reading PCS_TP_ERR_COUNT (3.43) register	RO/LH
7:0	RESERVED	For TI use only.	COR

5.6.1.4 Auto-Negotiation Registers

The registers below can be accessed only in Clause 45 mode and with device address field set to 0x07 (DA[4:0] = 5'b00111)

Table 5-148. AN_CONTROL

Device Address: 0x07 Register Address: 0x0000 Default: 0x3000			
Bit	**Name**	**Description**	**Access**
15	AN_RESET	1 = Resets Auto Negotiation 0 = Normal operation (Default 1'b0)	RW/SC
13	RESERVED	For TI use only (Default 1'b1)	RW
12	AN_ENABLE	1 = Enable Auto Negotiation (Default 1'b1) 0 = Disable Auto Negotiation	RW
9	AN_RESTART	1 = Restart Auto Negotiation 0 = Normal operation (Default 1'b0) If set, a read of this register is required to clear AN_RESTART bit.	RW/SC(1)

(1) If set, a read of register 7.0 is required to clear AN_RESTART bit.

Table 5-149. AN_STATUS

Device Address: 0x07 Register Address: 0x0001 Default: 0x0088			
Bit	**Name**	**Description**	**Access**
9	AN_PAR_DET_FAULT	1 = Fault has been detected via parallel detection function 0 = Fault has not been detected via parallel detection function	RO/LH
7	AN_EXP_NP_STATUS	1 = Extended next page is used 0 = Extended next page is not allowed	RO
6	AN_PAGE_RCVD	1 = A page has been received 0 = A page has not been received	RO/LH
5	AN_COMPLETE	1 = Auto Negotiation process is completed 0 = Auto Negotiation process not completed	RO
4	REMOTE_FAULT	Always reads 0. Fault condition status can be read at 7.1.9 and 7.1.2.	RO
3	AN_ABILITY	Always reads 1. 1 = Device is able to perform Auto Negotiation 0 = Device not able to perform Auto Negotiation	RO
2	LINK_STATUS	1 = Link is up 0 = Link is down	RO/LL
0	AN_LP_ABILITY	1 = LP is able to perform Auto Negotiation 0 = LP not able to perform Auto Negotiation	RO

Table 5-150. AN_DEV_PACKAGE

Device Address: 0x07 Register Address: 0x0005 Default: 0x0080			
Bit	**Name**	**Description**	**Access**
7	AN_PRESENT	Always reads 1 1 = Auto Negotiation present in the package 0 = Auto Negotiation not present in the package	RO

Table 5-151. AN_ADVERTISEMENT_1

Device Address: 0x07 Register Address: 0x0010 Default: 0x1001			
Bit	**Name**	**Description**	**Access**
15	AN_NEXT_PAGE	NP bit (D15) in base link codeword 1 = Next page available 0 = Next page not available (Default 1'b0)	RW
14	AN_ACKNOWLEDGE	Acknowledge bit (D14) in base link codeword. Always reads 0.	RO
13	AN_REMOTE_FAULT	RF bit (D13) in base link codeword 1 = Sets RF bit to 1 0 = Normal operation (Default 1'b0)	RW
12:10	AN_CAPABILITY[2:0]	Value to be set in D12:D10 bits of the base link codeword. Consists of abilities like PAUSE, ASM_DIR (Default 3'b100)	RW
9:5	AN_ECHO_NONCE[4:0]	Value to be set in D9:D5 bits of the base link codeword. Consists of Echo nonce value. Transmitted in base page only until local device and link Partner have exchanged unique Nonce values, at which time transmitted Echoed Nonce will change to Link Partner's Nonce value. Read value always reflects the value written, not the actual Echoed Nonce. (Default 5'b00000)	RW
4:0	AN_SELECTOR[4:0]	Value to be set in D4:D0 bits of the base link codeword. Consists of selector field value (Default 5'b00001)	RW

Table 5-152. AN_ADVERTISEMENT_2

Device Address: 0x07 Register Address: 0x0011 Default: 0x0080			
Bit	**Name**	**Description**	**Access**
15:8	AN_ABILITY[10:3]	Value to be set in D31:D24 bits of the base link codeword. Consists of technology ability field bits [10:3] (Default 9'b000000000)	RW
7	AN_ABILITY[2]	Value to be set in D23 bits of the base link codeword. Consists of technology ability field bits [2]. When set, indicates device supports 10GBASE-KR (Default 1'b1)	RW

Table 5-152. AN_ADVERTISEMENT_2 (continued)

Device Address: 0x07 Register Address: 0x0011 Default: 0x0080			
Bit	**Name**	**Description**	**Access**
6	AN_ABILITY[1]	Value to be set in D22 bits of the base link codeword. Consists of technology ability field bits [1]. Always set to 0 (Default 1'b0)	RW
5	AN_ABILITY[0]	Value to be set in D21 bits of the base link codeword. Consists of technology ability field bit [0]. When set, indicates device supports 1000BASE-KX (Default 1'b0)	RW
4:0	AN_TRANS_NONCE_ FIELD[4:0]	Not used. Transmitted Nonce field is generated by hardware random number generator. Read value always reflects value written, not the actual Transmitted Nonce (Default 5'b00000)	RW

Table 5-153. AN_ADVERTISEMENT_3

Device Address: 0x07 Register Address: 0x0012 Default: 0x4000			
Bit	**Name**	**Description**	**Access**
15	AN_FEC_REQUESTED	Value to be set in D47 bits of the base link codeword. When set, indicates a request to enable FEC on the link (Default 1'b0)	RW
14	AN_FEC_ABILITY	Value to be set in D46 bits of the base link codeword. When set, indicates 10GBASE-KR has FEC ability (Default 1'b1)	
13:0	AN_ABILITY[24:11]	Value to be set in D45:D32 bits of the base link codeword. Consists of technology ability field bits [24:11] (Default 14'b00000000000000)	

Table 5-154. AN_LP_ADVERTISEMENT_1(1)

Device Address: 0x07 Register Address: 0x0013 Default: 0x0001			
Bit	**Name**	**Description**	**Access**
15	AN_LP_NEXT_PAGE	NP bit (D15) in link partner base page 1 = Next page available in link partner 0 = Next page not available in link partner	RO
14	AN_LP_ACKNOWLEDGE	Acknowledge bit (D14) in link partner base page.	RO
13	AN_LP_REMOTE_FAULT	RF bit (D13) in link partner base page 1 = Remote fault detected in link partner 0 = Remote fault not detected in link partner	RO
12:10	AN_ LP_CAPABILITY	D12:D10 bits of the link partner base page. Consists of abilities like PAUSE, ASM_DIR	RO
9:5	AN_ LP_ECHO_NONCE	D9:D5 bits of the link partner base page. Consists of Echo nonce value	RO
4:0	AN_LP_SELECTOR[4:0]	D4:D0 bits of the link partner base page. Consists of selector field value Always reads 5'b00001	RO

(1) To get accurate AN_LP_ADVERTISEMENT read value, Register 7.19 should be read first before reading 7.20 and 7.21

Table 5-155. AN_LP_ADVERTISEMENT_2

Device Address: 0x07 Register Address: 0x0014 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:8	AN_ LP_ABILITY[10:3]	D31:D24 bits of the link partner base page. Consists of technology ability field bits [10:3]	RO
7	AN_LP_ABILITY[2]	D23 bits of the link partner base page. Consists of technology ability field bits [2]. When high, indicates link partner supports 10GBASE-KR	
6	AN_LP_ABILITY[1]	D22 bits of the link partner base page. Consists of technology ability field bits [1].	
5	AN_LP_ABILITY[0]	D21 bits of the link partner base page. Consists of technology ability field bit [0]. When high, indicates link partner supports 1000BASE-KX	
4:0	AN_LP_TRANS_NONCE_ FIELD	D20:D16 bits of the link partner base page. Consists of transmitted nonce value	

Table 5-156. AN_LP_ADVERTISEMENT_3

Device Address: 0x07 Register Address: 0x0015 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15	AN_LP_FEC_REQUESTED	D47 bits of the link partner base page. When high, indicates link partner request to enable FEC on the link	RO
14	AN_LP_FEC_ABILITY	D46 bits of the link partner base page. When high, indicates link partner has FEC ability	
13:0	AN_LP_ABILITY[24:11]	D45:D32 bits of the link partner base page. Consists of link partner technology ability field bits [24:11]	

Table 5-157. AN_XNP_TRANSMIT_1

Device Address: 0x07 Register Address: 0x0016 Default: 0x2000			
Bit	**Name**	**Description**	**Access**
15	AN_XNP_NEXT_PAGE	NP bit (D15) in next page code word 1 = Next page available 0 = Next page not available (Default 1'b0)	RW
14	RESERVED	Always reads 0.	RO
13	AN_MP	Message page bit (D13) in next page code word 1 = Sets MP bit to 1 indicating next page is a message page (Default 1'b1) 0 = Sets MP bit to 0 indicating next page is unformatted next page	RW
12	AN_ACKNOWLEDGE_2	Value to be set in D12 bit of the next page code word. When set, indicates device is able to act on the information defined in the message (Default 1'b0)	RW
11	AN_TOGGLE	Not used. Toggle value is generated by hardware. Read value always reflects value written, not the actual Toggle field (Default 1'b0)	RW
10:0	AN_CODE_FIELD	Value to be set in D10:D0 bits of the next page code word. Consists of Message/Unformatted code field value (Default 11'b00000000000)	RW

Table 5-158. AN_XNP_TRANSMIT_2

Device Address: 0x07 Register Address: 0x0017 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	AN_MSG_CODE_1	Value to be set in D31:D16 bits of the next page code word. Consists of Message/Unformatted code field value (Default 16'b0000000000000000)	RW

Table 5-159. AN_XNP_TRANSMIT_3

Device Address: 0x07 Register Address: 0x0018 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	AN_MSG_CODE_2	Value to be set in D47:D32 bits of the next page code word. Consists of Message/Unformatted code field value (Default 16'b0000000000000000)	RW

Table 5-160. AN_LP_XNP_ABILITY_1(1)

Device Address: 0x07 Register Address: 0x0019 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15	AN_LP_XNP_NEXT_PAGE	NP bit (D15) in next page code word 1 = Next page available 0 = Next page not available (Default 1'b0)	RO
14	AN_LP_XNP_ACKNOWLEDGE	Value in D14 bit of the next page code word. When set, indicates device is able to act on the information defined in the message (Default 1'b0)	RO
13	AN_LP_MP	Message page bit (D13) in next page code word 1 = Sets MP bit to 1 indicating next page is a message page 0 = Sets MP bit to 0 indicating next page is unformatted next page (Default 1'b0)	RO
12	AN_LP_ACKNOWLEDGE_2	Value in D12 bit of the next page code word. When set, indicates device is able to act on the information defined in the message (Default 1'b0)	RO

(1) To get accurate AN_LP_XNP_ABILITYT read value, Register 7.25 should be read first before reading 7.26 and 7.27

Table 5-160. AN_LP_XNP_ABILITY_1[(1)] (continued)

Device Address: 0x07 Register Address: 0x0019 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
11	AN_LP_TOGGLE	Value of D11 bit of the next page code word. Consists of Toggle field value(Default 1'b0)	RO
10:0	AN_ LP_CODE_FIELD	Value in D10:D0 bits of the next page code word. Consists of Message/Unformatted code field value (Default 11'b00000000000)	RO

Table 5-161. AN_LP_XNP_ABILITY_2

Device Address: 0x07 Register Address: 0x001A Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	AN_LP_MSG_CODE_1	Value to be set in D31:D16 bits of the next page code word. Consists of Message/Unformatted code field value (Default 16'b0000000000000000)	RO

Table 5-162. AN_LP_XNP_ABILITY_3

Device Address: 0x07 Register Address: 0x001B Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	AN_LP_MSG_CODE_2	Value to be set in D47:D32 bits of the next page code word. Consists of Message/Unformatted code field value (Default 16'b0000000000000000)	RO

Table 5-163. AN_BP_STATUS

Device Address: 0x07 Register Address: 0x0030 Default: 0x0001			
Bit	**Name**	**Description**	**Access**
4	AN_10G_KR_FEC	1 = PMA/PMD is negotiated to perform 10GBASE-KR FEC	RO
3	AN_10G_KR	1 = PMA/PMD is negotiated to perform 10GBASE-KR	
1	AN_1G_KX	1 = PMA/PMD is negotiated to perform 1000BASE-KX	
0	AN_BP_AN_ABILITY	Always reads 1. 1 = Indicates 1000BASE-KX, 10GBASE-KR is implemented	

Table 5-164. AN_VS_CONTROL

Device Address: 0x03 Register Address: 0x0023 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
7.32768.0	RESERVED	For TI use only. (Default 1'b0)	RW

5.6.2 1G-KX Programmers Reference

5.6.2.1 Vendor Specific Device Registers

The registers below can be accessed directly through Clause 22 and Clause 45. In Clause 45 mode, these registers can be accessed by setting device address field to 0x1E (DA[4:0] = 5'b11110). In Clause 22 mode, these registers can be accessed by setting 5 bit register address field to same value as 5 LSB bits of Register Address field specified for each register. For example, 16 bit register address 0x001C in clause 45 mode can be accessed by setting register address field to 5'h1C in clause 22 mode.

Table 5-165. GLOBAL_CONTROL_1 (1)

Device Address: 0x1E Register Address: 0x0000 Default: 0x0020			
Bit	**Name**	**Description**	**Access**
15	GLOBAL_RESET	Global reset. 0 = Normal operation (Default 1'b0) 1 = Resets TX and RX data path including MDIO registers. Equivalent to asserting RESET_N.	RW SC (2)
11	GLOBAL_WRITE	Global write enable. 0 = Control settings are specific to channel addressed (Default 1'b0) 1 = Control settings in channel specific registers are applied to all 4 channels regardless of channel addressed	RW
5:0	PRBS_PASS_OVERLAY[5:0]	PRBS_PASS pin status selection. Applicable only when PRBS test pattern verification is enabled on HS side or LS side. PRBS_PASS pin reflects PRBS verification status on selected Channel HS/LS side 1xx000 = PRBS_PASS reflects combined status of Channel A/B/C/D HS serdes PRBS verification. If PRBS verification fails on any channel HS serdes, PRBS_PASS will be asserted low. (Default 6'b100000) 000000 = Status from Channel A HS Serdes side 000100 = Status from Channel A LS Serdes side Lane 0 001000 = Status from Channel B HS Serdes side 001100 = Status from Channel B LS Serdes side Lane 0 010000 = Status from Channel C HS Serdes side 010100 = Status from Channel C LS Serdes side Lane 0 011000 = Status from Channel D HS Serdes side 011100 = Status from Channel D LS Serdes side Lane 0 Rest = NA	RW

(1) This global register is channel independent.
(2) After reset bit is set to one, it automatically sets itself back to zero on the next MDC clock cycle.

Table 5-166. CHANNEL_CONTROL_1

Device Address: 0x1E Register Address: 0x0001 Default: 0x0B88			
Bit	**Name**	**Description**	**Access**
15	POWERDOWN	Setting this bit high powers down entire data path with exception that MDIO interface stays active. 0 = Normal operation (Default 1'b0) 1 = Power Down mode is enabled.	RW
14	HSRX_CLKOUT_POWERDOWN	0 = Normal operation (Default 1'b0) 1 = Enable HSRXx_CLKOUTP/N Power Down	RW
11	SW_PCS_SEL	Applicable in Clause 45 mode only. Valid only when MODE_SEL pin is 0, AN_ENABLE (7.0.12) is 0 and SW_DEV_MODE_SEL (30.1.10) is 0. 1 = NA (Default 1'b1) 0 = Set device to 1G-KX mode	RW
10	SW_DEV_MODE_SEL	Valid only when MODE_SEL pin is 0 1 = NA 0 = In clause 45 mode, device mode is set using Auto negotiation. In clause 22 mode, device set to 1G-KX mode(Default 1'b0)	RW
7:4	HSRX_CLKOUT_DIV[3:0]	Output clock divide setting. This value is used to divide selected clock (Selected using HSRX_CLKOUT_SEL) before giving it out onto respective channel HSRXx_CLKOUTP/N. 0000 = Divide by 1 0001 = RESERVED 0010 = RESERVED 0011 = RESERVED 0100 = Divide by 2 0101 = RESERVED 0110 = RESERVED 0111 = RESERVED 1000 = Divide by 4 (Default 4'b1000) 1001 = Divide by 8 1010 = Divide by 16 1011 = RESERVED 1100 = Divide by 5 1101 = Divide by 10 1110 = Divide by 20 1111 = Divide by 25	RW

Table 5-166. CHANNEL_CONTROL_1 (continued)

Device Address: 0x1E Register Address: 0x0001 Default: 0x0B88			
Bit	**Name**	**Description**	**Access**
3	HSRX_CLKOUT_ EN	Output clock enable. 0 = Holds HSRXx_CLKOUTP/N output to a fixed value. 1 = Allows HSRXx_CLKOUTP/N output to toggle normally (Default 1'b1)	RW
2	HSRX_CLKOUT_SEL	Output clock select. Selected Recovered clock sent out on HSRXx_CLKOUTP/N pins 0 = Selects respective Channel HSRX recovered byte clock as output clock (Default 1'b0) 1 = Selects respective Channel HSRX VCO divide by 2 clock as output clock	RW
1	REFCLK_SW_SEL	Channel HS Reference clock selection. Applicable only when REFCLK_SEL pin is LOW. 0 = Selects REFCLK_0_P/N as clock reference to Channel x HS side serdes macro(Default 1'b0) 1 = Selects REFCLK_1_P/N as clock reference to Channel x HS side serdes macro	RW
0	LS_REFCLK_SEL	Channel LS Reference clock selection. 0 = LS side serdes macro reference clock is same as HS side serdes reference clock (E.g. If REFCLK_0_P/N is selected as HS side serdes macro reference clock, REFCLK_0_P/N is selected as LS side serdes macro reference clock and vice versa) (Default 1'b0) 1 = Alternate reference clock is selected as clock reference to Channel x LS side serdes macro (E.g. If REFCLK_0_P/N is selected as HS side serdes macro reference clock, REFCLK_1_P/N is selected as LS side serdes macro reference clock and vice versa)	RW

Table 5-167. HS_SERDES_CONTROL_1

Device Address: 0x1E Register Address: 0x0002 Default: 0x811D			
Bit	**Name**	**Description**	**Access**
15:10	RESERVED	For TI use only (Default 9'b100000)	RW
9:8	HS_LOOP BANDWIDTH[1:0]	HS Serdes PLL Loop Bandwidth settings 00 = Reserved 01 = Narrow bandwidth (Default 2'b01) 10 = Medium bandwidth 11 = Highest bandwidth.	RW
7	RESERVED	For TI use only (Default 1'b0)	
6	RESERVED	For TI use only (Default 1'b0)	
5	RESERVED	For TI use only (Default 1'b0)	
4	HS_ENPLL	HS Serdes PLL enable control. HS Serdes PLL is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 30.1.15 is set HIGH. 0 = Disables PLL in HS serdes 1 = Enables PLL in HS serdes (Default 1'b1)	
3:0	HS_PLL_MULT[3:0]	HS Serdes PLL multiplier setting (Default 4'b1101). Refer to Table 5-23. This setting is automatically controlled and value set through these register bits is ignored unless REFCLK_FREQ_SEL_1 or related OVERRIDE bit is set. See 1GKX supported rates for more information on valid PLL multiplier settings	

Table 5-168. HS PLL Multiplier Control

30.2.3:0		30.2.3:0	
Value	**PLL Multiplier factor**	**Value**	**PLL Multiplier factor**
0000	Reserved	1000	12x
0001	Reserved	1001	12.5x
0010	4x	1010	15x
0011	5x	1011	16x
0100	6x	1100	16.5x
0101	8x	1101	20x
0110	8.25x	1110	25x

Table 5-168. HS PLL Multiplier Control (continued)

30.2.3:0		30.2.3:0	
Value	**PLL Multiplier factor**	**Value**	**PLL Multiplier factor**
0111	10x	1111	Reserved

Table 5-169. HS_ SERDES_CONTROL_2

Device Address: 0x1E Register Address: 0x0003 Default: 0x8848			
Bit	**Name**	**Description**	**Access**
15:12	HS_SWING[3:0]	Transmitter Output swing control for HS Serdes. (Default 4'b1000) Refer to Table 5-25.	RW
11	HS_ENTX	HS Serdes transmitter enable control. HS Serdes transmitter is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 30.1.15 is set HIGH. 0 = Disables HS serdes transmitter 1 = Enables HS serdes transmitter (Default 1'b1)	RW
10	HS_EQHLD	HSRX Equalizer hold control 0 = Normal operation (Default 1'b0) 1 = Holds equalizer and long tail correction in its current state	RW
9:8	HS_RATE_TX [1:0]	HS Serdes TX rate settings. This setting is automatically controlled and value set through these register bits is ignored unless REFCLK_FREQ_SEL_1 or related OVERRIDE bit is set. 00 = Full rate (Default 2'b00) 01 = Half rate 10 = Quarter rate 11 = Eighth rate	RW
7:4	RESERVED	For TI use only (Default 4'b0100)	RW
3	HS_ENRX	HS Serdes receiver enable control. HS Serdes receiver is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 30.1.15 is set HIGH. 0 = Disables HS serdes receiver 1 = Enables HS serdes receiver (Default 1'b1)	RW
2:0	HS_RATE_RX [2:0]	HS Serdes RX rate settings. This setting is automatically controlled and value set through these register bits is ignored unless REFCLK_FREQ_SEL_1 or related OVERRIDE bit is set. 000 = Full rate (Default 3'b000) 101 = Half rate 110 = Quarter rate 111 = Eighth rate 001 = Reserved 01x = Reserved 100 = Reserved	RW

Table 5-170. HSTX AC Mode Output Swing Control

Value 30.3[15:12]	**AC Mode**
	Typical Amplitude (mVdfpp)
0000	130
0001	220
0010	300
0011	390
0100	480
0101	570
0110	660
0111	750
1000	830
1001	930
1010	1020
1011	1110

Table 5-170. HSTX AC Mode Output Swing Control (continued)

Value 30.3[15:12]	AC Mode
	Typical Amplitude (mVdfpp)
1100	1180
1101	1270
1110	1340
1111	1400

Table 5-171. HS_SERDES_CONTROL_3

Device Address: 0x1E Register Address: 0x0004 Default: 0x1400			
Bit	**Name**	**Description**	**Access**
15	HS_ENTRACK	HSRX ADC Track mode 0 = Normal operation (Default 1'b0) 1 = Forces ADC into track mode	RW
14:12	HS_EQPRE[2:0]	Serdes Rx precursor equalizer selection 000 = 1/9 cursor amplitude 001 = 3/9 cursor amplitude (Default 3'b001) 010 = 5/9 cursor amplitude 011 = 7/9 cursor amplitude 100 = 9/9 cursor amplitude 101 = 11/9 cursor amplitude 110 = 13/9 cursor amplitude 111 = Disable	RW
11:10	HS_CDRFMULT[1:0]	Clock data recovery algorithm frequency multiplication selection 00 = First order. Frequency offset thracking disabled 01 = Second order. 1x mode 10 = Second order. 2x mode (Default 2'b10) 11 = Reserved	RW
9:8	HS_CDRTHR[1:0]	Clock data recovery algorithm frequency threshold selection 00 = Four vote threshold (Default 2'b00) 01 = Eight vote threshold 10 = Sixteen vote threshold 11 = Thirty two vote threshold	RW
7	RESERVED	For TI use only (Default 1'b0)	RW
6	HS_PEAK_DISABLE	HS Serdes PEAK_DISABLE control 0 = Normal operation (Default 1'b0) 1 = Disables high frequency peaking. Suitable for <6 Gbps operation	RW
5	HS_H1CDRMODE	0 = Normal operation (Default 1'b0) 1 = Enables CDR mode suitable for short channel operation.	RW
4:0	HS_TWCRF[4:0]	Cursor Reduction Factor (Default 5'b00000) Refer to Table 5-27.	RW

Table 5-172. HSTX Cursor Reduction Factor Weights

30.4.4:0		30.4.4:0	
Value	**Cursor reduction (%)**	**Value**	**Cursor reduction (%)**
00000	0	10000	17
00001	2.5	10001	20
00010	5.0	10010	22
00011	7.5	10011	25
00100	10.0	10100	27
00101	12	10101	30
00110	15	10110	32

Table 5-172. HSTX Cursor Reduction Factor Weights (continued)

30.4.4:0		30.4.4:0	
Value	Cursor reduction (%)	Value	Cursor reduction (%)
00111	Reserved	10111	35
01000		11000	37
01001		11001	40
01010		11010	42
01011		11011	45
01100		11100	47
01101		11101	50
01110		11110	52
01111		11111	55

Table 5-173. HS_SERDES_CONTROL_4

Device Address: 0x1E Register Address:0x0005 Default:0x2000			
Bit	Name	Description	Access
15	HS_RX_INVPAIR	Receiver polarity. 0 = Normal polarity. HSRXxP considered positive data. HSRXxN considered negative data (Default 1'b0) 1 = Inverted polarity. HSRXxP considered negative data. HSRXxN considered positive data	RW
14	HS_TX_INVPAIR	Transmitter polarity. 0 = Normal polarity. HSTXxP considered positive data and HSTXxN considered negative data (Default 1'b0) 1 = Inverted polarity. HSTXxP considered negative data and HSTXxN considered positive data	RW
13	RESERVED	For TI use only (Default 1'b1)	RW
12:8	HS_TWPOST1[4:0]	Adjacent post cursor1 Tap weight. Selects TAP settings for TX waveform. This setting is automatically controlled through link training and value set through this register bits is ignored unless related OVERRIDE bit is set. (Default 5'b00000) Refer Table 5-29.	RW
7:4	HS_TWPRE[3:0]	Precursor Tap weight. Selects TAP settings for TX waveform. This setting is automatically controlled through link training and value set through this register bits is ignored unless related OVERRIDE bit is set. (Default 4'b0000) Refer Table 5-31.	RW
3:0	HS_TWPOST2[3:0]	Adjacent post cursor2 Tap weight. Selects TAP settings for TX waveform. This setting is automatically controlled through link training and value set through this register bits is ignored unless related OVERRIDE bit is set.(Default 4'b0000) Refer Table 5-30.	RW

Table 5-174. HSTX Post-cursor1 Transmit Tap Weights

30.5.12:8		30.5.12:8	
Value	Tap weight (%)	Value	Tap weight (%)
00000	0	10000	0
00001	+2.5	10001	–2.5
00010	+5.0	10010	–5.0
00011	+7.5	10011	–7.5
00100	+10.0	10100	–10.0
00101	+12.5	10101	–12.5
00110	+15.0	10110	–15.0
00111	+17.5	10111	–17.5
01000	+20.0	11000	–20.0
01001	+22.5	11001	–22.5
01010	+25.0	11010	–25.0

Table 5-174. HSTX Post-cursor1 Transmit Tap Weights (continued)

30.5.12:8		30.5.12:8	
Value	Tap weight (%)	Value	Tap weight (%)
01011	+27.5	11011	–27.5
01100	+30.0	11100	–30.0
01101	+32.5	11101	–32.5
01110	+35.0	11110	–35.0
01111	+37.5	11111	-37.5

Table 5-175. HSTX Post-cursor2 Transmit Tap Weights

30.5.3:0		30.5.3:0	
Value	Tap weight (%)	Value	Tap weight (%)
0000	0	1000	0
0001	+2.5	1001	–2.5
0010	+5.0	1010	–5.0
0011	+7.5	1011	–7.5
0100	+10.0	1100	–10.0
0101	+12.5	1101	–12.5
0110	+15.0	1110	–15.0
0111	+17.5	1111	–17.5

Table 5-176. HSTX Pre-cursor Transmit Tap Weights

30.5.7:4		30.5.7:4	
Value	Tap weight (%)	Value	Tap weight (%)
0000	0	1000	0
0001	+2.5	1001	–2.5
0010	+5.0	1010	–5.0
0011	+7.5	1011	–7.5
0100	+10.0	1100	–10.0
0101	+12.5	1101	–12.5
0110	+15.0	1110	–15.0
0111	+17.5	1111	–17.5

Table 5-177. LS_SERDES_CONTROL_1

Device Address: 0x1E Register Address:0x0006 Default:0xF115			
Bit	**Name**	**Description**	**Access**
15:12	LS_LN_CFG_EN[3:0]	Configuration control for LS Serdes Lane settings (Default 4'b1111) [3] corresponds to LN3, [2] corresponds to LN2 [1] corresponds to LN1, [0] corresponds to LN0 0 = Writes to LS_SERDES_CONTROL_2 and LS_SERDES_CONTROL_3 and LS_CH_CONTROL_1 control registers do not affect respective LS Serdes lane 1 = Writes to LS_SERDES_CONTROL_2 and LS_SERDES_CONTROL_3 and LS_CH_CONTROL_1 control registers affect respective LS Serdes lane For example, if subsequent writes to LS_SERDES_CONTROL_2 and LS_SERDES_CONTROL_3 and LS_CH_CONTROL_1 registers need to affect the settings in Lanes 0 and 1, LS_LN_CFG_EN[3:0] should be set to 4'b0011 Read values in LS_SERDES_CONTROL_2 and LS_SERDES_CONTROL_3 and LS_CH_CONTROL_1 reflect the settings value for Lane selected through LS_LN_CFG_EN[3:0]. To read Lane 0 settings, LS_LN_CFG_EN[3:0] should be set to 4'b0001 To read Lane 1 settings, LS_LN_CFG_EN[3:0] should be set to 4'b0010 To read Lane 2 settings, LS_LN_CFG_EN[3:0] should be set to 4'b0100 To read Lane 3 settings, LS_LN_CFG_EN[3:0] should be set to 4'b1000 Read values of LS_SERDES_CONTROL_2 and LS_SERDES_CONTROL_3 and LS_CH_CONTROL_1 registers are not valid for any other LS_LN_CFG_EN[3:0] combination	RW
11:10	RESERVED	For TI use only (Default 2'b00)	
9:8	LS_LOOP_BANDWIDTH[1:0]	LS Serdes PLL Loop Bandwidth settings 00 = Reserved 01 = Applicable when external JC_PLL is NOT used (Default 2'b01) 10 = Applicable when external JC_PLL is used 11 = Reserved	
7:5	RESERVED	For TI use only (Default 3'b000)	
4	LS_ENPLL	LS Serdes PLL enable control. LS Serdes PLL is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 30.1.15 is set HIGH. 0 = Disables PLL in LS serdes 1 = Enables PLL in LS serdes (Default 1'b1)	
3:0	LS_MPY[3:0]	LS Serdes PLL multiplier setting (Default 4'b0101). This setting is automatically controlled and value set through these register bits is ignored unless REFCLK_FREQ_SEL_1 or related OVERRIDE bit is set. Refer to Table 5-178. Refer 10GKR supported rates for valid PLL Multiplier values.	

Table 5-178. LS PLL Multiplier Control

30.6.3:0		30.6.3:0	
Value	**PLL Multiplier factor**	**Value**	**PLL Multiplier factor**
0000	4x	1000	15x
0001	5x	1001	20x
0010	6x	1010	25x
0011	Reserved	1011	Reserved
0100	8x	1100	Reserved
0101	10x	1101	50x
0110	12x	1110	65x
0111	12.5x	1111	Reserved

Table 5-179. LS_ SERDES_CONTROL_2

Device Address: 0x1E Register Address:0x0007 Default:0xDC04			
Bit	**Name**	**Description**	**Access**
15	RESERVED	For TI use only. (Default 1'b1)	RW
14:12	LS_SWING[2:0]	Output swing control on LS Serdes side. (Default 3'b101) Refer to Table 5-180.	RW
11	LS_LOS	LS Serdes LOS detector control 0 = Disable Loss of signal detection on LS serdes lane inputs 1 = Enable Loss of signal detection on LS serdes lane inputs (Default 1'b1)	RW
10	LS_TX_ENRX	LS Serdes enable control on the transmit channel. LS Serdes per lane on transmitter channel is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 30.1.15 is set HIGH. 0 = Disables LS serdes lane 1 = Enables LS serdes lane (Default 1'b1)	RW
9:8	LS_TX_RATE [1:0]	LS Serdes lane rate settings on transmit channel. This setting is automatically controlled and value set through this register bits is ignored unless REFCLK_FREQ_SEL_1 or related OVERRIDE bit is set. 00 = Full rate (Default 2'b00) 01 = Half rate 10 = Quarter rate 11 = Reserved	RW
7:4	LS_DE[3:0]	LS Serdes De-emphasis settings. (Default 4'b0000) Refer to Table 5-181.	RW
3	RESERVED	For TI use only.	RW
2	LS_RX_ENTX	LS Serdes lane enable control on receive channel. LS Serdes per lane on receiver channel is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 30.1.15 is set HIGH. 0 = Disables LS serdes lane 1 = Enables LS serdes lane (Default 1'b1)	RW
1:0	LS_RX_RATE [1:0]	LS Serdes lane rate settings on receive channel. This setting is automatically controlled and value set through this register bits is ignored unless REFCLK_FREQ_SEL_1 or related OVERRIDE bit is set. 00 = Full rate (Default 2'b00) 01 = Half rate 10 = Quarter rate 11 = Reserved	RW

Table 5-180. LSRX Output AC Mode Output Swing Control

VALUE 30.7.14:12	AC MODE
	Typical Amplitude (mVdfpp)
000	190
001	380
010	560
011	710
100	850
101	950
110	1010
111	1050

Table 5-181. LSRX Output De-emphasis

30.7.7:4			30.7.7:4		
Value	Amplitude reduction		Value	Amplitude reduction	
	(%)	dB		(%)	dB
0000	0	0	1000	38.08	–4.16
0001	4.76	–0.42	1001	42.85	–4.86
0010	9.52	–0.87	1010	47.61	–5.61
0011	14.28	–1.34	1011	52.38	–6.44
0100	19.04	–1.83	1100	57.14	–7.35
0101	23.8	–2.36	1101	61.9	–8.38
0110	28.56	–2.92	1110	66.66	–9.54
0111	33.32	–3.52	1111	71.42	–10.87

Table 5-182. LS_SERDES_CONTROL_3

Device Address: 0x1E Register Address:0x0008 Default:0x000D			
Bit	**Name**	**Description**	**Access**
15	LS_RX_INVPAIR	LS Serdes lane outputs polarity on the receive channel. (x = Channel A or B or C or D, y = Lane 0 or 1 or 2 or 3) 0 = Normal polarity. OUTxyP considered positive data. OUTxyN considered negative data (Default 1'b0) 1 = Inverted polarity. OUTxyP considered negative data. OUTxyN considered positive data	RW
14	LS_TX_INVPAIR	LS Serdes lane inputs polarity on the transmit channel. (x = Channel A or B or C or D, y = Lane 0 or 1 or 2 or 3) 0 = Normal polarity. INxyP considered positive data and INxyN considered negative data (Default 1'b0) 1 = Inverted polarity. INxyP considered negative data and INxyP considered positive data	RW
13:12	RESERVED	For TI use only (Default 2'b00)	RW
11:8	LS_EQ[3:0]	LS Serdes Equalization control (Default 4'b0000). Table 5-38.	RW
7:0	RESERVED	For TI use only (Default 8'b00001101)	RW

Table 5-183. LSEQ Serdes Equalization

30.8.11:8			30.8.11:8		
Value	Low Freq Gain	Zero Freq	Value	Low Freq Gain	Zero Freq
0000	Maximum		1000	Adaptive	365 MHz
0001	Adaptive		1001		275 MHz
0010	Reserved		1010		195 MHz
0011			1011		140 MHz
0100			1100		105 MHz
0101			1101		75 MHz
0110			1110		55 MHz
0111			1111		50 MHz

Table 5-184. HS_OVERLAY_CONTROL

Device Address: 0x1E Register Address:0x0009 Default:0x0380			
Bit	**Name**	**Description**	**Access**
11:8	RESERVED	For TI use only. (Default 4'b0011)	RW
5	HS_CH_SYNC_OVERLAY	0 = LOSx pin does not reflect receive channel loss of block lock (Default 1'b0) 1 = Allows channel loss of block lock to be reflected on LOSx pin	RW
4	HS_INVALID_CODE_OVERLAY	0 = LOSx pin does not reflect receive channel invalid code word error (Default 1'b0) 1 = Allows invalid code word error to be reflected on LOSx pin	RW
3	HS_AGCLOCK_OVERLAY	0 = LOSx pin does not reflect HS Serdes AGC unlock status (Default 1'b0) 1 = Allows HS Serdes AGC unlock status to be reflected on LOSx pin	RW
2	HS_AZDONE_OVERLAY	0 = LOSx pin does not reflect HS Serdes auto zero calibration not done status (Default 1'b0) 1 = Allows auto zero calibration not done status to be reflected on LOSx pin	RW
1	HS_PLL_LOCK_OVERLAY	0 = LOSx pin does not reflect loss of HS Serdes PLL lock status (Default 1'b0) 1 = Allows HS Serdes loss of PLL lock status to be reflected on LOSx pin	RW
0	HS_LOS_OVERLAY	0 = LOSx pin does not reflect HS Serdes Loss of signal condition (Default 1'b0) 1 = Allows HS Serdes Loss of signal condition to be reflected on LOSx pin	RW

Table 5-185. LS_OVERLAY_CONTROL

Device Address: 0x1E Register Address:0x000A Default:0x4000			
Bit	**Name**	**Description**	**Access**
12	LS_PLL_LOCK_OVERLAY	0 = LOSx pin does not reflect loss of LS SERDES PLL lock status (Default 1'b0) 1 = Allows LS SERDES loss of PLL lock status to be reflected on LOSx pin	RW
8	LS_CH_SYNC_OVERLAY_LN[0]	0 = LOSx pin does not reflect LS Serdes lane loss of synchronization condition (Default 1'b0) 1 = Allows LS serdes lane loss of synchronization condition to be reflected on LOSx pin	RW
4	LS_INVALID_CODE_OVERLAY_LN[0]	0 = LOSx pin does not reflect LS Serdes lane invalid code condition (Default 1'b0) 1 = Allows LS serdes lane invalid code condition to be reflected on LOSx pin	RW
0	LS_LOS_OVERLAY_LN[0]	0 = LOSx pin does not reflect LS Serdes lane Loss of signal condition (Default 1'b0) 1 = Allows LS serdes lane Loss of signal condition to be reflected on LOSx pin	RW

Table 5-186. LOOPBACK_TP_CONTROL

Device Address: 0x1E Register Address:0x000B Default:0x0F30			
Bit	**Name**	**Description**	**Access**
15:14	RESERVED	For TI use only. (Default 2'b00)	RW
13	HS_TP_GEN_EN	0 = Normal operation (Default 1'b0) 1 = Activates test pattern generation selected by bits 30.11.10:8	RW
12	HS_TP_VERIFY_EN	0 = Normal operation (Default 1'b0) 1 = Activates test pattern verification selected by bits 30.11.10:8	RW
11	LS_TEST_PATT_SEL[2]	See selection in 30.11.5:4	RW

Table 5-186. LOOPBACK_TP_CONTROL (continued)

Device Address: 0x1E Register Address:0x000B Default:0x0F30			
Bit	**Name**	**Description**	**Access**
10:8	HS_TEST_PATT_SEL[2:0]	Test Pattern Selection. Refer Test pattern procedures section for more information. 000 = High Frequency Test Pattern (Generation only) 001 = Low Frequency Test Pattern (Generation only) 010 = Mixed Frequency Test Pattern (Generation only) 011 = CRPAT Long (Requires setting LS_TP_VERIFY_EN to 1'b1 and setting LS_TEST_PATT_SEL[2:0]to 3'b011 or 3'b100) 100 = CRPAT Short (Requires setting LS_TP_VERIFY_EN to 1'b1 and setting LS_TEST_PATT_SEL[2:0]to 3'b011 or 3'b100) 101 = 2^7 - 1 PRBS pattern 110 = 2^{23} - 1 PRBS pattern 111 = 2^{31} - 1 PRBS pattern(Default 3'b111) Errors can be checked by reading HS_ERROR_COUNT register	RW
7	LS_TP_GEN_EN	0 = Normal operation (Default 1'b0) 1 = Activates test pattern generation selected by bits {30.11.11, 30.11.5:4} on the LS side	RW
6	LS_TP_VERIFY_EN	0 = Normal operation (Default 1'b0) 1 = Activates PRBS/CRPAT test pattern verification selected by bits {30.11.11, 30.11.5:4} on the LS side	RW
5:4	LS_TEST_PATT_SEL[1:0]	LS Test Pattern Selection LS_TEST_PATT_SEL[2:0]. Refer Test pattern procedures section for more information. LS_TEST_PATT_SEL[2] is 30.11.11 000 = High Frequency Test Pattern (Generation only) 001 = Low Frequency Test Pattern (Generation only) 010 = Mixed Frequency Test Pattern (Generation only) 011 = CRPAT Long 100 = CRPAT Short 101 = 27 - 1 PRBS pattern 110 = 223 - 1 PRBS pattern 111 = 231 - 1 PRBS pattern(Default 3'b111)	RW
3	DEEP_REMOTE_LPBK	0 = Normal functional mode (Default 1'b0) 1 = Enable deep remote loopback mode	RW
2	SHALLOW_REMOTE_LPBK	0 = Normal functional mode (Default 1'b0) 1 = Enable shallow remote loopback mode and serial retime mode	RW
1	DEEP_LOCAL_LPBK	0 = Normal functional mode (Default 1'b0) 1 = Enable deep local loopback mode	RW
0	SHALLOW_LOCAL_LPBK	0 = Normal functional mode (Default 1'b0) 1 = Enable shallow local loopback mode	RW

Table 5-187. LS_CONFIG_CONTROL

Device Address: 0x1E Register Address: 0x000C Default: 0x03F0			
Bit	**Name**	**Description**	**Access**
13:12	LS_STATUS_CFG[1:0]	Selects selected lane status to be reflected in LS_STATUS_1 register 0x15 00 = Lane 0 (Default 2'b00) 01 = NA 1x = NA	RW

Table 5-188. RESET_CONTROL

Device Address: 0x1E Register Address: 0x000E Default: 0x0000			
Bit	**Name**	**Description**	**Access**
3	DATAPATH_RESET	Channel datapath reset control. Required once the desired functional mode is configured. 0 = Normal operation. (Default 1'b0) 1 = Resets channel logic excluding MDIO registers. (Resets both Tx and Rx datapath)	RW SW(1)

(1) After reset bit is set to one, it automatically sets itself back to zero on the next MDC clock cycle.

Table 5-189. CHANNEL_STATUS_1

Device Address: 0x1E Register Address: 0x000F Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15	HS_TP_STATUS	Test Pattern status for CRPAT test patterns on HS side. 1 = Alignment has achieved and correct pattern has been received. Any bit errors are reflected in HS_ERROR_COUNTER register (0x10) 0 = Alignment has not been determined	RO
14	LS_TP_STATUS	Test Pattern status for CRPAT test patterns on LS side. 1 = Lane alignment is achieved on the LS side 0 = Lane alignment is not achieved on the LS side RO	RO
13	HS_LOS	Loss of Signal Indicator. When high, indicates that a loss of signal condition is detected on HS serial receive inputs RO/LH	RO/LH
12	HS_AZ_DONE	Auto zero complete indicator. When high, indicates auto zero calibration is complete RO/LL	RO/LL
11	HS_AGC_LOCKED	Adaptive gain control loop lock indicator. When high, indicates AGC loop is in locked state	
10	HS_CHANNEL_SYNC	Channel synchronization status indicator. When high, indicates channel synchronization has achieved on HS side	
9	RESERVED	For TI use only	RO/LH
8	HS_DECODE_INVALID	Valid when decoder is enabled and during CRPAT test pattern verification. When high, indicates decoder received an invalid code word. In functional mode, number of DECODE_INVALID errors are reflected in HS_ERROR_COUNTER register (0x10)	
6	TX_FIFO_OVERFLOW	When high, indicates overflow has occurred in the transmit datapath FIFO.	
4	RX_FIFO_OVERFLOW	When high, indicates overflow has occurred in the receive datapath FIFO.	
1	LS_PLL_LOCK	LS Serdes PLL lock indicator When high, indicates LS Serdes PLL achieved lock to the selected incoming REFCLK0/1_P/N	
0	HS_PLL_LOCK	HS Serdes PLL lock indicator When high, indicates HS Serdes PLL achieved lock to the selected incoming REFCLK0/1_P/N	

Table 5-190. HS_ERROR_COUNTER

Device Address: 0x1E Register Address: 0x0010 Default: 0xFFFD			
Bit	**Name**	**Description**	**Access**
15:0	HS_ERR_COUNT[15:0]	In functional mode, this counter reflects number of invalid code words received by HS decoder. In HS test pattern verification mode , this counter reflects error count for the test pattern selected through 30.11.10:8 (CRPAT and PRBS only) When PRBS_EN pin is set, this counter reflects error count for selected PRBS pattern. Counter value cleared to 16'h0000 when read.	COR

Table 5-191. LS_LN0_ERROR_COUNTER

Device Address: 0x1E Register Address: 0x0011 Default: 0xFFFD			
Bit	**Name**	**Description**	**Access**
15:0	LS_LN0_ERR_COUNT[15:0]	Lane 0 Error counter In functional mode, this counter reflects number of invalid code words received by LS decoder In LS test pattern verification mode , this counter reflects error count for the test pattern selected through {30.11.11,30.11.5:4} (CRPAT and PRBS only) Counter value cleared to 16'h0000 when read	COR

Table 5-192. LS_STATUS_1

Device Address: 0x1E Register Address: 0x0015 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
10	LS_LOS	Loss of Signal Indicator. When high, indicates that a loss of signal condition is detected on LS serial receive inputs for selected lane. Lane can be selected through LS_STATUS_CFG[1:0] (Register 30.12)	RO/LH
8	LS_CH_SYNC_STATUS	LS Channel sync status for selected lane. Lane can be selected through LS_STATUS_CFG[1:0] (Register 30.12)	ROLL
3	LS_INVALID_DECODE	LS Invalid decode error for selected lane. Lane can be selected through LS_STATUS_CFG[1:0] (Register 30.12). Error count for each lane can also be monitored through respective LS_LNx_ERR_COUNT registers	ROLH
2:0	RESERVED	For TI use only.	RO

Table 5-193. TI_RESERVED_CONTROL

Device Address: 0x01 Register Address: 0x0016 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
11:8	RESERVED	For TI use only. (Default 4'b0000)	RW
6:0	RESERVED	For TI use only. (Default 7'b0000000)	

Table 5-194. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address: 0x0017 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	RESERVED	For TI use only. (Default 16'h0000)	RW

Table 5-195. TI_RESERVED_STATUS

Device Address: 0x01 Register Address: 0x0023 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	RESERVED	For TI use only.	RO

Table 5-196. LS_CLKOUT_CONTROL(1)

Device Address: 0x1E Register Address: 0x0019 Default: 0x0808			
Bit	**Name**	**Description**	**Access**
15:12	LS1_CLKOUT_DIV[3:0]	LS1_CLKOUT Output clock divide setting. This value is used to divide selected clock (Selected using LS1_CLKOUT_SEL) before giving it out onto LS1_CLKOUTP/N. 0000 = Divide by 1 (Default 4'b0000) 0001 = RESERVED 0010 = RESERVED 0011 = RESERVED 0100 = Divide by 2 0101 = RESERVED 0110 = RESERVED 0111 = RESERVED 1000 = Divide by 4 1001 = Divide by 8 1010 = Divide by 16 1011 = RESERVED 1100 = Divide by 5 1101 = Divide by 10 1110 = Divide by 20 1111 = Divide by 25	RW
11	LS1_CLKOUT_ EN	Output clock enable. 0 = Holds LS1_CLKOUTP/N output to a fixed value. 1 = Allows LS1_CLKOUTP/N output to toggle normally. (Default 1'b1)	RW

(1) This register is channel independent.

Table 5-196. LS_CLKOUT_CONTROL[(1)] (continued)

Device Address: 0x1E Register Address: 0x0019 Default: 0x0808			
Bit	**Name**	**Description**	**Access**
10:8	LS1_CLKOUT_SEL[2:0]	Output clock select. Selected LS TXBCLK/RXBCLK sent out on LS1_CLKOUTP/N pins 000 = Selects Ch A LSRXBCLK0 clock as output clock (Default 3'b000) 001 = Selects Ch B LSRXBCLK0 clock as output clock 010 = Selects Ch C LSRXBCLK0 clock as output clock 011 = Selects Ch D LSRXBCLK0 clock as output clock 100 = Selects Ch A LSTXBCLK clock as output clock 101 = Selects Ch B LSTXBCLK clock as output clock 110 = Selects Ch C LSTXBCLK clock as output clock 111 = Selects Ch D LSTXBCLK clock as output clock	RW
7:4	LS0_CLKOUT_DIV[3:0]	LS0_CLKOUT Output clock divide setting. This value is used to divide selected clock (Selected using LS0_CLKOUT_SEL) before giving it out onto LS0_CLKOUTP/N. 0000 = Divide by 1 (Default 4'b0000) 0001 = RESERVED 0010 = RESERVED 0011 = RESERVED 0100 = Divide by 2 0101 = RESERVED 0110 = RESERVED 0111 = RESERVED 1000 = Divide by 4 1001 = Divide by 8 1010 = Divide by 16 1011 = RESERVED 1100 = Divide by 5 1101 = Divide by 10 1110 = Divide by 20 1111 = Divide by 25	RW
3	LS0_CLKOUT_ EN	Output clock enable. 0 = Holds LS0_CLKOUTP/N output to a fixed value. 1 = Allows LS0_CLKOUTP/N output to toggle normally. (Default 1'b1)	RW
2:0	LS0_CLKOUT_SEL[2:0]	Output clock select. Selected LS TXBCLK/RXBCLK sent out on LS0_CLKOUTP/N pins 000 = Selects Ch A LSRXBCLK0 clock as output clock (Default 3'b000) 001 = Selects Ch B LSRXBCLK0 clock as output clock 010 = Selects Ch C LSRXBCLK0 clock as output clock 011 = Selects Ch D LSRXBCLK0 clock as output clock 100 = Selects Ch A LSTXBCLK clock as output clock 101 = Selects Ch B LSTXBCLK clock as output clock 110 = Selects Ch C LSTXBCLK clock as output clock 111 = Selects Ch D LSTXBCLK clock as output clock	RW

Table 5-197. HS_TX_CLKOUT_CONTROL(1)

Device Address: 01E Register Address: 0x001A Default: 0x0C0C			
Bit	**Name**	**Description**	**Access**
15:12	HSTX1_CLKOUT_DIV[3:0]	HSTX1_CLKOUT Output clock divide setting. This value is used to divide selected clock (Selected using HSTX1_CLKOUT_SEL) before giving it out onto HSTX1_CLKOUTP/N. 0000 = Divide by 1 (Default 4'b0000) 0001 = RESERVED 0010 = RESERVED 0011 = RESERVED 0100 = Divide by 2 0101 = RESERVED 0110 = RESERVED 0111 = RESERVED 1000 = Divide by 4 1001 = Divide by 8 1010 = Divide by 16 1011 = RESERVED 1100 = Divide by 5 1101 = Divide by 10 1110 = Divide by 20 1111 = Divide by 25	RW
11	HSTX1_CLKOUT_ EN	Output clock enable. 0 = Holds HSTX1_CLKOUTP/N output to a fixed value. 1 = Allows HSTX1_CLKOUTP/N output to toggle normally. (Default 1'b1)	RW
10	HSTX1_CLKOUT_ POWERDOWN	0 = Normal operation 1 = Enable HSTX1_CLKOUTP/N Power Down (Default 1'b1)	RW
9:8	HSTX1_CLKOUT_SEL[1:0]	Output clock select. Selected HS TXBCLK sent out on HSTX1_ CLKOUTP/N pins 00 = Selects Channel A HSTXBCLK clock as output clock (Default 2'b00) 01 = Selects Channel B HSTXBCLK clock as output clock 10 = Selects Channel C HSTXBCLK clock as output clock 11 = Selects Channel D HSTXBCLK clock as output clock	RW
7:4	HSTX0_CLKOUT_DIV[3:0]	HSTX0_CLKOUT Output clock divide setting. This value is used to divide selected clock (Selected using HSTX0_CLKOUT_SEL) before giving it out onto HSTX0_CLKOUTP/N. 0000 = Divide by 1 (Default 4'b0000) 0001 = RESERVED 0010 = RESERVED 0011 = RESERVED 0100 = Divide by 2 0101 = RESERVED 0110 = RESERVED 0111 = RESERVED 1000 = Divide by 4 1001 = Divide by 8 1010 = Divide by 16 1011 = RESERVED 1100 = Divide by 5 1101 = Divide by 10 1110 = Divide by 20 1111 = Divide by 25	RW
3	HSTX0_CLKOUT_ EN	Output clock enable. 0 = Holds HSTX0_CLKOUTP/N output to a fixed value. 1 = Allows HSTX0_CLKOUTP/N output to toggle normally. (Default 1'b1)	RW
2	HSTX0_CLKOUT_ POWERDOWN	0 = Normal operation 1 = Enable HSTX0_CLKOUTP/N Power Down(Default 1'b1)	RW
1:0	HSTX0_CLKOUT_SEL[1:0]	Output clock select. Selected HS TXBCLK sent out on HSTX0_ CLKOUTP/N pins 00 = Selects Channel A HSTXBCLK clock as output clock (Default 2'b00) 01 = Selects Channel B HSTXBCLK clock as output clock 10 = Selects Channel C HSTXBCLK clock as output clock 11 = Selects Channel D HSTXBCLK clock as output clock	RW

(1) This register is channel independent.

Table 5-198. LS_CLKOUT_PWRDWN_CONTROL

Device Address: 0x1E Register Address: 0x001B Default: 0x0063			
Bit	**Name**	**Description**	**Access**
6:2	RESERVED	For TI use only (Default 5'b11000)	RW
1	LS1_CLKOUT_POWERDOWN	0 = Normal operation 1 = Enable LS1_CLKOUTP/N Power Down (Default 1'b1)	
0	LS0_CLKOUT_POWERDOWN	0 = Normal operation (Default 1'b1) 1 = Enable LS0_CLKOUTP/N Power Down (Default 1'b1)	

Table 5-199. LS_CH_CONTROL_1

Device Address: 0x1E Register Address: 0x001C Default: 0x0000			
Bit	**Name**	**Description**	**Access**
9:8	RESERVED	For TI use only (Default 2'b00)	RW
3:2	RESERVED	For TI use only (Default 2'b00)	

Table 5-200. HS_CH_CONTROL_1

Device Address: 0x1E Register Address: 0x001C Default: 0x0000			
Bit	**Name**	**Description**	**Access**
13	REFCLK_FREQ_SEL_1	Input REFCLK frequency selection MSB. Applicable in 10GKR/1GKX modes only. When set, HS_PLL_MULT, LS_MPY and HS/LS TX/RX RATE settings can be set through related control bits specified in registers 30.2, 30.3, 30.6 0 = HS_PLL_MULT, LS_MPY and HS/LS TX/RX RATE are set automatically based on input REFCLK frequency as specified in REFCLK_FREQ_SEL_0(30.29.12) (Default 1'b0) 1 = Set this value if HS_PLL_MULT, LS_MPY and HS/LS TX/RX RATE values are NOT to be set automatically.	RW
12	REFCLK_FREQ_SEL_0	Input REFCLK frequency selection LSB. Applicable only when REFCLK_FREQ_SEL_1(30.29.13) is set to 0. 0 = Set this value if REFCLK frequency is 156.25 MHz (Default 1'b0) 1 = Set this value if REFCLK frequency is 312.5 MHz	
11	RX_CTC_BYPASS	0 = Normal operation. (Default 1'b0) 1 = Disables RX CTC operation.	
10	TX_CTC_BYPASS	0 = Normal operation. (Default 1'b0) 1 = Disables TX CTC operation.	
9:8	RESERVED	For TI use only (Default 2'b00)	
3:2	RESERVED	For TI use only (Default 2'b00)	

Table 5-201. EXT_ADDRESS_CONTROL

Device Address: 0x1E Register Address: 0x001E Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	EXT_ADDR_CONTROL[15:0]	Applicable in Clause 22 mode only. This register should be written with the extended register address to be written/read. Contents of address written in this register can be accessed from Reg 31 (0x001F). (Default 16'h0000)	RW

Table 5-202. EXT_ADDRESS_DATA

Device Address: 0x1E Register Address: 0x001F Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	EXT_ADDR_DATA[15:0]	Applicable in Clause 22 mode only. This register contains the data associated with the register address written in Register 30 (0x001E).	RW

The registers below can be accessed directly through Clause 45 and indirectly through Clause 22. Contains mode specific control/status registers and implemented per channel basis.

Table 5-203. VS_SERDES_CFG_OVERRIDE_CTRI

Device Address: 0x1E Register Address: 0x8020 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15	LS_PLL_MULT_OVERRIDE	1 = Override PLL_MULT value going into LS Serdes with MDIO configured value(Default 1'b0)	RW
14	LS_RATE_ OVERRIDE	1 = Override RATE value going into LS Serdes with MDIO configured value(Default 1'b0)	
13	HS_PLL_MULT_OVERRIDE	1 = Override PLL_MULT value going into HS Serdes with MDIO configured value(Default 1'b0)	
12	HS_RATE_OVERRIDE	1 = Override RATE value going into HS Serdes with MDIO configured value(Default 1'b0)	
10	RESERVED	NA	

Table 5-204. AUTO_CLKOUT_CONTROL

Device Address: 0x1E Register Address: 0x8021 Default: 0x000f			
Bit	**Name**	**Description**	**Access**
7	RESERVED	For TI use only (Default 1'b0)	RW
6	RESERVED	For TI use only (Default 1'b0) Must be set to 1.	
5	RESERVED	For TI use only (Default 1'b0) Must be set to 1.	
4	RESERVED	For TI use only (Default 1'b0)	
3	RX_CLKOUT_EN_AUTO_ DISABLE	This bit controls the signal which flat lines RX CLKOUT 1 = RX CLKOUT clock flat lined if HS PLL lock is lost or if HS LOS is detected (Default 1'b1) 0 = RX CLKOUT clock not flat lined if HS PLL lock is lost or if HS LOS is detected Must be set to 1.	
2	RX_CLKOUT_PWRDWN_ AUTO_DISABLE	This bit controls the signal which power down RX CLKOUT output buffer 1 = RX CLKOUT output buffer powered down if HS PLL lock is lost or if HS LOS is detected (Default 1'b1) 0 = RX CLKOUT output buffer not powered down if HS PLL lock is lost or if HS LOS is detected Must be set to 1.	
1	RESERVED	For TI use only (Default 1'b1) Must be set to 1.	
0	RESERVED	For TI use only (Default 1'b1) Must be set to 1.	

Table 5-205. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address: 0x8022 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	RESERVED	For TI use only (Default 16'h0000)	RW

Table 5-206. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address: 0x8023 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	RESERVED	For TI use only (Default 16'h0000)	RW

Table 5-207. TI_RESERVED_STATUS

Device Address: 0x1E Register Address: 0x8030 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
13:0	RESERVED	For TI use only.	RO

Table 5-208. TI_RESERVED_STATUS

Device Address: 0x1E Register Address: 0x8031 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	RESERVED	For TI use only	RO

Table 5-209. TI_RESERVED_STATUS

Device Address: 0x1E Register Address: 0x8032 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
11:0	RESERVED	For TI use only	RO

Table 5-210. TI_RESERVED_STATUS

Device Address: 0x1E Register Address: 0x8033 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
11:0	RESERVED	For TI use only	RO

Table 5-211. TI_RESERVED_STATUS

Device Address: 0x1E Register Address: 0x8034 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
9:0	RESERVED	For TI use only	RO

Table 5-212. TI_RESERVED_STATUS

Device Address: 0x1E Register Address: 0x8035 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
6:0	RESERVED	For TI use only	RO

Table 5-213. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address: 0x8050 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
3:0	RESERVED	For TI use only (Default 4’b0000)	RW

Table 5-214. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address: 0x8100 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
10:0	RESERVED	For TI use only (Default 11’b000000000000)	RW

Table 5-215. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address: 0x8101 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
10:0	RESERVED	For TI use only (Default 11’b000000000000)	RW

The registers below can be accessed directly through Clause 45 and indirectly through Clause 22. Contains device specific debug control/status registers and not implemented per channel basis (i.e. same physical register accessed irrespective of channel addressed)

Table 5-216. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address: 0x9000 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
11:8	RESERVED	For TI use only. (Default 4'b0000)	RW
5:4	RESERVED	For TI use only. (Default 2'b00)	
0	RESERVED	For TI use only. (Default 1'b0)	

5.6.2.2 PMA/PMD Registers

The registers below can be accessed only in Clause 45 mode and with device address field set to 0x01 (DA[4:0] = 5'b00001).

Table 5-217. PMA_CONTROL_1

Device Address: 0x01 Register Address: 0x0000 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15	RESET	1 = Global reset. Resets datapath and MDIO registers of all channels. Equivalent to asserting RESET_N. 0 = Normal operation (Default 1'b0)	RW/SC
11	POWERDOWN	1 = Enable power down mode 0 = Normal operation (Default 1'b0)	RW
0	LOOPBACK	1 = Enables loopback on HS serial side. LS data traverses through entire Tx datapath including HS serdes and will be available at LS output side 0 = Normal operation (Default 1'b0)	RW

Table 5-218. PMA_STATUS_1

Device Address: 0x01 Register Address: 0x0001 Default: 0x0002			
Bit	**Name**	**Description**	**Access**
1	LOW_POWER_ABILITY	Always reads 1. 1 = Supports low power mode 0 = Does not support low power mode	RO

Table 5-219. PMA_DEV_IDENTIFIER_1

Device Address: 0x01 Register Address: 0x0002 Default: 0x4000			
Bit	**Name**	**Description**	**Access**
0	DEV_IDENTIFIER[31:16]	16 MSB of 32 bit unique device identifier. See Table 5-79 for identifier code details.	RO

Table 5-220. PMA_DEV_IDENTIFIER_2

Device Address: 0x01 Register Address: 0x0003 Default: 0x50F0			
Bit	**Name**	**Description**	**Access**
15:0	DEV_IDENTIFIER[15:0]	16 LSB of 32 bit unique device identifier. See Table 5-79 for identifier code details.	RO

Table 5-221. UNIQUE DEVICE IDENTIFIER(1)

Register Address	Value	Description
15:0	16'b0100_0000_0000_0000	OUI[3-18]
15:10	6'b010100	OUI[19-24]
9:4	6'b001111	6-bit Manufacturer device model number
3:0	4'b0000	4-bit Manufacturer device revision number

(1) The identifier code is composed of bits 3-24 of 25-bit organizationally unique identifier (OUI) assigned to Texas Instruments by IEEE. The 6-bit Manufacturer device model number is unique to TLK10034. The 4-bit Manufacturer device revision number denotes the current revision of TLK10034.

Table 5-222. PMA_SPEED_ABILITY

Device Address: 0x01 Register Address: 0x0004 Default: 0x0011			
Bit	**Name**	**Description**	**Access**
4	SPEED_1G	Always reads 1. 1 = Capable of operating at 1000 Mb/s 0 = Not capable of operating at 1000 Mb/s	RO
0	SPEED_10G	Always reads 1. 1 = Capable of operating at 10 Gb/s 0 = Not capable of operating at 10 Gb/s	

Table 5-223. PMA_DEV_PACKAGE_1

Device Address: 0x01 Register Address: 0x0005 Default: 0x000B			
Bit	**Name**	**Description**	**Access**
3	PCS_ PRESENT	Always reads 1. 1 = PCS present in the package 0 = PCS not present in the package RO	RO
1	PMA_PMD_PRESENT	Always reads 1. 1 = PMA/PMD present in the package 0 = PMA/PMD not present in the package	
0	CL22_PRESENT	Always reads 1. 1 = Clause 22 registers present in the package 0 = Clause 22 registers not present in the package	

Table 5-224. PMA_DEV_PACKAGE_2

Device Address: 0x01 Register Address: 0x0006 Default: 0x4000			
Bit	**Name**	**Description**	**Access**
15	VS_DEV2_PRESENT	Always reads 0. 1 = Vendor specific device 2 present in the package 0 = Vendor specific device 2 not present in the package	RO
14	VS_DEV1_PRESENT	Always reads 1. 1 = Vendor specific device 1 present in the package 0 = Vendor specific device 1 not present in the package	RO

Table 5-225. PMA_STATUS_2

Device Address: 0x01 Register Address: 0x0008 Default: 0xb000			
Bit	**Name**	**Description**	**Access**
15:14	DEV_PRESENT	Always reads 2'b10 0x = No device responding at this address 10 = Device responding at this address 11 = No device responding at this address	RO
8	TX_DISABLE_ABILITY	Always reads 1'b0. 1 = Able to perform transmit disable function 0 = Not able to perform transmit disable function	RO

Table 5-226. PMA_EXTENDED_ABILITY

Device Address: 0x01 Register Address: 0x000B Default: 0x0050			
Bit	**Name**	**Description**	**Access**
6	KX_ABILITY	Always reads 1'b1 1 = Able to perform 1000BASE-KX 0 = Not able to perform 1000BASE-KX	RO
4	KR_ABILITY	Always reads 1'b1 1 = Able to perform 10GBASE-KR 0 = Not able to perform 10GBASE-KR	RO

Table 5-227. KX_STATUS

Device Address: 0x01 Register Address: 0x00A1 Default: 0x3000			
Bit	**Name**	**Description**	**Access**
13	KX_TX_FAULT_ABILITY	Always reads 1. 1 = Has ability to detect a fault condition on transmit path 0 = Does not have ability to detect a fault condition on transmit path	RO
12	KX_RX_FAULT_ABILITY	Always reads 1. 1 = Has ability to detect a fault condition on receive path 0 = Does not have ability to detect a fault condition on receive path	RO
11	KX_TX_FAULT	1 = Fault condition detected on transmit path 0 = No fault condition detected on transmit path	RO/LH
10	KX_RX_FAULT	1 = Fault condition detected on receive path 0 = No fault condition detected on receive path	RO/LH
0	KX_RX_SIGNAL_DETECT	1 = Signal detected 0 = Signal not detected	RO

5.6.2.3 Auto-Negotiation Registers

The registers below can be accessed only in Clause 45 mode and with device address field set to 0x07 (DA[4:0] = 5'b00111)

Table 5-228. AN_CONTROL

Device Address: 0x07 Register Address: 0x0000 Default: 0x3000			
Bit	**Name**	**Description**	**Access**
15	AN_RESET	1 = Resets Auto Negotiation 0 = Normal operation (Default 1'b0)	RW/SC
13	RESERVED	For TI use only (Default 1'b1)	RW
12	AN_ENABLE	1 = Enable Auto Negotiation (Default 1'b1) 0 = Disable Auto Negotiation	RW
9	AN_RESTART	1 = Restart Auto Negotiation 0 = Normal operation (Default 1'b0) If set, a read of this register is required to clear AN_RESTART bit.	RW/SC(1)

(1) If set, a read of register 7.0 is required to clear AN_RESTART bit.

Table 5-229. AN_STATUS

Device Address: 0x07 Register Address: 0x0001 Default: 0x0088			
Bit	**Name**	**Description**	**Access**
9	AN_PAR_DET_FAULT	1 = Fault has been detected via parallel detection function 0 = Fault has not been detected via parallel detection function	RO/LH
7	AN_EXP_NP_STATUS	1 = Extended next page is used 0 = Extended next page is not allowed	RO
6	AN_PAGE_RCVD	1 = A page has been received 0 = A page has not been received	RO/LH
5	AN_COMPLETE	1 = Auto Negotiation process is completed 0 = Auto Negotiation process not completed	RO

Table 5-229. AN_STATUS (continued)

Device Address: 0x07 Register Address: 0x0001 Default: 0x0088			
Bit	**Name**	**Description**	**Access**
4	REMOTE_FAULT	Always reads 0. Fault condition status can be read at 7.1.9 and 7.1.2.	RO
3	AN_ABILITY	Always reads 1. 1 = Device is able to perform Auto Negotiation 0 = Device not able to perform Auto Negotiation	RO
2	LINK_STATUS	1 = Link is up 0 = Link is down	RO/LL
0	AN_LP_ABILITY	1 = LP is able to perform Auto Negotiation 0 = LP not able to perform Auto Negotiation	RO

Table 5-230. AN_DEV_PACKAGE

Device Address: 0x07 Register Address: 0x0005 Default: 0x0080			
Bit	**Name**	**Description**	**Access**
7	AN_PRESENT	Always reads 1 1 = Auto Negotiation present in the package 0 = Auto Negotiation not present in the package	RO

Table 5-231. AN_ADVERTISEMENT_1

Device Address: 0x07 Register Address: 0x0010 Default: 0x1001			
Bit	**Name**	**Description**	**Access**
15	AN_NEXT_PAGE	NP bit (D15) in base link codeword 1 = Next page available 0 = Next page not available (Default 1'b0)	RW
14	AN_ACKNOWLEDGE	Acknowledge bit (D14) in base link codeword. Always reads 0.	RO
13	AN_REMOTE_FAULT	RF bit (D13) in base link codeword 1 = Sets RF bit to 1 0 = Normal operation (Default 1'b0)	RW
12:10	AN_CAPABILITY[2:0]	Value to be set in D12:D10 bits of the base link codeword. Consists of abilities like PAUSE, ASM_DIR (Default 3'b100)	RW
9:5	AN_ECHO_NONCE[4:0]	Value to be set in D9:D5 bits of the base link codeword. Consists of Echo nonce value. Transmitted in base page only until local device and link Partner have exchanged unique Nonce values, at which time transmitted Echoed Nonce will change to Link Partner's Nonce value. Read value always reflects the value written, not the actual Echoed Nonce. (Default 5'b00000)	RW
4:0	AN_SELECTOR[4:0]	Value to be set in D4:D0 bits of the base link codeword. Consists of selector field value (Default 5'b00001)	RW

Table 5-232. AN_ADVERTISEMENT_2

Device Address: 0x07 Register Address: 0x0011 Default: 0x0080			
Bit	**Name**	**Description**	**Access**
15:8	AN_ABILITY[10:3]	Value to be set in D31:D24 bits of the base link codeword. Consists of technology ability field bits [10:3] (Default 9'b000000000)	RW
7	AN_ABILITY[2]	Value to be set in D23 bits of the base link codeword. Consists of technology ability field bits [2]. When set, indicates device supports 10GBASE-KR (Default 1'b1)	
6	AN_ABILITY[1]	Value to be set in D22 bits of the base link codeword. Consists of technology ability field bits [1]. Always set to 0 (Default 1'b0)	
5	AN_ABILITY[0]	Value to be set in D21 bits of the base link codeword. Consists of technology ability field bit [0]. When set, indicates device supports 1000BASE-KX (Default 1'b0)	
4:0	AN_TRANS_NONCE_ FIELD[4:0]	Not used. Transmitted Nonce field is generated by hardware random number generator. Read value always reflects value written, not the actual Transmitted Nonce (Default 5'b00000)	

Table 5-233. AN_ADVERTISEMENT_3

Device Address: 0x07 Register Address: 0x0012 Default: 0x4000			
Bit	**Name**	**Description**	**Access**
15	AN_FEC_REQUESTED	Value to be set in D47 bits of the base link codeword. When set, indicates a request to enable FEC on the link (Default 1'b0)	RW
14	AN_FEC_ABILITY	Value to be set in D46 bits of the base link codeword. When set, indicates 10GBASE-KR has FEC ability (Default 1'b1)	
13:0	AN_ABILITY[24:11]	Value to be set in D45:D32 bits of the base link codeword. Consists of technology ability field bits [24:11] (Default 14'b00000000000000)	

Table 5-234. AN_LP_ADVERTISEMENT_1(1)

Device Address: 0x07 Register Address: 0x0013 Default: 0x0001			
Bit	**Name**	**Description**	**Access**
15	AN_LP_NEXT_PAGE	NP bit (D15) in link partner base page 1 = Next page available in link partner 0 = Next page not available in link partner	RO
14	AN_LP_ACKNOWLEDGE	Acknowledge bit (D14) in link partner base page.	RO
13	AN_LP_REMOTE_FAULT	RF bit (D13) in link partner base page 1 = Remote fault detected in link partner 0 = Remote fault not detected in link partner	RO
12:10	AN_ LP_CAPABILITY	D12:D10 bits of the link partner base page. Consists of abilities like PAUSE, ASM_DIR	RO
9:5	AN_ LP_ECHO_NONCE	D9:D5 bits of the link partner base page. Consists of Echo nonce value	RO
4:0	AN_LP_SELECTOR[4:0]	D4:D0 bits of the link partner base page. Consists of selector field value Always reads 5'b00001	RO

(1) To get accurate AN_LP_ADVERTISEMENT read value, Register 7.19 should be read first before reading 7.20 and 7.21

Table 5-235. AN_LP_ADVERTISEMENT_2

Device Address: 0x07 Register Address: 0x0014 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:8	AN_ LP_ABILITY[10:3]	D31:D24 bits of the link partner base page. Consists of technology ability field bits [10:3]	RO
7	AN_LP_ABILITY[2]	D23 bits of the link partner base page. Consists of technology ability field bits [2]. When high, indicates link partner supports 10GBASE-KR	
6	AN_LP_ABILITY[1]	D22 bits of the link partner base page. Consists of technology ability field bits [1].	
5	AN_LP_ABILITY[0]	D21 bits of the link partner base page. Consists of technology ability field bit [0]. When high, indicates link partner supports 1000BASE-KX	
4:0	AN_LP_TRANS_NONCE_FIELD	D20:D16 bits of the link partner base page. Consists of transmitted nonce value	

Table 5-236. AN_LP_ADVERTISEMENT_3

Device Address: 0x07 Register Address: 0x0015 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15	AN_LP_FEC_REQUESTED	D47 bits of the link partner base page. When high, indicates link partner request to enable FEC on the link	RO
14	AN_LP_FEC_ABILITY	D46 bits of the link partner base page. When high, indicates link partner has FEC ability	
13:0	AN_LP_ABILITY[24:11]	D45:D32 bits of the link partner base page. Consists of link partner technology ability field bits [24:11]	

Table 5-237. AN_XNP_TRANSMIT_1

Device Address: 0x07 Register Address: 0x0016 Default: 0x2000			
Bit	**Name**	**Description**	**Access**
15	AN_XNP_NEXT_PAGE	NP bit (D15) in next page code word 1 = Next page available 0 = Next page not available (Default 1'b0)	RW
14	RESERVED	Always reads 0.	RO
13	AN_MP	Message page bit (D13) in next page code word 1 = Sets MP bit to 1 indicating next page is a message page (Default 1'b1) 0 = Sets MP bit to 0 indicating next page is unformatted next page	RW
12	AN_ACKNOWLEDGE_2	Value to be set in D12 bit of the next page code word. When set, indicates device is able to act on the information defined in the message (Default 1'b0)	RW
11	AN_TOGGLE	Not used. Toggle value is generated by hardware. Read value always reflects value written, not the actual Toggle field (Default 1'b0)	RW
10:0	AN_CODE_FIELD	Value to be set in D10:D0 bits of the next page code word. Consists of Message/Unformatted code field value (Default 11'b00000000000)	RW

Table 5-238. AN_XNP_TRANSMIT_2

Device Address: 0x07 Register Address: 0x0017 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	AN_MSG_CODE_1	Value to be set in D31:D16 bits of the next page code word. Consists of Message/Unformatted code field value (Default 16'b0000000000000000)	RW

Table 5-239. AN_XNP_TRANSMIT_3

Device Address: 0x07 Register Address: 0x0018 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	AN_MSG_CODE_2	Value to be set in D47:D32 bits of the next page code word. Consists of Message/Unformatted code field value (Default 16'b0000000000000000)	RW

Table 5-240. AN_LP_XNP_ABILITY_1(1)

Device Address: 0x07 Register Address: 0x0019 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15	AN_LP_XNP_NEXT_PAGE	NP bit (D15) in next page code word 1 = Next page available 0 = Next page not available (Default 1'b0)	RO
14	AN_LP_XNP_ACKNOWLEDGE	Value in D14 bit of the next page code word. When set, indicates device is able to act on the information defined in the message (Default 1'b0)	
13	AN_LP_MP	Message page bit (D13) in next page code word 1 = Sets MP bit to 1 indicating next page is a message page 0 = Sets MP bit to 0 indicating next page is unformatted next page (Default 1'b0)	
12	AN_LP_ACKNOWLEDGE_2	Value in D12 bit of the next page code word. When set, indicates device is able to act on the information defined in the message (Default 1'b0)	
11	AN_LP_TOGGLE	Value of D11 bit of the next page code word. Consists of Toggle field value(Default 1'b0)	
10:0	AN_ LP_CODE_FIELD	Value in D10:D0 bits of the next page code word. Consists of Message/Unformatted code field value (Default 11'b00000000000)	

(1) To get accurate AN_LP_XNP_ABILITYT read value, Register 7.25 should be read first before reading 7.26 and 7.27

Table 5-241. AN_LP_XNP_ABILITY_2

Device Address: 0x07 Register Address: 0x001A Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	AN_LP_MSG_CODE_1	Value to be set in D31:D16 bits of the next page code word. Consists of Message/Unformatted code field value (Default 16'b0000000000000000)	RO

Table 5-242. AN_LP_XNP_ABILITY_3

Device Address: 0x07 Register Address: 0x001B Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	AN_LP_MSG_CODE_2	Value to be set in D47:D32 bits of the next page code word. Consists of Message/Unformatted code field value (Default 16'b0000000000000000)	RO

Table 5-243. AN_BP_STATUS

Device Address: 0x07 Register Address: 0x0030 Default: 0x0001			
Bit	**Name**	**Description**	**Access**
4	AN_10G_KR_FEC	1 = PMA/PMD is negotiated to perform 10GBASE-KR FEC	RO
3	AN_10G_KR	1 = PMA/PMD is negotiated to perform 10GBASE-KR	
1	AN_1G_KX	1 = PMA/PMD is negotiated to perform 1000BASE-KX	
0	AN_BP_AN_ABILITY	Always reads 1. 1 = Indicates 1000BASE-KX, 10GBASE-KR is implemented	

5.6.3 10G Programmers Reference

5.6.3.1 Vendor Specific Device Registers

The registers below can be accessed directly through Clause 22 and Clause 45. In Clause 45 mode, these registers can be accessed by setting device address field to 0x1E (DA[4:0] = 5'b11110). In Clause 22 mode, these registers can be accessed by setting 5 bit register address field to same value as 5 LSB bits of Register Address field specified for each register. For example, 16 bit register address 0x001C in clause 45 mode can be accessed by setting register address field to 5'h1C in clause 22 mode.

Table 5-244. GLOBAL_CONTROL_1 (1)

Device Address: 0x1E Register Address: 0x0000 Default: 0x0020			
Bit	**Name**	**Description**	**Access**
15	GLOBAL_RESET	Global reset. 0 = Normal operation (Default 1'b0) 1 = Resets TX and RX data path including MDIO registers. Equivalent to asserting RESET_N.	RW SC (2)
11	GLOBAL_WRITE	Global write enable. 0 = Control settings are specific to channel addressed (Default 1'b0) 1 = Control settings in channel specific registers are applied to all 4 channels regardless of channel addressed RW	RW

(1) This global register is channel independent.
(2) After reset bit is set to one, it automatically sets itself back to zero on the next MDC clock cycle.

Table 5-244. GLOBAL_CONTROL_1[(1)] (continued)

Device Address: 0x1E Register Address: 0x0000 Default: 0x0020			
Bit	**Name**	**Description**	**Access**
5:0	PRBS_PASS_ OVERLAY[5:0]	PRBS_PASS pin status selection. Applicable only when PRBS test pattern verification is enabled on HS side or LS side. PRBS_PASS pin reflects PRBS verification status on selected Channel HS/LS side 1xx000 = PRBS_PASS reflects combined status of Channel A/B/C/D HS serdes PRBS verification. If PRBS verification fails on any channel HS serdes, PRBS_PASS will be asserted low. (Default 6'b100000) 000000 = Status from Channel A HS Serdes side 000001 = Reserved 00001x = Reserved 000100 = Status from Channel A LS Serdes side Lane 0 000101 = Status from Channel A LS Serdes side Lane 1 000110 = Status from Channel A LS Serdes side Lane 2 000111 = Status from Channel A LS Serdes side Lane 3 001000 = Status from Channel B HS Serdes side 001001 = Reserved 00101x = Reserved 001100 = Status from Channel B LS Serdes side Lane 0 001101 = Status from Channel B LS Serdes side Lane 1 001110 = Status from Channel B LS Serdes side Lane 2 001111 = Status from Channel B LS Serdes side Lane 3 010000 = Status from Channel C HS Serdes side 010001 = Reserved 01001x = Reserved 010100 = Status from Channel C LS Serdes side Lane 0 010101 = Status from Channel C LS Serdes side Lane 1 010110 = Status from Channel C LS Serdes side Lane 2 010111 = Status from Channel C LS Serdes side Lane 3 011000 = Status from Channel D HS Serdes side 011001 = Reserved 01101x = Reserved 011100 = Status from Channel D LS Serdes side Lane 0 011101 = Status from Channel D LS Serdes side Lane 1 011110 = Status from Channel D LS Serdes side Lane 2 011111 = Status from Channel D LS Serdes side Lane 3	RW

Table 5-245. CHANNEL_CONTROL_1

Device Address: 0x1E Register Address: 0x0001 Default: 0x0B88			
Bit	**Name**	**Description**	**Access**
15	POWERDOWN	Setting this bit high powers down entire data path with exception that MDIO interface stays active. 0 = Normal operation (Default 1'b0) 1 = Power Down mode is enabled.	RW
14	HSRX_CLKOUT_ POWERDOWN	0 = Normal operation (Default 1'b0) 1 = Enable HSRXx_CLKOUTP/N Power Down.	RW
13	10G_RX_MODE_SEL	RX mode selection. Valid in 10G only. 0 = RX mode dependent upon RX_DEMUX_SEL(Default 1'b0) 1 = Enables 1 to 1 mode on receive channel. Requires HS_DEC_BYPASS(30.29.2) to be set.	RW
12	10G_TX_MODE_SEL	TX mode selection Valid in 10G only. 0 = TX mode dependent upon TX_MUX_SEL (Default 1'b0) 1 = Enables 1 to 1 mode on transmit channel. Requires HS_ENC_BYPASS (30.29.3) to be set.	RW
11	SW_PCS_SEL	NA.	RW
10	SW_DEV_MODE_SEL	Valid only when MODE_SEL pin is 0 1 = Device set to 10G mode 0 = NA(Default 1'b0)	RW
9	10G_RX_DEMUX_SEL	RX De-Mux selection control for lane de-serialization on receive channel. Valid when 10G_RX_MODE_SEL (30.1.13) is LOW 0 = 1 to 2 1 = 1 to 4 (Default 1'b1)	RW
8	10G_TX_MUX_SEL	TX Mux selection control for lane serialization on transmit channel. Valid when 10G_TX_MODE_SEL (30.1.12) is LOW 0 = 2 to 1 1 = 4 to 1 (Default 1'b1)	RW

Table 5-245. CHANNEL_CONTROL_1 (continued)

Device Address: 0x1E Register Address: 0x0001 Default: 0x0B88			
Bit	**Name**	**Description**	**Access**
7:4	HSRX_CLKOUT_DIV[3:0]	Output clock divide setting. This value is used to divide selected clock (Selected using HSRX_CLKOUT_SEL) before giving it out onto respective channel HSRXx_CLKOUTP/N. 0000 = Divide by 1 0001 = RESERVED 0010 = RESERVED 0011 = RESERVED 0100 = Divide by 2 0101 = RESERVED 0110 = RESERVED 0111 = RESERVED 1000 = Divide by 4 (Default 4'b1000) 1001 = Divide by 8 1010 = Divide by 16 1011 = RESERVED 1100 = Divide by 5 1101 = Divide by 10 1110 = Divide by 20 1111 = Divide by 25	RW
3	HSRX_CLKOUT_ EN	Output clock enable. 0 = Holds HSRXx_CLKOUTP/N output to a fixed value. 1 = Allows HSRXx_CLKOUTP/N output to toggle normally (Default 1'b1)	RW
2	HSRX_CLKOUT_SEL	Output clock select. Selected Recovered clock sent out on HSRXx_CLKOUTP/N pins 0 = Selects respective Channel HSRX recovered byte clock as output clock (Default 1'b0) 1 = Selects respective Channel HSRX VCO divide by 2 clock as output clock	RW
1	REFCLK_SW_SEL	Channel HS Reference clock selection. Applicable only when REFCLK_SEL pin is LOW. 0 = Selects REFCLK_0_P/N as clock reference to Channel x HS side serdes macro(Default 1'b0) 1 = Selects REFCLK_1_P/N as clock reference to Channel x HS side serdes macro	RW
0	LS_REFCLK_SEL	Channel LS Reference clock selection. 0 = LS side serdes macro reference clock is same as HS side serdes reference clock (E.g. If REFCLK_0_P/N is selected as HS side serdes macro reference clock, REFCLK_0_P/N is selected as LS side serdes macro reference clock and vice versa) (Default 1'b0) 1 = Alternate reference clock is selected as clock reference to Channel x LS side serdes macro (E.g. If REFCLK_0_P/N is selected as HS side serdes macro reference clock, REFCLK_1_P/N is selected as LS side serdes macro reference clock and vice versa)	RW

Table 5-246. HS_SERDES_CONTROL_1

Device Address: 0x1E Register Address: 0x0002 Default: 0x811D			
Bit	**Name**	**Description**	**Access**
15:10	RESERVED	For TI use only (Default 9'b100000)	RW
9:8	HS_LOOP_BANDWIDTH [1:0]	HS Serdes PLL Loop Bandwidth settings 00 = Reserved 01 = Narrow bandwidth (Default 2'b01) 10 = Medium bandwidth 11 = Highest bandwidth.	RW
7	RESERVED	For TI use only (Default 1'b0)	
6	HS_VRANGE	HS Serdes PLL VCO range selection. 0 = VCO runs at higher end of frequency range (Default 1'b0) 1 = VCO runs at lower end of frequency range This bit needs to be set HIGH if VCO frequency (REFCLK * HS_PLL_MULT) is below 2.5 GHz.	
5	RESERVED	For TI use only (Default 1'b0)	

Table 5-246. HS_SERDES_CONTROL_1 (continued)

Device Address: 0x1E Register Address: 0x0002 Default: 0x811D			
Bit	**Name**	**Description**	**Access**
4	HS_ENPLL	HS Serdes PLL enable control. HS Serdes PLL is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 30.1.15 is set HIGH. 0 = Disables PLL in HS serdes 1 = Enables PLL in HS serdes (Default 1'b1)	
3:0	HS_PLL_MULT[3:0]	HS Serdes PLL multiplier setting (Default 4'b1101). Refer Table 5-23. Refer to 10G supported rates for more information on valid PLL multiplier settings	

Table 5-247. HS PLL Multiplier Control

30.2.3:0		30.2.3:0	
Value	**PLL Multiplier Factor**	**Value**	**PLL Multiplier Factor**
0000	Reserved	1000	12x
0001	Reserved	1001	12.5x
0010	4x	1010	15x
0011	5x	1011	16x
0100	6x	1100	16.5x
0101	8x	1101	20x
0110	8.25x	1110	25x
0111	10x	1111	Reserved

Table 5-248. HS_ SERDES_CONTROL_2

Device Address: 0x1E Register Address: 0x0003 Default: 0x8848			
Bit	**Name**	**Description**	**Access**
15:12	HS_SWING[3:0]	Transmitter Output swing control for HS Serdes. (Default 4'b1000) Refer to Table 5-25.	RW
11	HS_ENTX	HS Serdes transmitter enable control. HS Serdes transmitter is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 30.1.15 is set HIGH. 0 = Disables HS serdes transmitter 1 = Enables HS serdes transmitter (Default 1'b1)	RW
10	HS_EQHLD	HSRX Equalizer hold control 0 = Normal operation (Default 1'b0) 1 = Holds equalizer and long tail correction in its current state	RW
9:8	HS_RATE_TX [1:0]	HS Serdes TX rate settings 00 = Full rate (Default 2'b00) 01 = Half rate 10 = Quarter rate 11 = Eighth rate	RW
7:4	RESERVED	For TI use only (Default 4'b0100)	RW
3	HS_ENRX	HS Serdes receiver enable control. HS Serdes receiver is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 30.1.15 is set HIGH. 0 = Disables HS serdes receiver 1 = Enables HS serdes receiver (Default 1'b1)	RW
2:0	HS_RATE_RX [2:0]	HS Serdes RX rate settings 000 = Full rate (Default 3'b000) 101 = Half rate 110 = Quarter rate 111 = Eighth rate 001 = Reserved 01x = Reserved 100 = Reserved	RW

Table 5-249. HSTX AC Mode Output Swing Control

VALUE 30.3[15:12]	AC MODE
	TYPICAL AMPLITUDE (mVdfpp)
0000	130
0001	220
0010	300
0011	390
0100	480
0101	570
0110	660
0111	750
1000	830
1001	930
1010	1020
1011	1110
1100	1180
1101	1270
1110	1340
1111	1400

Table 5-250. HS_SERDES_CONTROL_3

Device Address: 0x1E Register Address: 0x0004 Default: 0x1400			
Bit	**Name**	**Description**	**Access**
15	HS_ENTRACK	HSRX ADC Track mode 0 = Normal operation (Default 1'b0) 1 = Forces ADC into track mode	RW
14:12	HS_EQPRE[2:0]	Serdes Rx precursor equalizer selection 000 = 1/9 cursor amplitude 001 = 3/9 cursor amplitude (Default 3'b001) 010 = 5/9 cursor amplitude 011 = 7/9 cursor amplitude 100 = 9/9 cursor amplitude 101 = 11/9 cursor amplitude 110 = 13/9 cursor amplitude 111 = Disable	RW
11:10	HS_CDRFMULT[1:0]	Clock data recovery algorithm frequency multiplication selection 00 = First order. Frequency offset tracking disabled 01 = Second order. 1x mode 10 = Second order. 2x mode (Default 2'b10) 11 = Reserved	RW
9:8	HS_CDRTHR[1:0]	Clock data recovery algorithm threshold selection 00 = Four vote threshold (Default 2'b00) 01 = Eight vote threshold 10 = Sixteen vote threshold 11 = Thirty two vote threshold	RW
4.7	RESERVED	For TI use only (Default 1'b0)	RW
4.6	HS_PEAK_DISABLE	HS Serdes PEAK_DISABLE control 0 = Normal operation (Default 1'b0) 1 = Disables high frequency peaking. Suitable for <6 Gbps operation	RW
5	HS_H1CDRMODE	0 = Normal operation (Default 1'b0) 1 = Enables CDR mode suitable for short channel operation.	RW
4:0	HS_TWCRF[4:0]	Cursor Reduction Factor (Default 5'b00000) Refer to Table 5-27.	RW

Table 5-251. HSTX Cursor Reduction Factor Weights

30.4.4:0		30.4.4:0	
Value	**Cursor Reduction (%)**	**Value**	**Cursor Reduction (%)**
00000	0	10000	17
00001	2.5	10001	20
00010	5.0	10010	22
00011	7.5	10011	25
00100	10.0	10100	27
00101	12	10101	30
00110	15	10110	32
00111	Reserved	10111	35
01000		11000	37
01001		11001	40
01010		11010	42
01011		11011	45
01100		11100	47
01101		11101	50
01110		11110	52
01111		11111	55

Table 5-252. HS_SERDES_CONTROL_4

Device Address: 0x1E Register Address: 0x0005 Default: 0x2000			
Bit	**Name**	**Description**	**Access**
15	HS_RX_INVPAIR	Receiver polarity. 0 = Normal polarity. HSRXxP considered positive data. HSRXxN considered negative data (Default 1'b0) 1 = Inverted polarity. HSRXxP considered negative data. HSRXxN considered positive data	RW
14	HS_TX_INVPAIR	Transmitter polarity. 0 = Normal polarity. HSTXxP considered positive data and HSTXxN considered negative data (Default 1'b0) 1 = Inverted polarity. HSTXxP considered negative data and HSTXxN considered positive data	RW
13	RESERVED	For TI use only (Default 1'b1)	RW
12:8	HS_TWPOST1[4:0]	Adjacent post cursor1 Tap weight. Selects TAP settings for TX waveform. (Default 5'b00000) Refer to Table 5-29.	RW
7:4	HS_TWPRE[3:0]	Pre-cursor Tap weight. Selects TAP settings for TX waveform. (Default 4'b0000) Refer to Table 5-31.	RW
3:0	HS_TWPOST2[3:0]	Adjacent post cursor2 Tap weight. Selects TAP settings for TX waveform. (Default 4'b0000) Refer to Table 5-30.	RW

Table 5-253. HSTX Post-cursor1 Transmit Tap Weights

30.5.12:8		30.5.12:8	
Value	**Tap Weight (%)**	**Value**	**Tap Weight (%)**
00000	0	10000	0
00001	+2.5	10001	-2.5
00010	+5.0	10010	-5.0
00011	+7.5	10011	-7.5
00100	+10.0	10100	-10.0
00101	+12.5	10101	-12.5

Table 5-253. HSTX Post-cursor1 Transmit Tap Weights (continued)

30.5.12:8		30.5.12:8	
Value	Tap Weight (%)	Value	Tap Weight (%)
00110	+15.0	10110	-15.0
00111	+17.5	10111	-17.5
01000	+20.0	11000	-20.0
01001	+22.5	11001	-22.5
01010	+25.0	11010	-25.0
01011	+27.5	11011	-27.5
01100	+30.0	11100	-30.0
01101	+32.5	11101	-32.5
01110	+35.0	11110	-35.0
01111	+37.5	11111	-37.5

Table 5-254. HSTX Post-cursor2 Transmit Tap Weights

30.5.3:0		30.5.3:0	
Value	Tap Weight (%)	Value	Tap Weight (%)
0000	0	1000	0
0001	+2.5	1001	-2.5
0010	+5.0	1010	-5.0
0011	+7.5	1011	-7.5
0100	+10.0	1000	-10.0
0101	+12.5	1001	-12.5
0110	+15.0	1110	-15.0
0111	+17.5	1111	-17.5

Table 5-255. HSTX Pre-cursor Transmit Tap Weights

30.5.7:4		30.5.7:4	
Value	Tap Weight (%)	Value	Tap Weight (%)
0000	0	1000	0
0001	+2.5	1001	-2.5
0010	+5.0	1010	-5.0
0011	+7.5	1011	-7.5
0100	+10.0	1000	-10.0
0101	+12.5	1001	-12.5
0110	+15.0	1110	-15.0
0111	+17.5	1111	-17.5

Table 5-256. LS_SERDES_CONTROL_1

Device Address: 0x1E Register Address: 0x0006 Default: 0xF115			
Bit	**Name**	**Description**	**Access**
12	LS_LN_CFG_EN[3:0]	Configuration control for LS Serdes Lane settings (Default 4'b1111) [3] corresponds to LN3, [2] corresponds to LN2 [1] corresponds to LN1, [0] corresponds to LN0 0 = Writes to LS_SERDES_CONTROL_2 and LS_SERDES_CONTROL_3 and LS_CH_CONTROL_1 control registers do not affect respective LS Serdes lane 1 = Writes to LS_SERDES_CONTROL_2 and LS_SERDES_CONTROL_3 and LS_CH_CONTROL_1 control registers affect respective LS Serdes lane For example, if subsequent writes to LS_SERDES_CONTROL_2 and LS_SERDES_CONTROL_3 and LS_CH_CONTROL_1 registers need to affect the settings in Lanes 0 and 1, LS_LN_CFG_EN[3:0] should be set to 4'b0011 Read values in LS_SERDES_CONTROL_2 and LS_SERDES_CONTROL_3 & LS_CH_CONTROL_1 reflect the settings value for Lane selected through LS_LN_CFG_EN[3:0]. To read settings for Lane 0, LS_LN_CFG_EN[3:0] should be set to 4'b0001 To read settings for Lane 1, LS_LN_CFG_EN[3:0] should be set to 4'b0010 To read settings for Lane 2, LS_LN_CFG_EN[3:0] should be set to 4'b0100 To read settings for Lane 3, LS_LN_CFG_EN[3:0] should be set to 4'b1000 Read values of LS_SERDES_CONTROL_2 and LS_SERDES_CONTROL_3 and LS_CH_CONTROL_1 registers are not valid for any other LS_LN_CFG_EN[3:0] combination	RW
11:10	RESERVED	For TI use only(Default 2'b00)	RW
9:8	LS_LOOP_BANDWIDTH [1:0]	LS Serdes PLL Loop Bandwidth settings 00 = Reserved 01 = Applicable when external JC_PLL is NOT used (Default 2'b01) 10 = Applicable when external JC_PLL is used 11 = Reserved	RW
7:5	RESERVED	For TI use only (Default 3'b000)	RW
6.4	LS_ENPLL	LS Serdes PLL enable control. LS Serdes PLL is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 30.1.15 is set HIGH. 0 = Disables PLL in LS serdes 1 = Enables PLL in LS serdes (Default 1'b1)	RW
3:0	LS_MPY[3:0]	LS Serdes PLL multiplier setting (Default 4'b0101). Refer to Table 5-257. Refer 10G supported modes for more information on valid PLL multiplier settings	RW

Table 5-257. LS PLL Multiplier Control

30.6.3:0		30.6.3:0	
Value	**PLL Multiplier Factor**	**Value**	**PLL Multiplier Factor**
0000	4x	1000	15x
0001	5x	1001	20x
0010	6x	1010	25x
0011	Reserved	1011	Reserved
0100	8x	1100	Reserved
0101	10x	1101	50x
0110	12x	1110	65x
0111	12.5x	1111	Reserved

Table 5-258. LS_SERDES_CONTROL_2

Device Address: 0x1E Register Address: 0x0007 Default: 0xDC04			
Bit	**Name**	**Description**	**Access**
15	RESERVED	For TI use only.	RW
14:12	LS_SWING[2:0]	Output swing control on LS Serdes side. (Default 3'b101) Refer to Table 5-259.	RW
11	LS_LOS	LS Serdes LOS detector control 0 = Disable Loss of signal detection on LS serdes lane inputs 1 = Enable Loss of signal detection on LS serdes lane inputs (Default 1'b1)	RW

Table 5-258. LS_SERDES_CONTROL_2 (continued)

Device Address: 0x1E Register Address: 0x0007 Default: 0xDC04			
Bit	**Name**	**Description**	**Access**
10	LS_TX_ENRX	LS Serdes enable control on the transmit channel. LS Serdes per lane on transmitter channel is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 30.1.15 is set HIGH. Lanes 3 and 2 are automatically disabled when in 2ln 10G mode on transmit channel. Lanes 3, 2 and 1 are automatically disabled when in 1ln mode on transmit channel. 0 = Disables LS serdes lane 1 = Enables LS serdes lane (Default 1'b1)	RW
9:8	LS_TX_RATE [1:0]	LS Serdes lane rate settings on transmit channel 00 = Full rate (Default 2'b00) 01 = Half rate 10 = Quarter rate 11 = Reserved	RW
7:4	LS_DE[3:0]	LS Serdes De-emphasis settings. (Default 4'b0000) Refer to Table 5-260.	RW
3	RESERVED	For TI use only.	RW
2	LS_RX_ENTX	LS Serdes lane enable control on receive channel. LS Serdes per lane on receiver channel is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 30.1.15 is set HIGH. Lanes 3 and 2 are automatically disabled when in 2ln 10G mode on receive channel. Lanes 3, 2 and 1 are automatically disabled when in 1ln mode on receive channel. 0 = Disables LS serdes lane 1 = Enables LS serdes lane (Default 1'b1)	RW
1:0	LS_RX_RATE [1:0]	LS Serdes lane rate settings on receive channel 00 = Full rate (Default 2'b00) 01 = Half rate 10 = Quarter rate 11 = Reserved	RW

Table 5-259. LSRX Output AC Mode Output Swing Control

VALUE 30.7.14:12	AC MODE
	Typical Amplitude (mVdfpp)
000	190
001	380
010	560
011	710
100	850
101	950
110	1010
111	1050

Table 5-260. LSRX Output De-emphasis

30.7.7:4			30.7.7:4		
Value	**Amplitude reduction**		**Value**	**Amplitude reduction**	
	(%)	**dB**		**(%)**	**dB**
0000	0	0	1000	38.08	–4.16
0001	4.76	–0.42	1001	42.85	–4.86
0010	9.52	–0.87	1010	47.61	–5.61
0011	14.28	–1.34	1011	52.38	–6.44
0100	19.04	–1.83	1100	57.14	–7.35
0101	23.8	–2.36	1101	61.9	–8.38
0110	28.56	–2.92	1110	66.66	–9.54
0111	33.32	–3.52	1111	71.42	–10.87

Table 5-261. LSRX Output AC Mode Output Swing Control

Device Address: 0x1E Register Address: 0x0008 Default: 0x000D			
Bit	**Name**	**Description**	**Access**
15	LS_RX_INVPAIR	LS Serdes lane outputs polarity on the receive channel. (x = Channel A or B or C or D, y = Lane 0 or 1 or 2 or 3) 0 = Normal polarity. OUTxyP considered positive data. OUTxyN considered negative data (Default 1'b0) 1 = Inverted polarity. OUTxyP considered negative data. OUTxyN considered positive data	RW
14	LS_TX_INVPAIR	LS Serdes lane inputs polarity on the transmit channel. (x = Channel A or B or C or D, y = Lane 0 or 1 or 2 or 3) 0 = Normal polarity. INxyP considered positive data and INxyN considered negative data (Default 1'b0) 1 = Inverted polarity. INxyP considered negative data and INxyP considered positive data	RW
13:12	RESERVED	For TI use only (Default 2'b00)	RW
11:8	LS_EQ[3:0]	LS Serdes Equalization control (Default 4'b0000). Refer to Table 5-38.	RW
7:0	RESERVED	For TI use only (Default 8'b00001101)	RW

Table 5-262. LS_EQ Serdes Equalization

30.8.11:8			30.8.11:8		
Value	**Low Freq Gain**	**Zero Freq**	**Value**	**Low Freq Gain**	**Zero Freq**
0000	Maximum		1000	Adaptive	365 MHz
0001	Adaptive		1001		275 MHz
0010	Reserved		1010		195 MHz
0011			1011		140 MHz
0100			1100		105 MHz
0101			1101		75 MHz
0110			1110		55 MHz
0111			1111		50 MHz

Table 5-263. HS_OVERLAY_CONTROL

Device Address: 0x1E Register Address: 0x0009 Default: 0x0380			
Bit	**Name**	**Description**	**Access**
15:14	LS_OK_OUT_GATE[1:0]	LS_OK_OUT gating control X0 = Gating disabled (Default 2'b00) 01 = Gating enabled. LS_OK_OUT gated to LOW 11 = Gating enabled. LS_OK_OUT gated to HIGH	RW
13:12	LS_OK_IN_GATE[1:0]	LS_OK_IN gating control X0 = Gating disabled (Default 2'b00) 01 = Gating enabled. LS_OK_IN gated to LOW 11 = Gating enabled. LS_OK_IN gated to HIGH	RW
11:8	RESERVED	For TI use only. (Default 4'b0011)	RW
7	HS_LOS_MASK	0 = HS Serdes LOS status is used to generate HS channel synchronization status. If HS Serdes indicates LOS, channel synchronization indicates synchronization is not achieved 1 = HS Serdes LOS status is not used to generate HS channel synchronization status (Default 1'b1)	RW
5	HS_CH_SYNC_OVERLAY	0 = LOSx pin does not reflect receive channel loss of channel synchronization status (Default 1'b0) 1 = Allows channel loss of synchronization to be reflected on LOSx pin	RW
4	HS_INVALID_CODE_OVERLAY	0 = LOSx pin does not reflect receive channel invalid code word error (Default 1'b0) 1 = Allows invalid code word error to be reflected on LOSx pin	RW
3	HS_AGCLOCK_OVERLAY	0 = LOSx pin does not reflect HS Serdes AGC unlock status (Default 1'b0) 1 = Allows HS Serdes AGC unlock status to be reflected on LOSx pin	RW
2	HS_AZDONE_OVERLAY	0 = LOSx pin does not reflect HS Serdes auto zero calibration not done status (Default 1'b0) 1 = Allows auto zero calibration not done status to be reflected on LOSx pin	RW
1	HS_PLL_LOCK_OVERLAY	0 = LOSx pin does not reflect loss of HS Serdes PLL lock status (Default 1'b0) 1 = Allows HS Serdes loss of PLL lock status to be reflected on LOSx pin	RW
0	HS_LOS_OVERLAY	0 = LOSx pin does not reflect HS Serdes Loss of signal condition (Default 1'b0) 1 = Allows HS Serdes Loss of signal condition to be reflected on LOSx pin	RW

Table 5-264. LS_OVERLAY_CONTROL

Device Address: 0x1E Register Address: 0x000A Default: 0x4000			
Bit	**Name**	**Description**	**Access**
15:14	RESERVED	For TI use only. (Default 2'b01)	RW
13	10G_BER_TIMER_CLK_EN	0 = Disable BER timer clock in 10G mode (Default 1'b0) 1 = Enable BER timer clock See LAS BER procedure for more information.	RW
12	LS_PLL_LOCK_OVERLAY	0 = LOSx pin does not reflect loss of LS SERDES PLL lock status (Default 1'b0) 1 = Allows LS SERDES loss of PLL lock status to be reflected on LOSx pin	RW
11:8	LS_CH_SYNC_OVERLAY_LN[3:0]	[3] Corresponds to Lane 3, [2] Corresponds to Lane 2 [1] Corresponds to Lane 1, [0] Corresponds to Lane 0 0 = LOSx pin does not reflect LS Serdes lane loss of synchronization condition (Default 1'b0) 1 = Allows LS serdes lane loss of synchronization condition to be reflected on LOSx pin	RW
7:4	LS_INVALID_CODE_OVERLAY_LN[3:0]	[3] Corresponds to Lane 3, [2] Corresponds to Lane 2 [1] Corresponds to Lane 1, [0] Corresponds to Lane 0 0 = LOSx pin does not reflect LS Serdes lane invalid code condition (Default 1'b0) 1 = Allows LS serdes lane invalid code condition to be reflected on LOSx pin	RW
3:0	LS_LOS_OVERLAY_LN[3:0]	[3] Corresponds to Lane 3, [2] Corresponds to Lane 2 [1] Corresponds to Lane 1, [0] Corresponds to Lane 0 0 = LOSx pin does not reflect LS Serdes lane Loss of signal condition (Default 1'b0) 1 = Allows LS serdes lane Loss of signal condition to be reflected on LOSx pin	RW

Table 5-265. LOOPBACK_TP_CONTROL

Device Address: 0x1E Register Address: 0x000B Default: 0x0F30			
Bit	**Name**	**Description**	**Access**
15:14	RESERVED	For TI use only.	RW
13	HS_TP_GEN_EN	0 = Normal operation (Default 1'b0) 1 = Activates test pattern generation selected by bits 30.11.10:8	RW
12	HS_TP_VERIFY_EN	0 = Normal operation (Default 1'b0) 1 = Activates test pattern verification selected by bits 30.11.10:8	RW
11	LS_TEST_PATT_SEL[2]	See selection in 30.11.5:4	RW
10:8	HS_TEST_PATT_SEL[2:0]	Test Pattern Selection. Refer Test pattern procedures section for more information. 000 = High Frequency Test Pattern 001 = Low Frequency Test Pattern 010 = Mixed Frequency Test Pattern 011 = CRPAT Long 100 = CRPAT Short 101 = 2^7 - 1 PRBS pattern 110 = 2^{23} - 1 PRBS pattern 111 = 2^{31} - 1 PRBS pattern(Default 3'b111) Errors can be checked by reading HS_ERROR_COUNT register	RW
7	LS_TP_GEN_EN	0 = Normal operation (Default 1'b0) 1 = Activates test pattern generation selected by bits {30.11.11, 30.11.5:4} on the LS side	RW
6	LS_TP_VERIFY_EN	0 = Normal operation (Default 1'b0) 1 = Activates test pattern verification selected by bits {30.11.11, 30.11.5:4} on the LS side	RW
5:4	LS_TEST_PATT_SEL[1:0]	LS Test Pattern Selection LS_TEST_PATT_SEL[2:0]. Refer Test pattern procedures section for more information. LS_TEST_PATT_SEL[2] is 30.11.11 000 = High Frequency Test Pattern (Generation only) 001 = NA 010 = NA 011 = NA 100 = NA 101 = 27 - 1 PRBS pattern 110 = 2^{23} - 1 PRBS pattern 111 = 2^{31} - 1 PRBS pattern(Default 3'b111)	RW
3	DEEP_REMOTE_LPBK	0 = Normal functional mode (Default 1'b0) 1 = Enable deep remote loopback mode	RW
2	SHALLOW_REMOTE_LPBK	0 = Normal functional mode (Default 1'b0) 1 = Enable shallow remote loopback mode and serial retime mode	RW
1	DEEP_LOCAL_LPBK	0 = Normal functional mode (Default 1'b0) 1 = Enable deep local loopback mode	RW
0	SHALLOW_LOCAL_LPBK	0 = Normal functional mode (Default 1'b0) 1 = Enable shallow local loopback mode	RW

Table 5-266. LS_CONFIG_CONTROL

Device Address: 0x1E Register Address: 0x000C Default: 0x03F0			
Bit	**Name**	**Description**	**Access**
15	RESERVED	For TI use only. (Default 1'b0)	RW
14	RESERVED	For TI use only. (Default 1'b0)	RW
13:12	LS_STATUS_CFG[1:0]	Selects selected lane status to be reflected in LS_STATUS_1 register 0x15 00 = Lane 0 (Default 2'b00) 01 = Lane 1 10 = Lane 2 11 = Lane 3	RW
9:8	RESERVED	For TI use only. (Default 2'b11)	RW
7	LS_DECODE_ERR_MASK	0 = LS side decode errors of enabled lanes are used to generate link status if error rate exceeds threshold 1 = LS side decode errors of any lane is not used to generate link status (Default 1'b1)	RW
6	RESERVED	For TI use only. (Default 1'b1)	RW

Table 5-266. LS_CONFIG_CONTROL (continued)

Device Address: 0x1E Register Address: 0x000C Default: 0x03F0			
Bit	**Name**	**Description**	**Access**
5	LS_LOS_MASK	0 = LS Serdes LOS status of enabled lanes is used to generate link status 1 = LS Serdes LOS status of enabled lanes is not used to generate link status (Default 1'b1)	RW
4	LS_PLL_LOCK_MASK	0 = LS Serdes PLL Lock status is used to generate link status 1 = LS Serdes PLL Lock status is not used to generate link status (Default 1'b1)	RW
1	FORCE_LM_REALIGN	0 = Normal operation (Default 1'b0) 1 = Force lane realignment in Link status monitor	RW/SC
0	LAS_BER_THRESH	Threshold setting for 8b/10b error rate checking . See LAS BER procedure for more information. 0 = Link Ok if 1 error when timer in 30.13.15:0 expires (Default 1'b0) 1 = Link Ok if 15 error when timer in 30.13.15:0 expires	RW

Table 5-267. LAS_BER_TIMER_CONTROL

Device Address: 0x1E Register Address: 0x000D Default: 0xFFFF			
Bit	**Name**	**Description**	**Access**
15:0	LAS_BER_TIMER[15:0]	16 msb of a 32-bit counter whose 16 lsb are fixed to 16'hFFFF. This counter's clock is reference clock divided by 64 and is used in link status monitor for BER calculation (Default 16'hFFFF). See LAS BER procedure for more information.	RW

Table 5-268. RESET_CONTROL

Device Address: 0x1E Register Address: 0x000E Default: 0x0000			
Bit	**Name**	**Description**	**Access**
3	DATAPATH_RESET	Channel datapath reset control. Required once the desired functional mode is configured. 0 = Normal operation. (Default 1'b0) 1 = Resets channel logic excluding MDIO registers. (Resets both Tx and Rx datapath)	RW SC(1)
2	TXFIFO_RESET	Transmit FIFO reset control. 0 = Normal operation. (Default 1'b0) 1 = Resets transmit datapath FIFO.	
1	RXFIFO_RESET	Receive FIFO reset control. 0 = Normal operation. (Default 1'b0) 1 = Resets receive datapath FIFO.	

(1) After reset bit is set to one, it automatically sets itself back to zero on the next MDC clock cycle.

Table 5-269. CHANNEL_STATUS_1

Device Address: 0x1E Register Address: 0x000F Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15	HS_TP_STATUS	Test Pattern status for High/Low/Mixed/CRPAT test patterns. 1 = Alignment has achieved and correct pattern has been received. Any bit errors are reflected in HS_ERROR_COUNTER register (0x10) 0 = Alignment has not been determined	RO
14	RESERVED	For TI use only.	RO
13	HS_LOS	Loss of Signal Indicator. When high, indicates that a loss of signal condition is detected on HS serial receive inputs	RO/LH
12	HS_AZ_DONE	Auto zero complete indicator. When high, indicates auto zero calibration is complete	RO/LL
11	HS_AGC_LOCKED	Adaptive gain control loop lock indicator. When high, indicates AGC loop is in locked state	
10	HS_CHANNEL_SYNC	Channel synchronization status indicator. When high, indicates channel synchronization has achieved	

Table 5-269. CHANNEL_STATUS_1 (continued)

Device Address: 0x1E Register Address: 0x000F Default: 0x0000			
Bit	**Name**	**Description**	**Access**
9	RESERVED	For TI use only	RO/LH
8	HS_DECODE_INVALID	Valid when decoder is enabled and during CRPAT test pattern verification. When high, indicates decoder received an invalid code word, or a 8b/10b disparity error. In functional mode, number of DECODE_INVALID errors are reflected in HS_ERROR_COUNTER register (0x10)	
7	TX_FIFO_UNDERFLOW	When high, indicates underflow has occurred in the transmit datapath FIFO.	
6	TX_FIFO_OVERFLOW	When high, indicates overflow has occurred in the transmit datapath FIFO.	
5	RX_FIFO_UNDERFLOW	When high, indicates underflow has occurred in the receive datapath FIFO.	
4	RX_FIFO_OVERFLOW	When high, indicates overflow has occurred in the receive datapath FIFO.	
3	RX_LS_OK	Receive link status indicator from system side. When high, indicates receive link status is achieved on the system side	RO/LL
2	TX_LS_OK	Link status indicator from Lane alignment/Link training slave inside TLK10034 When high, indicates 10G Link align achieved sync and alignment	
1	LS_PLL_LOCK	LS Serdes PLL lock indicator When high, indicates LS Serdes PLL achieved lock to the selected incoming REFCLK0/1_P/N	
0	HS_PLL_LOCK	HS Serdes PLL lock indicator When high, indicates HS Serdes PLL achieved lock to the selected incoming REFCLK0/1_P/N	

Table 5-270. HS_ERROR_COUNTER

Device Address: 0x1E Register Address: 0x0010 Default: 0xFFFD			
Bit	**Name**	**Description**	**Access**
15:0	HS_ERR_COUNT[15:0]	In functional mode, this counter reflects number of invalid code words (includes disparity errors) received by decoder. In HS test pattern verification mode , this counter reflects error count for the test pattern selected through 30.11.10:8 When PRBS_EN pin is set, this counter reflects error count for selected PRBS pattern. Counter value cleared to 16'h0000 when read.	COR

Table 5-271. LS_LN0_ERROR_COUNTER

Device Address: 0x1E Register Address: 0x0011 Default: 0xFFFD			
Bit	**Name**	**Description**	**Access**
15:0	LS_LN0_ERR_COUNT[15:0]	Lane 0 Error counter In functional mode, this counter reflects number of invalid code words (includes disparity errors) received by decoder in lane alignment slave. In LS test pattern verification mode , this counter reflects error count for the test pattern selected through 30.11.5:4 Counter value cleared to 16'h0000 when read.	COR

Table 5-272. LS_LN1_ERROR_COUNTER

Device Address: 0x1E Register Address: 0x0012 Default: 0xFFFD			
Bit	**Name**	**Description**	**Access**
15:0	LS_LN1_ERR_COUNT[15:0]	Lane 1 Error counter In functional mode, this counter reflects number of invalid code words (includes disparity errors) received by decoder in lane alignment slave. In LS test pattern verification mode , this counter reflects error count for the test pattern selected through 30.11.5:4 Counter value cleared to 16'h0000 when read.	COR

Table 5-273. LS_LN2_ERROR_COUNTER

Device Address: 0x1E Register Address: 0x0013 Default: 0xFFFD			
Bit	**Name**	**Description**	**Access**
15:0	LS_LN2_ERR_COUNT[15:0]	Lane 2 Error counter In functional mode, this counter reflects number of invalid code words (includes disparity errors) received by decoder in lane alignment slave. In LS test pattern verification mode , this counter reflects error count for the test pattern selected through 30.11.5:4 Counter value cleared to 16'h0000 when read.	COR

Table 5-274. LS_LN3_ERROR_COUNTER

Device Address: 0x1E Register Address: 0x0014 Default: 0xFFFD			
Bit	**Name**	**Description**	**Access**
15:0	LS_LN3_ERR_COUNT[15:0]	Lane 3 Error counter In functional mode, this counter reflects number of invalid code words (includes disparity errors) received by decoder in lane alignment slave. n LS test pattern verification mode , this counter reflects error count for the test pattern selected through 30.11.5:4 Counter value cleared to 16'h0000 when read.	COR

Table 5-275. LS_STATUS_1

Device Address: 01E Register Address: 0x0015 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
14:11	RESERVED	For TI use only.	RO
10	LS_LOS	Loss of Signal Indicator. When high, indicates that a loss of signal condition is detected on LS serial receive inputs for selected lane. Lane can be selected through LS_STATUS_CFG[1:0] (Register 30.12)	RO/LH
9	LS_LN_ALIGN_FIFO_ERR	LS Lane alignment FIFO error status 1 = Lane alignment FIFO on LS side has error 0 = Lane alignment FIFO on LS side has no error	RO/LH
8	LS_CH_SYNC_STATUS	LS Channel sync status for selected lane. Lane can be selected through LS_STATUS_CFG[1:0] (Register 30.12)	RO/LL
6:4	RESERVED	For TI use only.	RO
3	LS_INVALID_DECODE	LS Invalid decode error for selected lane. Lane can be selected through LS_STATUS_CFG[1:0] (Register 30.12). Error count for each lane can also be monitored through respective LS_LNx_ERR_COUNT registers	RO/LH
2:0	RESERVED	For TI use only.	RO

Table 5-276. TI_RESERVED_CONTROL

Device Address: 0x01 Register Address: 0x0016 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
11:8	RESERVED	For TI use only. (Default 4'b0000)	RW
6:0	RESERVED	For TI use only. (Default 7'b0000000)	

Table 5-277. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address: 0x0017 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	RESERVED	For TI use only.	RW

Table 5-278. LATENCY_STATUS_CLEAR_CONTROL

Device Address: 0x01 Register Address: 0x0018 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	LATENCY_CLEAR	Reading this register will clear Latency stopwatch status specified in LATENCY_COUNTER_1 and LATENCY_COUNTER_2 registers. Below sequence of reads needs to be performed for accurate and repeat stopwatch measurements. See Latency measurement procedure more information. READ 0x8041 READ 0x8042 READ 0x0018	RO

Table 5-279. LS_CLKOUT_CONTROL (1)

Device Address: 0x1E Register Address: 0x0019 Default: 0x0808			
Bit	**Name**	**Description**	**Access**
15:12	LS1_CLKOUT_DIV[3:0]	LS1_CLKOUT Output clock divide setting. This value is used to divide selected clock (Selected using LS1_CLKOUT_SEL) before giving it out onto LS1_CLKOUTP/N. 0000 = Divide by 1 (Default 4'b0000) 0001 = RESERVED 0010 = RESERVED 0011 = RESERVED 0100 = Divide by 2 0101 = RESERVED 0110 = RESERVED 0111 = RESERVED 1000 = Divide by 4 1001 = Divide by 8 1010 = Divide by 16 1011 = RESERVED 1100 = Divide by 5 1101 = Divide by 10 1110 = Divide by 20 1111 = Divide by 25 RW	
11	LS1_CLKOUT_ EN	Output clock enable. 0 = Holds LS1_CLKOUTP/N output to a fixed value. 1 = Allows LS1_CLKOUTP/N output to toggle normally. (Default 1'b1)	
10:8	LS1_CLKOUT_SEL[2:0]	Output clock select. Selected LS TXBCLK/RXBCLK sent out on LS1_CLKOUTP/N pins 000 = Selects Ch A LSRXBCLK0 clock as output clock (Default 3'b000) 001 = Selects Ch B LSRXBCLK0 clock as output clock 010 = Selects Ch C LSRXBCLK0 clock as output clock 011 = Selects Ch D LSRXBCLK0 clock as output clock 100 = Selects Ch A LSTXBCLK clock as output clock 101 = Selects Ch B LSTXBCLK clock as output clock 110 = Selects Ch C LSTXBCLK clock as output clock 111 = Selects Ch D LSTXBCLK clock as output clock	
7:4	LS0_CLKOUT_DIV[3:0]	LS0_CLKOUT Output clock divide setting. This value is used to divide selected clock (Selected using LS0_CLKOUT_SEL) before giving it out onto LS0_CLKOUTP/N. 0000 = Divide by 1 (Default 4'b0000) 0001 = RESERVED 0010 = RESERVED 0011 = RESERVED 0100 = Divide by 2 0101 = RESERVED 0110 = RESERVED 0111 = RESERVED 1000 = Divide by 4 1001 = Divide by 8 1010 = Divide by 16 1011 = RESERVED 1100 = Divide by 5 1101 = Divide by 10 1110 = Divide by 20 1111 = Divide by 25	

(1) This register is channel independent.

Table 5-279. LS_CLKOUT_CONTROL[1] (continued)

Device Address: 0x1E Register Address: 0x0019 Default: 0x0808			
Bit	**Name**	**Description**	**Access**
3	LS0_CLKOUT_ EN	Output clock enable. 0 = Holds LS0_CLKOUTP/N output to a fixed value. 1 = Allows LS0_CLKOUTP/N output to toggle normally. (Default 1'b1)	
2:0	LS0_CLKOUT_SEL[2:0]	Output clock select. Selected LS TXBCLK/RXBCLK sent out on LS0_CLKOUTP/N pins 000 = Selects Ch A LSRXBCLK0 clock as output clock (Default 3'b000) 001 = Selects Ch B LSRXBCLK0 clock as output clock 010 = Selects Ch C LSRXBCLK0 clock as output clock 011 = Selects Ch D LSRXBCLK0 clock as output clock 100 = Selects Ch A LSTXBCLK clock as output clock 101 = Selects Ch B LSTXBCLK clock as output clock 110 = Selects Ch C LSTXBCLK clock as output clock 111 = Selects Ch D LSTXBCLK clock as output clock	

Table 5-280. HS_TX_CLKOUT_CONTROL[1]

Device Address: 0x1E Register Address: 0x001A Default: 0x0C0C			
Bit	**Name**	**Description**	**Access**
15:12	HSTX1_CLKOUT_DIV[3:0]	HSTX1_CLKOUT Output clock divide setting. This value is used to divide selected clock (Selected using HSTX1_CLKOUT_SEL) before giving it out onto HSTX1_CLKOUTP/N. 0000 = Divide by 1 (Default 4'b0000) 0001 = RESERVED 0010 = RESERVED 0011 = RESERVED 0100 = Divide by 2 0101 = RESERVED 0110 = RESERVED 0111 = RESERVED 1000 = Divide by 4 1001 = Divide by 8 1010 = Divide by 16 1011 = RESERVED 1100 = Divide by 5 1101 = Divide by 10 1110 = Divide by 20 1111 = Divide by 25	RW
11	HSTX1_CLKOUT_ EN	Output clock enable. 0 = Holds HSTX1_CLKOUTP/N output to a fixed value. 1 = Allows HSTX1_CLKOUTP/N output to toggle normally. (Default 1'b1)	RW
10	HSTX1_CLKOUT_POWERDOWN	0 = Normal operation 1 = Enable HSTX1_CLKOUTP/N Power Down (Default 1'b1)	RW
9:8	HSTX1_CLKOUT_SEL[1:0]	Output clock select. Selected HS TXBCLK sent out on HSTX1_ CLKOUTP/N pins 00 = Selects Channel A HSTXBCLK clock as output clock (Default 2'b00) 01 = Selects Channel B HSTXBCLK clock as output clock 10 = Selects Channel C HSTXBCLK clock as output clock 11 = Selects Channel D HSTXBCLK clock as output clock	RW

(1) This register is channel independent

Table 5-280. HS_TX_CLKOUT_CONTROL[(1)] (continued)

Device Address: 0x1E Register Address: 0x001A Default: 0x0C0C			
Bit	**Name**	**Description**	**Access**
7:4	HSTX0_CLKOUT_DIV[3:0]	HSTX0_CLKOUT Output clock divide setting. This value is used to divide selected clock (Selected using HSTX0_CLKOUT_SEL) before giving it out onto HSTX0_CLKOUTP/N. 0000 = Divide by 1 (Default 4'b0000) 0001 = RESERVED 0010 = RESERVED 0011 = RESERVED 0100 = Divide by 2 0101 = RESERVED 0110 = RESERVED 0111 = RESERVED 1000 = Divide by 4 1001 = Divide by 8 1010 = Divide by 16 1011 = RESERVED 1100 = Divide by 5 1101 = Divide by 10 1110 = Divide by 20 1111 = Divide by 25	RW
3	HSTX0_CLKOUT_ EN	Output clock enable. 0 = Holds HSTX0_CLKOUTP/N output to a fixed value. 1 = Allows HSTX0_CLKOUTP/N output to toggle normally. (Default 1'b1)	RW
2	HSTX0_CLKOUT_POWERDOWN	0 = Normal operation 1 = Enable HSTX0_CLKOUTP/N Power Down(Default 1'b1)	RW
1:0	HSTX0_CLKOUT_SEL[1:0]	Output clock select. Selected HS TXBCLK sent out on HSTX0_ CLKOUTP/N pins 00 = Selects Channel A HSTXBCLK clock as output clock (Default 2'b00) 01 = Selects Channel B HSTXBCLK clock as output clock 10 = Selects Channel C HSTXBCLK clock as output clock 11 = Selects Channel D HSTXBCLK clock as output clock	RW

Table 5-281. LS_CLKOUT_PWRDWN_CONTROL

Device Address: 0x1E Register Address: 0x001B Default: 0x0063			
Bit	**Name**	**Description**	**Access**
6:2	RESERVED	For TI use only (Default 5'b11000)	RW
1	LS1_CLKOUT_POWERDOWN	0 = Normal operation 1 = Enable LS1_CLKOUTP/N Power Down (Default 1'b1)	
0	LS0_CLKOUT_POWERDOWN	0 = Normal operation (Default 1'b1) 1 = Enable LS0_CLKOUTP/N Power Down (Default 1'b1)	

Table 5-282. LS_CH_CONTROL_1

Device Address: 0x1E Register Address: 0x001C Default: 0x0000			
Bit	**Name**	**Description**	**Access**
6	RESERVED	For TI use only (Default 1'b0)	RW/SC
5:2	RESERVED	For TI use only (Default 4'b0000)	RW
1:0	LS_CH_SYNC_HYS_SEL[1:0]	LS Channel synchronization hysteresis selection for selected lane. Lane can be selected in LS_SERDES_CONTROL_1. 00 = The channel synchronization, when in the synchronization state, performs the Ethernet standard specified hysteresis to return to the LOS state (Default 2'b00) 01 = A single 8b/10b invalid decode error or disparity error causes the channel synchronization state machine to immediately transition from sync to LOS 10 = Two adjacent 8b/10b invalid decode errors or disparity errors cause the channel synchronization state machine to immediately transition from sync to LOS 11 = Three adjacent 8b/10b invalid decode errors or disparity errors cause the channel synchronization state machine to immediately transition from sync to LOS	

Table 5-283. HS_CH_CONTROL_1

Device Address: 0x1E Register Address: 0x001D Default: 0x0000			
Bit	**Name**	**Description**	**Access**
6	RESERVED	For TI use only (Default 1'b0)	RW/SC
5	RESERVED	For TI use only (Default 4'b0000)	RW
3	HS_ENC_BYPASS	0 = Normal operation. 1 = Disables 8B/10B encoder on HS side. Required for 1:1 operation	RW
2	HS_DEC_BYPASS	0 = Normal operation. 1 = Disables 8B/10B decoder on HS side. Required for 1:1 operation	RW
1:0	HS_CH_SYNC_ HYSTERESIS[1:0]	Channel synchronization hysteresis control on the HS receive channel. 00 = The channel synchronization, when in the synchronization state, performs the Ethernet standard specified hysteresis to return to the unsynchronized state (Default 2'b00) 01 = A single 8b/10b invalid decode error or disparity error causes the channel synchronization state machine to immediately transition from sync to unsync 10 = Two adjacent 8b/10b invalid decode errors or disparity errors cause the channel synchronization state machine to immediately transition from sync to unsync 11 = Three adjacent 8b/10b invalid decode errors or disparity errors cause the channel synchronization state machine to immediately transition from sync to unsync	RW

Table 5-284. EXT_ADDRESS_CONTROL

Device Address: 0x1E Register Address: 0x001E Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	EXT_ADDR_CONTROL[15:0]	Applicable in Clause 22 mode only. This register should be written with the extended register address to be written/read. Contents of address written in this register can be accessed from Reg 31 (0x001F). (Default 16'h0000)	RW

Table 5-285. EXT_ADDRESS_DATA

Device Address: 0x1E Register Address: 0x001F Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	EXT_ADDR_DATA[15:0]	Applicable in Clause 22 mode only. This register contains the data associated with the register address written in Register 30 (0x001E)	RW

Table 5-286. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address: 0x8000 Default: 0x04D1			
Bit	**Name**	**Description**	**Access**
11:4	RESERVED	For TI use only (Default 8'b01001101)	RW
0		For TI use only (Default 1'b1)	

Table 5-287. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address: 0x8001 Default: 0x0107			
Bit	**Name**	**Description**	**Access**
9:0	RESERVED	For TI use only (Default 10'h107)	RW

Table 5-288. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address: 0x8002 Default: 0x01FE			
Bit	**Name**	**Description**	**Access**
9:0	RESERVED	For TI use only (Default 10'h1FE)	RW

Table 5-289. VS_10G_LN_ALIGN_CODE_P

Device Address: 0x1E Register Address: 0x8003 Default: 0x01BC			
Bit	**Name**	**Description**	**Access**
9:0	LN_ALIGN_CODE_P[9:0]	10-bit alignment code to be matched for positive disparity	RW

Table 5-290. VS_10G_LN_ALIGN_CODE_N

Device Address: 0x1E Register Address: 0x8004 Default: 0x01BC			
Bit	**Name**	**Description**	**Access**
9:0	LN_ALIGN_CODE_N[9:0]	10-bit alignment code to be matched for negative disparity	RW

Table 5-291. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address: 0x8005 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
14:12	RESERVED	For TI use only (Default 3'b000)	RW
9:0	RESERVED	For TI use only (Default 10'h000)	

Table 5-292. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address: 0x8006 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:12	RESERVED	For TI use only (Default 4'b0000)	RW
9:0	RESERVED	For TI use only (Default 10'h000)	

Table 5-293. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address: 0x8007 Default: 0x8000			
Bit	**Name**	**Description**	**Access**
15:12	RESERVED	For TI use only (Default 4'b1000)	RW
9:0	RESERVED	For TI use only (Default 10'h000)	

Table 5-294. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address: 0x8008 Default: 0x0000			
Bit30.32776.15	**Name**	**Description**	**Access**
	RESERVED	For TI use only (Default 1'b0)	RW/SC
14:12	RESERVED	For TI use only (Default 3'b000)	RW
9:0	RESERVED	For TI use only (Default 10'h000)	

Table 5-295. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address: 0x8009 Default: 0x5500			
Bit	**Name**	**Description**	**Access**
14:8	RESERVED	For TI use only (Default 7'h55)	RW
1:0	RESERVED	For TI use only (Default 2'b00)	

Table 5-296. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address: 0x800A Default: 0x5500			
Bit	**Name**	**Description**	**Access**
14:8	RESERVED	For TI use only (Default 7'h55)	RW
1:0	RESERVED	For TI use only (Default 2'b00)	

Table 5-297. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address: 0x800B Default: 0x013C			
Bit	**Name**	**Description**	**Access**
9:0	RESERVED	For TI use only (Default 10'h13C)	RW

Table 5-298. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address: 0x800C Default: 0x01BC			
Bit	**Name**	**Description**	**Access**
9:0	RESERVED	For TI use only (Default 10'h1BC)	RW

Table 5-299. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address: 0x800D Default: 0x01FC			
Bit	**Name**	**Description**	**Access**
9:0	RESERVED	For TI use only (Default 10'h1FC)	RW

Table 5-300. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address: 0x800E Default: 0x013C			
Bit	**Name**	**Description**	**Access**
9:0	RESERVED	For TI use only (Default 10'h13C)	RW

Table 5-301. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address: 0x800F Default: 0x01BC			
Bit	**Name**	**Description**	**Access**
9:0	RESERVED	For TI use only (Default 10'h1BC)	RW

Table 5-302. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address: 0x8010 Default: 0x01FC			
Bit	**Name**	**Description**	**Access**
9:0	RESERVED	For TI use only (Default 10'h1FC)	RW

Table 5-303. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address: 0x8011 Default: 0x7F00			
Bit	**Name**	**Description**	**Access**
15:8	RESERVED	For TI use only. (Default 8'b0111_1111)	RW

Table 5-304. TI_RESERVED_STATUS

Device Address: 0x1E Register Address: 0x8012 Default: 0xFFFD			
Bit	**Name**	**Description**	**Access**
15:0	RESERVED	For TI use only.	COR

Table 5-305. TI_RESERVED_STATUS

Device Address: 0x1E Register Address: 0x8013 Default: 0xFFFD			
Bit	**Name**	**Description**	**Access**
15:0	RESERVED	For TI use only.	COR

Table 5-306. TI_RESERVED_STATUS

Device Address: 0x1E Register Address: 0x8014 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
11	RESERVED	For TI use only	RO/LH
8	RESERVED	For TI use only	
4:0	RESERVED	For TI use only	

Table 5-307. TI_RESERVED_STATUS

Device Address: 0x1E Register Address: 0x8015 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	RESERVED	For TI use only	RO

Table 5-308. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address: 0x8020 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	RESERVED	For TI use only (Default 16'h0000)	RW

Table 5-309. AUTO_CLKOUT_CONTROL

Device Address: 0x1E Register Address: 0x8021 Default: 0x000F			
Bit	**Name**	**Description**	**Access**
7	RESERVED	For TI use only (Default 1'b0)	RW
6	RESERVED	For TI use only (Default 1'b0) Must be set to 1.	RW
5	RESERVED	For TI use only (Default 1'b0) Must be set to 1.	RW
4	RESERVED	For TI use only (Default 1'b0)	RW
3	RX_CLKOUT_EN_AUTO_ DISABLE	This bit controls the signal which flat lines RX CLKOUT 1 = RX CLKOUT clock flat lined if HS PLL lock is lost or if HS LOS is detected (Default 1'b1) 0 = RX CLKOUT clock not flat lined if HS PLL lock is lost or if HS LOS is detected Must be set to 1.	RW
2	RX_CLKOUT_PWRDWN_ AUTO_DISABLE	This bit controls the signal which power down RX CLKOUT output buffer 1 = RX CLKOUT output buffer powered down if HS PLL lock is lost or if HS LOS is detected (Default 1'b1) 0 = RX CLKOUT output buffer not powered down if HS PLL lock is lost or if HS LOS is detected Must be set to 1.	RW
1	RESERVED	For TI use only (Default 1'b1) Must be set to 1.	RW
0	RESERVED	For TI use only (Default 1'b1) Must be set to 1.	RW

Table 5-310. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address: 0x8022 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	RESERVED	For TI use only (Default 16'h0000)	RW

Table 5-311. TI_RESERVED_STATUS

Device Address: 0x1E Register Address: 0x8030 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
13:0	RESERVED	For TI use only.	RO

Table 5-312. TI_RESERVED_STATUS

Device Address: 0x1E Register Address: 0x8031 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	RESERVED	For TI use only	RO

Table 5-313. TI_RESERVED_STATUS

Device Address: 0x1E Register Address: 0x8032 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
11:0	RESERVED	For TI use only	RO

Table 5-314. TI_RESERVED_STATUS

Device Address: 0x1E Register Address: 0x8033 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
11:8	RESERVED	For TI use only	RO
6:0	RESERVED	For TI use only	

Table 5-315. TI_RESERVED_STATUS

Device Address: 0x1E Register Address: 0x8034 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
9:8	RESERVED	For TI use only	RO
5:0	RESERVED	For TI use only	

Table 5-316. TI_RESERVED_STATUS

Device Address: 0x1E Register Address: 0x8035 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
5:0	RESERVED	For TI use only	

Table 5-317. LATENCY_MEASURE_CONTROL (1)

Device Address: 0x1E Register Address: 0x8040 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
7:6	LATENCY_MEAS_START_SEL[1:0]	Latency measurement start point selection 00 = Selects LS RX as start point (Default 2 ’b00) 01 = Selects HS TX as start point 1x = Selects external pin (PRTAD1) rising edge as start point	RW
5:4	LATENCY_MEAS_CLK_DIV[1:0]	Latency measurement clock divide control. Valid only when bit 30.32832.2 is 0. Divides clock to needed resolution. Higher the divide value, lesser the latency measurement resolution. Divider value should be chosen such that the divided clock doesn’t result in clock slower than the high speed byte clock. 00 = Divide by 1 (Default 2’b00) (Most Accurate Measurement) 01 = Divide by 2 10 = Divide by 4 11 = Divide by 8 (Longest Measurement Capability)	RW
3:2	LATENCY_MEAS_STOP_SEL[1:0]	Latency measurement stop point selection 00 = Selects LS TX as stop point (Default 2’b00) 01 = Selects HS RX as stop point 1x = Selects external pin (PRTAD1) falling edge as stop point	RW
1	LATENCY_MEAS_EN	Latency measurement enable 0 = Disable Latency measurement (Default ’b0) 1 = Enable Latency measurement	RW

(1) See Latency measurement procedure for more information

Table 5-317. LATENCY_MEASURE_CONTROL[1] (continued)

Device Address: 0x1E Register Address: 0x8040 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
0	LATENCY_MEAS_CLK_SEL	Latency measurement clock selection. 0 = Selects VCO clock as per Latency measurement table. Bits 30.32832.5:4 can be used to divide this clock to achieve needed resolution. (Default 1'b0) 1 = Selects respective channel recovered byte clock (Frequency = Serial bit rate/ 20).	RW

Table 5-318. LATENCY_COUNTER_2

Device Address: 0x1E Register Address: 0x8041 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:12	LATENCY_MEAS_START_ COMMA[3:0]	Latency measurement start comma location status. "1" indicates start comma location found. If LS TX is selected as start point (30.32832.7 = 0), [3:0] indicates status for lane3, lane2, lane1, lane0. If HS RX is selected as start point (30.32832.7 = 1), [0] indicates status for data[9:0], [1] indicates status for data[19:10]. [3:2] is unused.	RO/LH (1)
11:8	LATENCY_MEAS_STOP_ COMMA[3:0]	Latency measurement stop comma location status. "1" indicates stop comma location found. If LS RX is selected as stop point (30.32832.6 = 0), [3:0] indicates status for lane3, lane2, lane1, lane0. If HS TX is selected as stop point (30.32832.6 = 1), [0] indicates status for data[9:0], [1] indicates status for data[19:10]. [3:2] is unused.	
4	LATENCY_ MEAS_READY	Latency measurement ready indicator 0 = Indicates latency measurement not complete. 1 = Indicates latency measurement is complete and value in latency measurement counter (LATENCY_MEAS_COUNT[19:0]) is ready to be read.	
3:0	LATENCY_MEAS_ COUNT[19:16]	Bits[19:16] of 20 bit wide latency measurement counter. Latency measurement counter value represents the latency in number of clock cycles. Each clock cycle is half of the period of the measurement clock as determined by register 30.32832.5:4 and 30.32832.0. This counter will return 20'h00000 if it's read before rx comma is received. If latency is more than 20'hFFFFF clock cycles then this counter returns 20'hFFFFF.	COR (1)

(1) Latency measurement counter value resets to 20'h00000 when Register 30.24 (0x0018) is read. Start and Stop Comma (30.32833.15:12 & 30.32833.11:8) and count valid (30.32833.4) bits are also cleared when Register30.24 is read.

Table 5-319. LATENCY_COUNTER_1

Device Address: 0x1E Register Address: 0x8042 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
15:0	LATENCY_MEAS_ COUNT[15:0]	Bits[15:0] of 20 bit wide latency measurement counter. Below sequence of reads needs to be performed for accurate and repeat stopwatch measurements. READ 0x8041 READ 0x8042 READ 0x0018	COR (1)

(1) Latency measurement counter value resets to 20'h00000 when Register 30.24 (0x0018) is read. Start and Stop Comma (30.32833.15:12 & 30.32833.11:8) and count valid (30.32833.4) bits are also cleared when Register30.24 is read.

Table 5-320. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address: 0x8050 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
3:0	RESERVED	For TI use only (Default 4'b0000)	RW

Table 5-321. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address: 0x8100 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
10:0	RESERVED	For TI use only (Default 11'b000000000000)	RW

Table 5-322. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address: 0x8101 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
10:0	RESERVED	For TI use only (Default 11'b000000000000)	RW

The registers below can be accessed directly through Clause 45 and indirectly through Clause 22. Contains device specific debug control/status registers and not implemented per channel basis (i.e. same physical register accessed irrespective of channel addressed).

Table 5-323. TI_RESERVED_CONTROL

Device Address: 0x1E Register Address: 0x9000 Default: 0x0000			
Bit	**Name**	**Description**	**Access**
11:8	RESERVED	For TI use only. (Default 4'b0000)	RW
5:4	RESERVED	For TI use only. (Default 2'b00)	
0	RESERVED	For TI use only. (Default 1'b0)	

6 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

Each channel of the TLK10034 can be used to convert between XAUI (on the low speed port) and 10GBASE-R signaling (on the high speed port). The high speed side of the device meets the requirements of the 10GBASE-KR physical layer standard for 10 Gbps data transmission over a PCB backplane. The device can also be used for optical physical layers (like 10GBASE-SR or 10GBASE-LR) by interfacing to optical modules requiring SFI or XFI electrical signaling. For optical use cases, KR-specific features like Clause 73 auto-negotiation and link training should be disabled.

6.2 Typical Application

A typical application for TLK10034 is to support 10 Gbps Ethernet data transmission over a backplane, e.g., between a network processor or MAC and switch ASIC located on separate cards within a router chassis. A block diagram of this application is shown below.

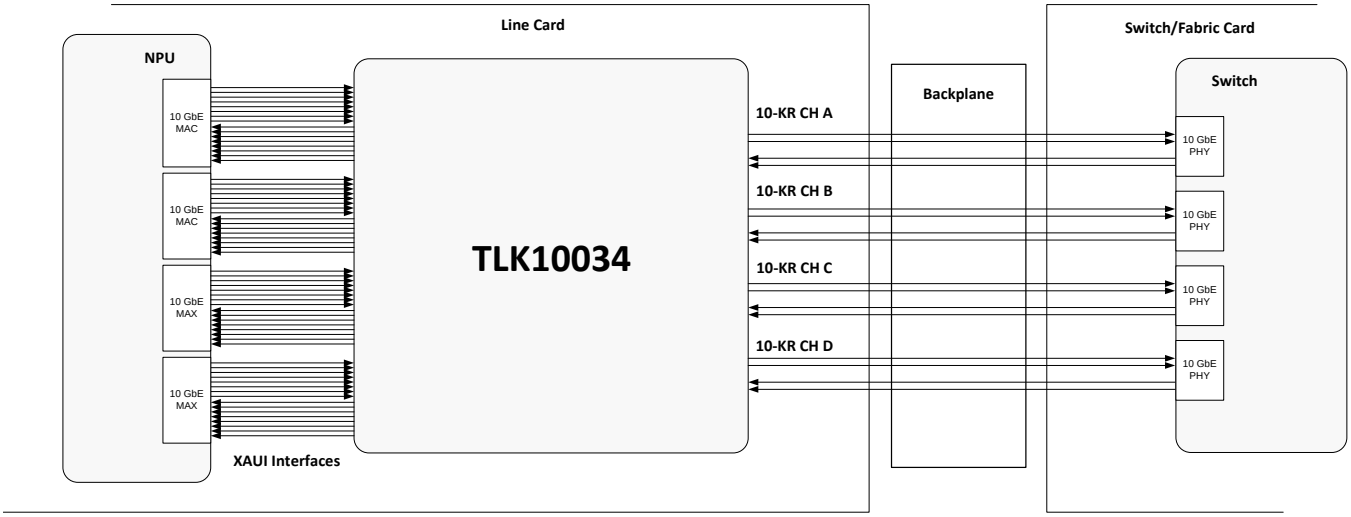


Figure 6-1. Typical Application Circuit

6.2.1 Design Requirements

Table 6-1 lists the design requirements for this typical application example.

Table 6-1. Design Parameters

PARAMETER	VALUE
10GBASE-KR Interface Requirements	
Signaling rate	10.3125 Gbps, ±100ppm
Differential peak-to-peak output voltage (maximum)	1200 mV
Total jitter (maximum)	0.28 UI
Encoding	64b/66b
Scrambling	Yes

Table 6-1. Design Parameters (continued)

PARAMETER	VALUE
Auto-negotiation?	Yes
Link training	Yes
XAUI Interface Requirements	
Signaling rate per lane	3.125 Gbps ±100 ppm
Differential peak-to-peak output voltage (maximum)	1600 mV
Total jitter (maximum)	0.35 UI
Encoding	8b/10b

6.2.2 Detailed Design Procedure

The TLK10034 should be powered via a 1-V (nominal) supply on the VDDD, VDDA, DVDD, VDDT, and VPP rails and by a 1.5-V or 1.8-V (nominal) supply on the VDDR and VDDO rails. The power supply accuracy should be 5% or better, and the user should be careful that resistive losses across the application PCB's power distribution network do not cause the voltage present at the TLK10034's BGA balls to be below specification. If a switched-mode power supply is used, care should be taken to ensure low supply ripple.

A differential reference clock must be provided to either the REFCLK0P/N or REFCLK1P/N input port. The clock signal should be AC-coupled and have a differential amplitude between 250 mV and 2000 mV peak-to-peak. For 10GBASE-R applications, the clock frequency should be either 156.25 MHz or 312.5 MHz and have an accuracy of 100 ppm. Because jitter on the reference clock can transfer through the TLK10034's PLLs and onto the serial outputs, it is best to keep the reference clock's jitter as low as possible (e.g., under 1 ps from 10 kHz to 20 MHz) in order to meet the requirements of IEEE 802.3.

All serial inputs and outputs should be laid out on the PCB following best practices for high speed signal integrity. Detailed layout recommendations are given in the Section 6.2.4.1 section.

6.2.3 Application Curve

The output eye diagram of the TLK10034 (operated at 10.3125 Gbps under nominal conditions) is shown below.

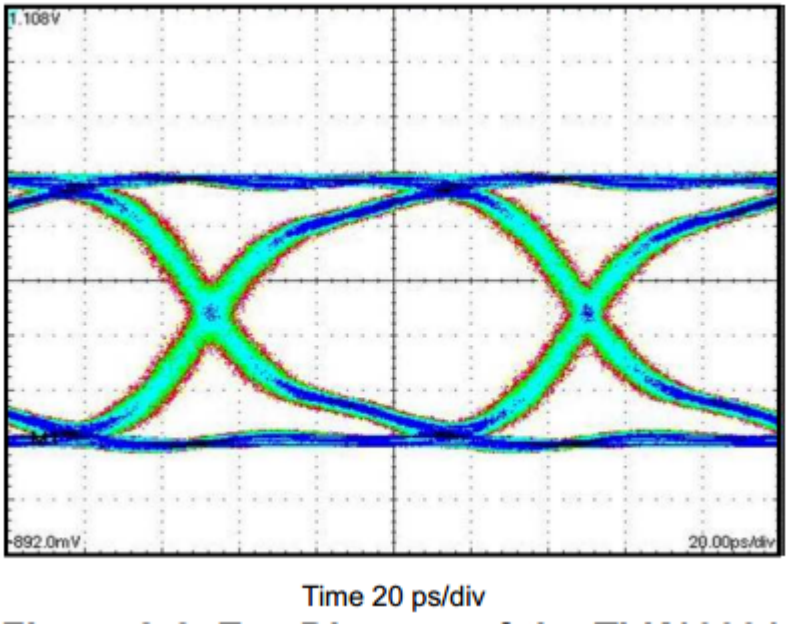


Figure 6-2. Eye Diagram of the TLK10034

6.2.4 Layout

6.2.4.1 Layout Guidelines

6.2.4.1.1 TLK10034 High-Speed Data Path

Both “low-speed” side and “high-speed” side serial signals are referred to as “high-speed” signals for the purpose of this document as they support very high data rates. For that reason care must be taken to realize them on a printed circuit board with signal integrity in mind. The high-speed data path CML input pins INA[3:0]P/INA[3:0]N, INB[3:0]P/INB[3:0]N, HSRXAP/HSRXAN, and HSRXBP/HSRXBN, and the CML output pins OUTA[3:0]P/OUTA[3:0]N, OUTB[3:0]P/OUTB[3:0]N, HSTXAP/HSTXAN, and HSTXBP/HSTXBN, have to be connected with loosely-coupled 100-Ω differential transmission lines. Differential intra-pair skew needs to be minimized to within ±1 mil. Inter-pair (lane-to-lane) skew for the low-speed signals can be as high as 30 UI. An example of FR-4 printed circuit board (PCB) realization of such differential transmission lines in microstrip format is shown in Figure 6-8.

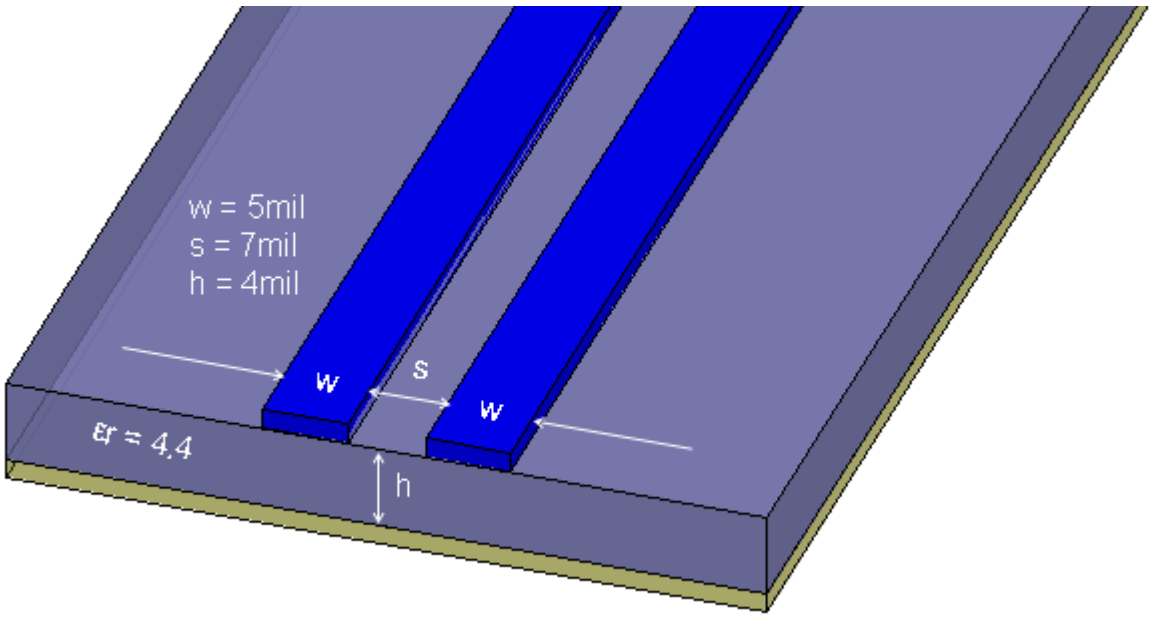


Figure 6-3. Differential Microstrip PCB Trace Geometry Example

To avoid impedance discontinuities the high-speed serial signals should be routed on a PCB on either the top or bottom PCB layers in microstrip format with no VIAS. If VIAS are unavoidable, an absolute minimum number of vias need to be used. The VIAS should be made to stretch through the entire PCB thickness (as shown in Figure 12-2) to connect microstrip traces on the top and bottom layers of the PCB so as to leave no via stubs that can severely impact the performance. If stripline traces are absolutely necessary, and if via back-drilling is not possible, then the routing layers should be chosen so as to have via stubs that are shorter than 10 mils.

All unused internal layer via pads on high-speed signal VIAS should be removed to further improve impedance matching. On the high-speed side, the HSRXAP/HSRXAN and HSRXBP/HSRXBN signals are more sensitive to impedance discontinuities introduced by VIAS than HSTXAP/HSTXAN and HSTXBP/HSTXBN signals. For that reason, if only some of those signals need to be routed with VIAS, then the latter should be routed with VIAS and the former with no VIAS.

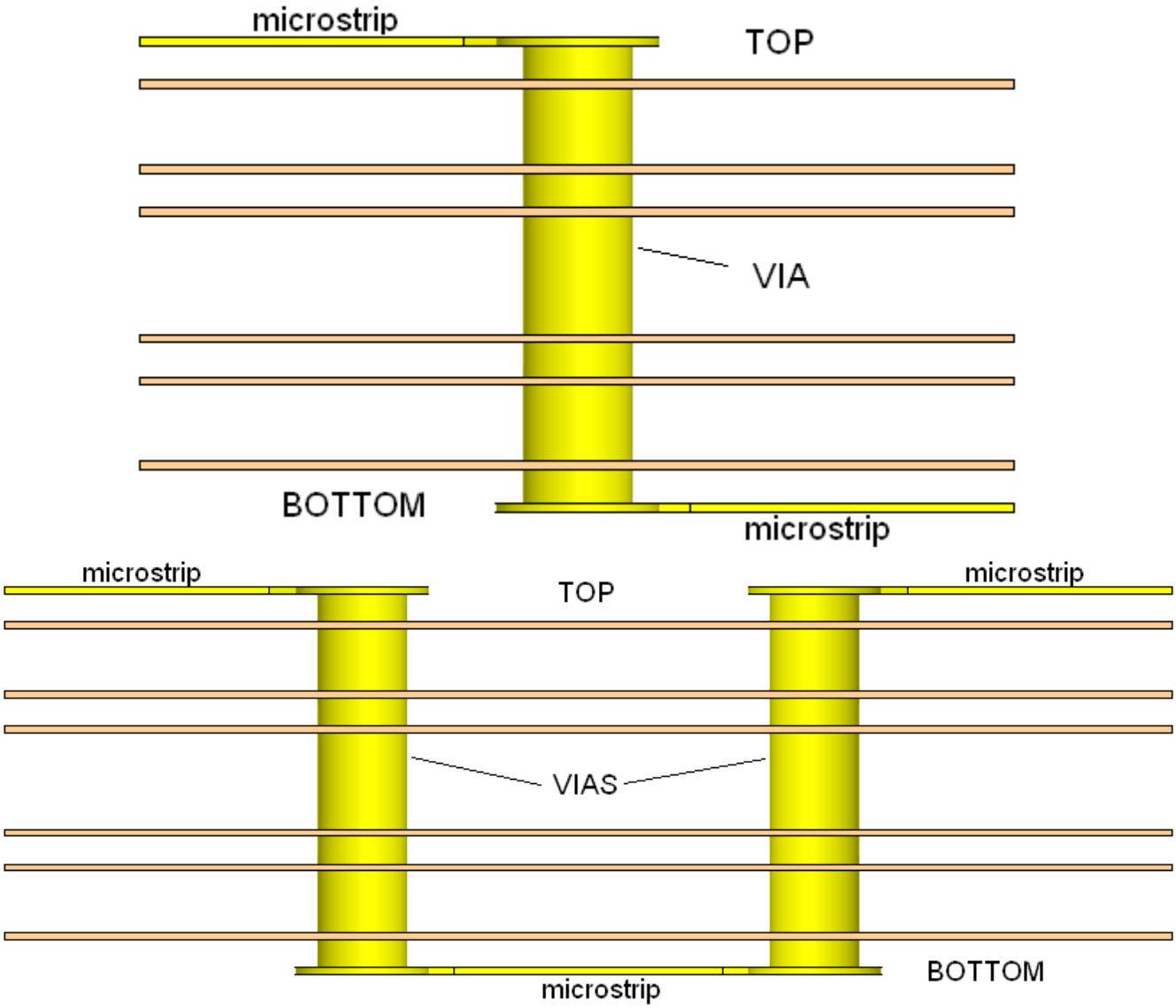


Figure 6-4. Examples of High-Speed PCB Traces with VIAS that Have No Via Stubs and No Via Pads on Internal Layers

To further improve on impedance matching, differential vias with neighboring ground vias can be used as shown in Figure 6-5. The optimum dimensions of such a differential via structure depend on various parameters such as the trace geometry, dielectric material, as well as the PCB layer stack-up. A 3D electromagnetic field solver can be used to find the optimum via dimensions.

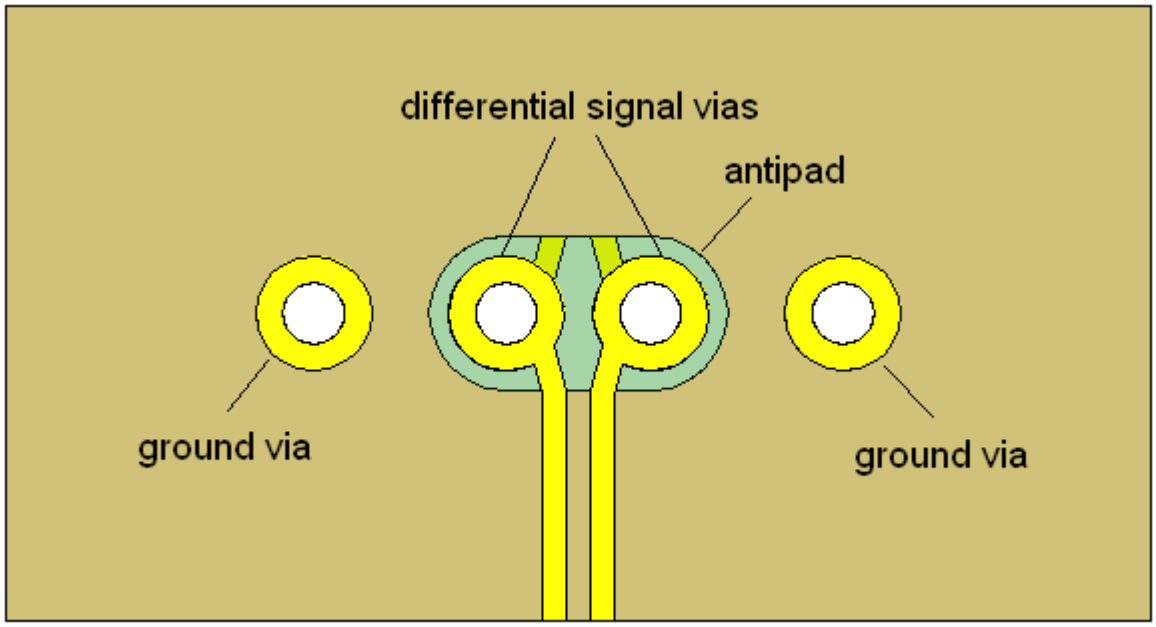


Figure 6-5. A Differential PCB via Structure (Top View)

PCB traces connected to the HSRXAP/HSRXAN and HSRXBP/HSRXBN pins should have differential insertion loss of less than 25 dB at 5 GHz.

Surface-mount connector pads such as those used with the SFP/SFP+ module connectors are wider and hence have characteristic impedance that is lower than the regular high-speed PCB traces. If the pads are more than 2 times wider than the PCB traces, the pads' impedance needs to be increased to minimize impedance discontinuities. The easy way of increasing the pads' impedance is to cut out the reference plane immediately under those pads as shown in Figure 6-6 so as to have the pads refer to a reference plane on lower layers while maintaining 100Ω differential characteristic impedance.

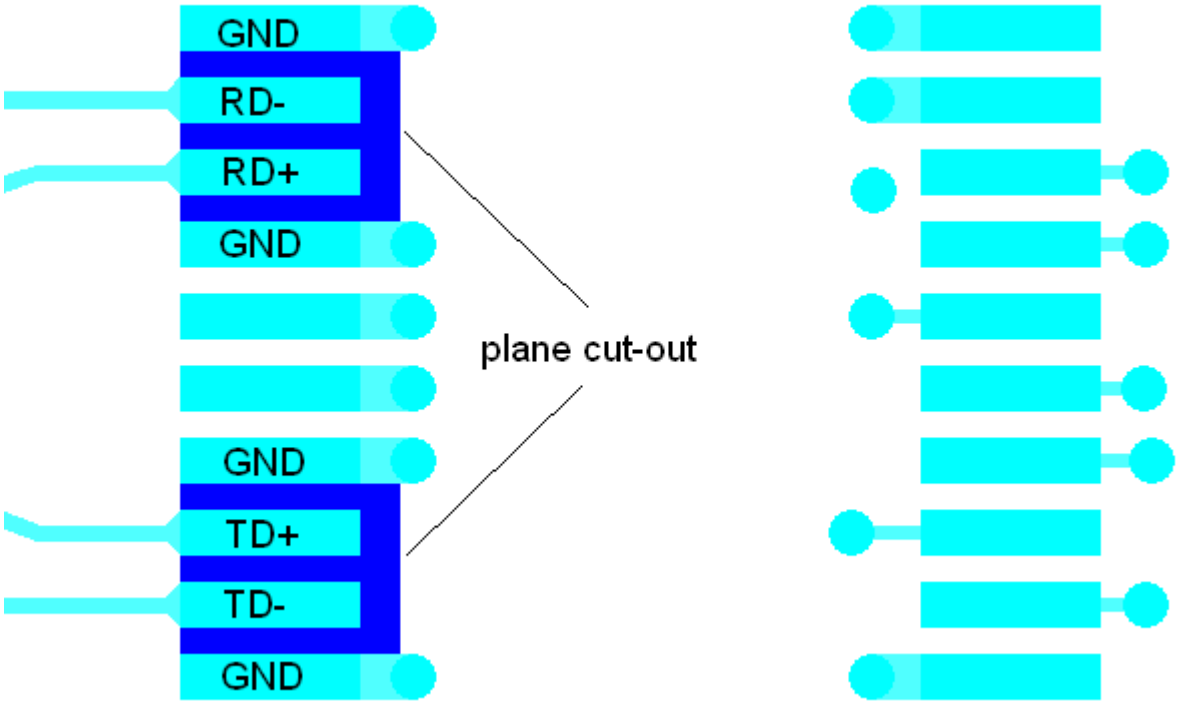


Figure 6-6. Reference Plane Cut-Out Under SFP/SFP+ Module Connector Pads

6.2.4.1.2 AC-Coupling

A 0.1-uF series AC-coupling capacitor should be connected to each of the high-speed data path pins INA[3:0]P/INA[3:0]N, INB[3:0]P/INB[3:0]N, HSRXAP/HSRXAN, HSRXBP/HSRXBN, OUTA[3:0]P/OUTA[3:0]N, OUTB[3:0]P/OUTB[3:0]N, HSTXAP/HSTXAN, and HSTXBP/HSTXBN. If the TLK10034 high-speed side data path pins are connected to SFP/SFP+ optical modules with internal AC-coupling capacitors, then no external capacitors should be used. Adding additional series capacitors may severely impact the performance.

To avoid impedance discontinuities, it is strongly recommended where possible to make the transmission line trace width closely match the AC-coupling capacitor pad size. Smaller capacitor packages such as 0201 make it easy to meet that condition.

6.2.4.1.3 External Clock Connections

An external clock jitter cleaner, such as Texas Instruments CDCE72010 or CDCM7005, may be used when needed to provide a low jitter reference clock. An example external clock jitter cleaner connection for channel A is shown in Figure 6-7.

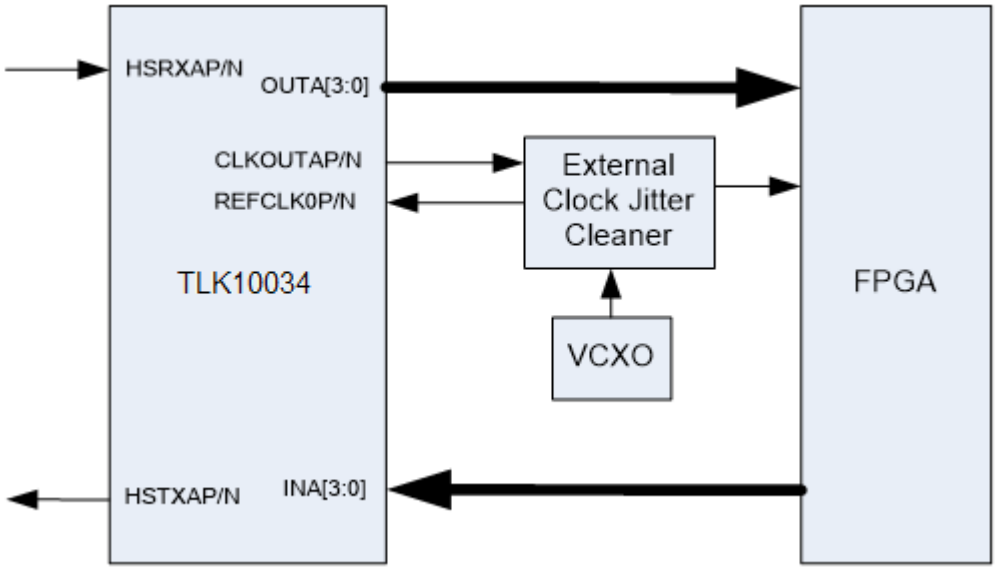


Figure 6-7. External Clock Jitter Cleaner Connection Example for Channel A

6.2.4.2 Layout Example

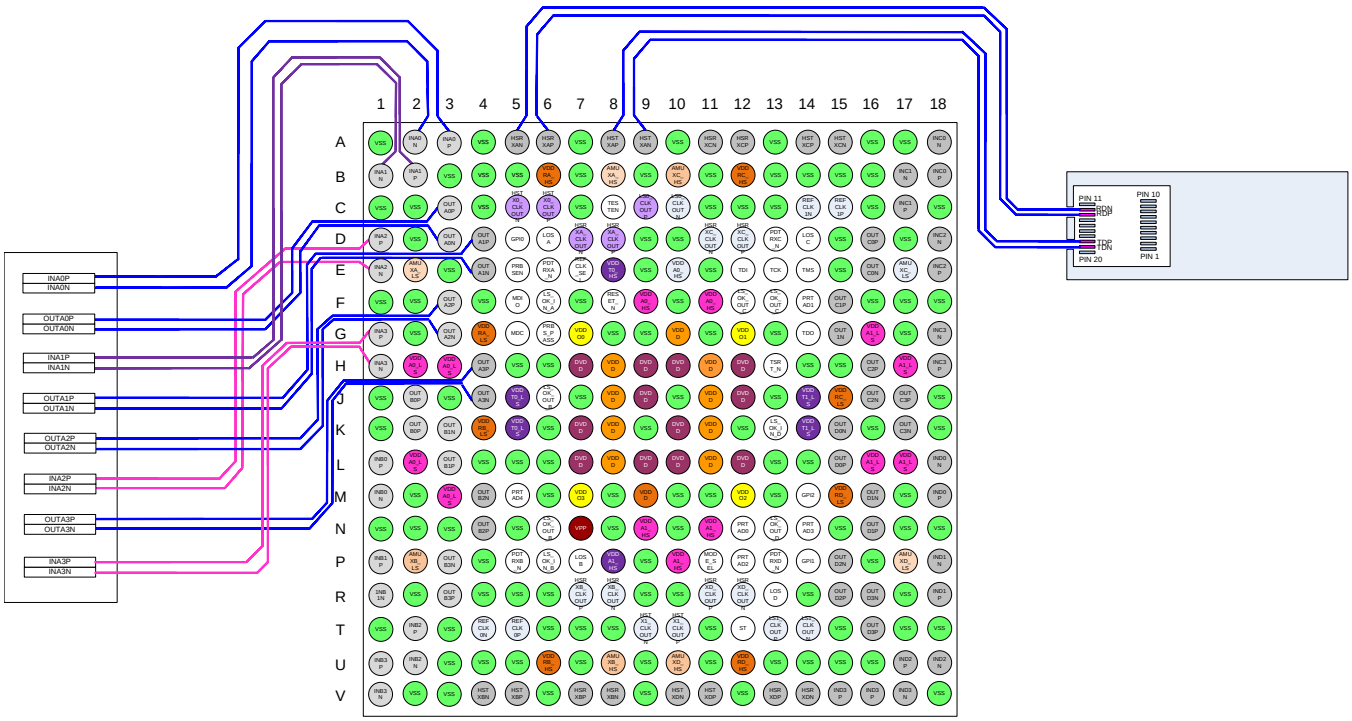


Figure 6-8. TLK10034 Pinout and Routing

6.2.4.3 Package Thermal Dissipation Ratings

Table 6-2 details the thermal characteristics of the TLK10034 package.

Table 6-2. Package Thermal Characteristics

JEDEC STANDARD BOARD		
PARAMETER		VALUE
Θ_{JA}	Theta-JA	21.2°C/W
Ψ_{JT}	Psi-JT	0.10°C/W
Ψ_{JB}	Psi-JB	7.7°C/W
CUSTOM TYPICAL APPLICATION BOARD(1)		
Θ_{JA}	Theta-JA	11.2°C/W
Ψ_{JT}	Psi-JT	0.10°C/W
Ψ_{JB}	Psi-JB	5.53°C/W

(1) Custom Typical Application Board Characteristics:
- 10x15 inches
- 12 layer
  - 8 power/ground layers – 95% copper (1oz)
  - 4 signal layers – 20% copper (1oz)

$\Psi_{JB} = (T_J - T_B)/(\text{Total Device Power Dissipation})$
T_J = Device Junction Temperature
T_B = Temperature of PCB 1 mm from device edge.
$\Psi_{JT} = (T_J - T_C)/(\text{Total Device Power Dissipation})$
T_J = Device Junction Temperature
T_C = Hottest temperature on the case of the package.

6.3 Power Supply Recommendations

The TLK10034 allows either the core or I/O power supply to be powered up for an indefinite period of time while the other supply is not powered up, if all of the following conditions are met:

1. All maximum ratings and recommending operating conditions are followed.
2. Bus contention while 1.5/1.8V power is applied (>0V) must be limited to 100 hours over the projected lifetime of the device.
3. Junction temperature is less than 105°C during device operation

NOTE

Voltage stress up to the absolute maximum voltage values for up to 100 hours of lifetime operation at a TJ of 105°C or lower will minimally impact reliability.

The TLK10034 inputs are not failsafe (i.e. cannot be driven with the I/O power disabled). TLK10034 inputs should not be driven high until their associated power supply is active.

7 Device and Documentation Support

7.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

7.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

7.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

7.4 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLK10034AAJ	ACTIVE	FCBGA	AAJ	324	84	Green (RoHS & no Sb/Br)	SNAGCU	Level-4-260C-72 HR	-40 to 85	TLK10034	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

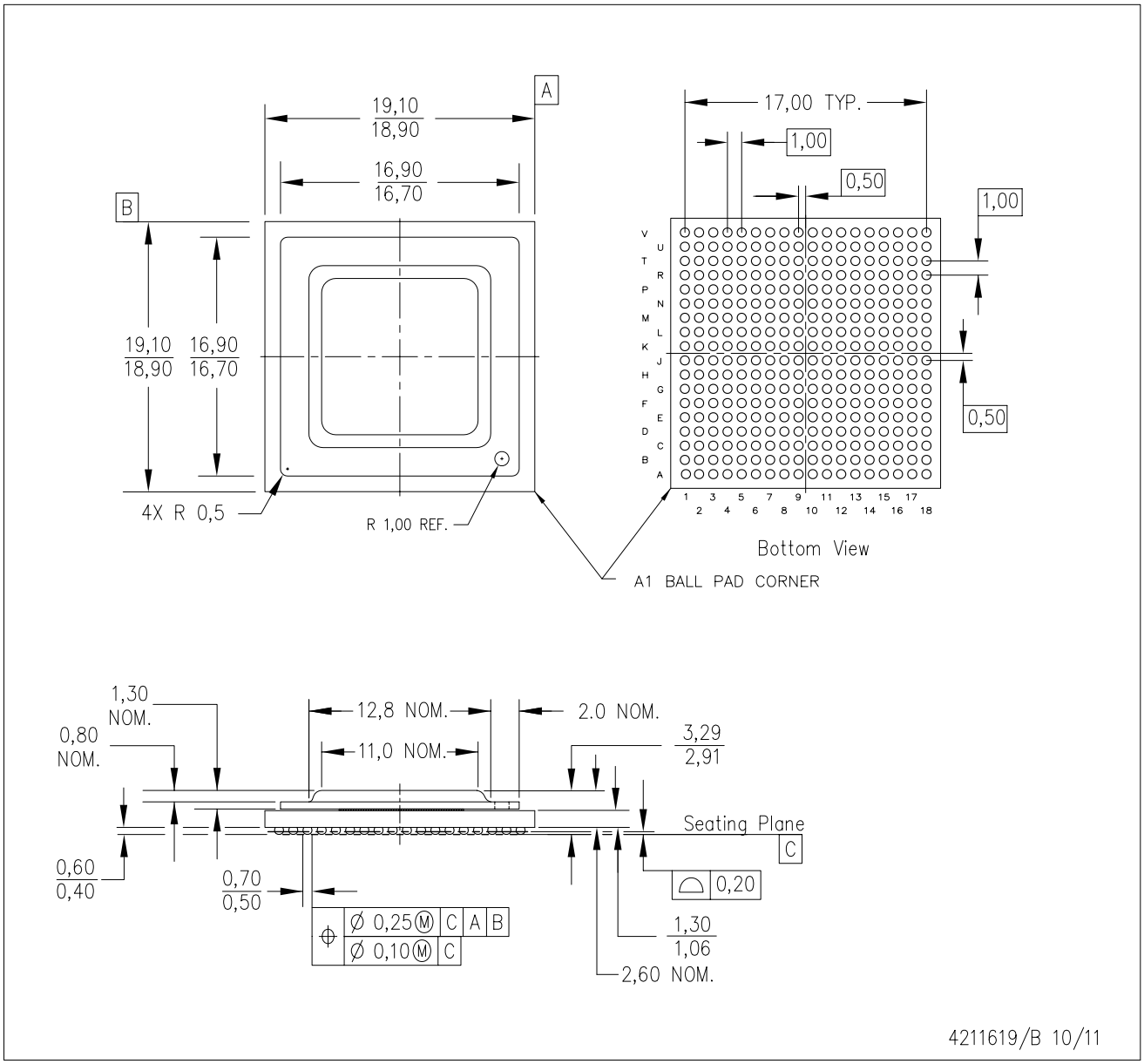
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

AAJ (S–PBGA–N324) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Flip chip application only.
D. Pb–free die bump and solder ball.

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