Unitrode Products from Texas Instruments

application INFO available

UC1525B UC1527B
UC2525B UC2527B
UC3525B UC3527B

Regulating Pulse Width Modulators

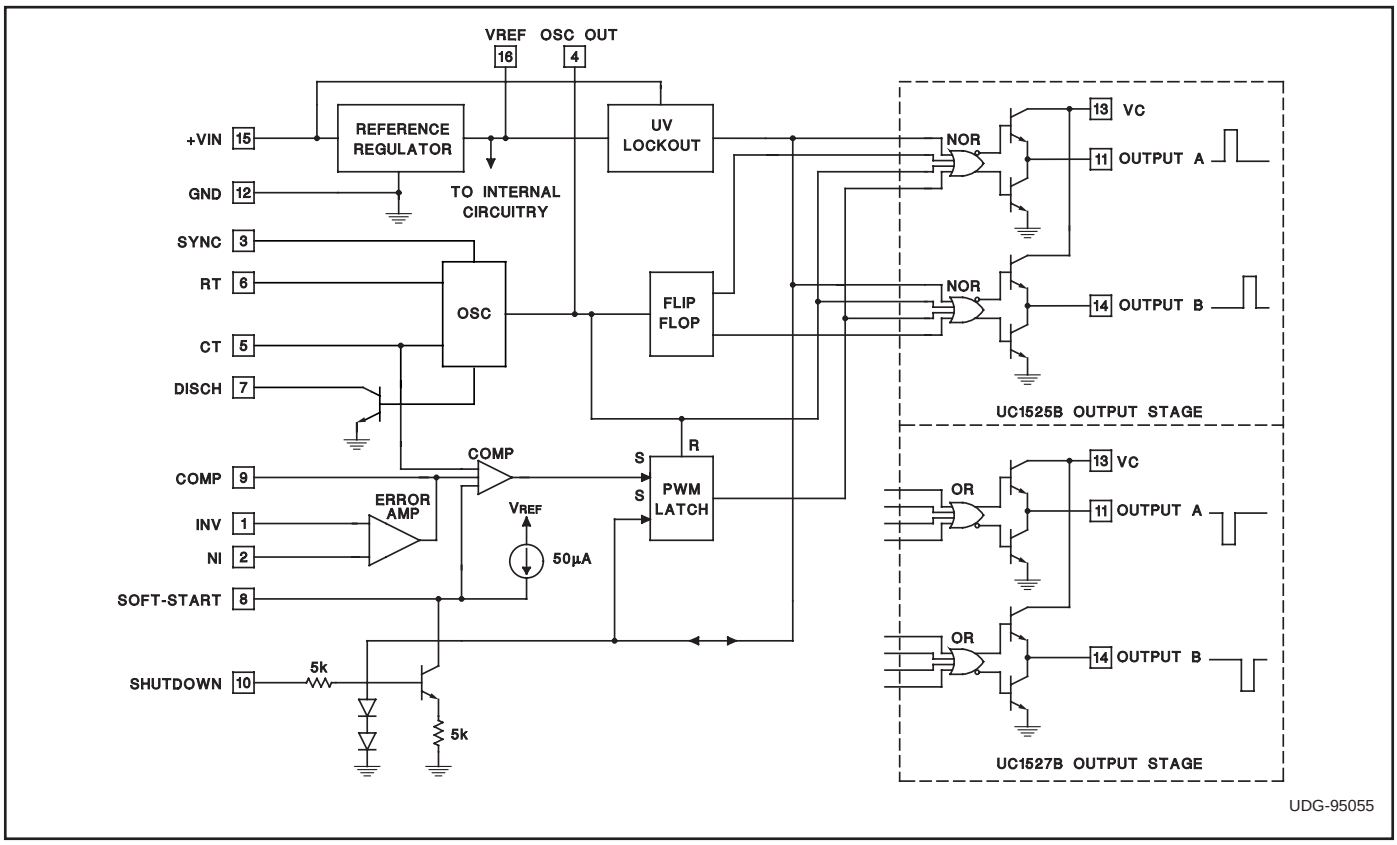
FEATURES

- 8 to 35V Operation
- 5.1V Buried Zener Reference Trimmed to ±0.75%
- 100Hz to 500kHz Oscillator Range
- Separate Oscillator Sync Terminal
- Adjustable Deadtime Control
- Internal Soft-Start
- Pulse-by-Pulse Shutdown
- Input Undervoltage Lockout with Hysteresis
- Latching PWM to Prevent Multiple Pulses
- Dual Source/Sink Output Drivers
- Low Cross Conduction Output Stage
- Tighter Reference Specifications

DESCRIPTION

The UC1525B/1527B series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip +5.1V buried zener reference is trimmed to ±0.75% and the input common-mode range of the error amplifier includes the reference voltage, eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between the CT and the discharge terminals provide a wide range of dead time adjustment. These devices also feature built-in soft-start circuitry with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for sub-normal input voltages. This lockout circuitry includes approximately 500mV of hysteresis for jitter-free operation. Another feature of these PWM circuits is a latch following the comparator. Once a PWM pulse has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200mA. The UC1525B output stage features NOR logic, giving a LOW output for an OFF state. The UC1527B utilizes OR logic which results in a HIGH output level when OFF.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, (+VIN) . . . . . +40V
Collector Supply Voltage (VC) . . . . . +40V
Logic Inputs . . . . . –0.3V to +5.5V
Analog Inputs . . . . . –0.3V to VIN
Output Current, Source or Sink 500mA
Reference Output Current 50mA
Oscillator Charging Current 5mA
Power Dissipation at T_A = +25°C 1000mW
Power Dissipation at T_C = +25°C 2000mW
Operating Junction Temperature . . . . . –55°C to +150°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

All currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

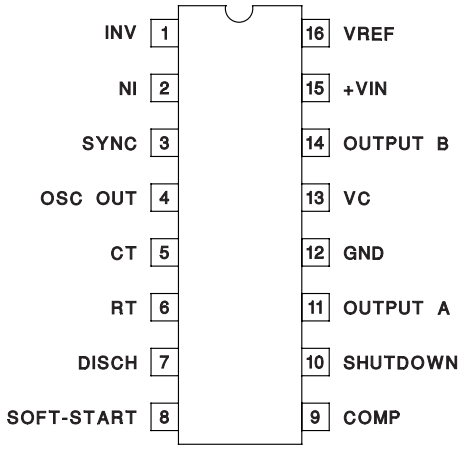
RECOMMENDED OPERATING CONDITIONS (Note 1)

Input Voltage (+VIN) . . . . . +8V to +35V
Collector Supply Voltage (VC) . . . . . +4.5V to +35V
Sink/Source Load Current (steady state) . . . . . 0 to 100mA
Sink/Source Load Current (peak) . . . . . 0 to 400mA
Reference Load Current . . . . . 0 to 20mA
Oscillator Frequency Range . . . . . 100Hz to 400kHz
Oscillator Timing Resistor . . . . . 2kΩ to 150kΩ
Oscillator Timing Capacitor . . . . . 0.001μF to 0.1μF
Dead Time Resistor Range . . . . . 0Ω to 500Ω

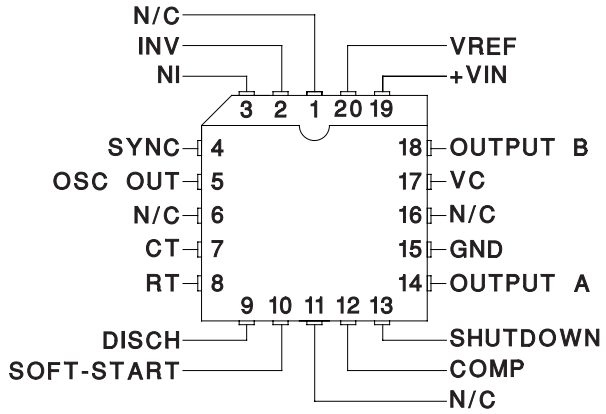
Note 1: Range over which the device is functional and parameter limits are guaranteed.

CONNECTION DIAGRAMS

DIL-16, SOIC-16 (Top View)
J or N, DW Packages



LCC-20, PLCC-20 (Top View)
L, Q Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1525B and UC1527B; –40°C to +85°C for the UC2525B and UC2527B; 0°C to +70°C for the UC3525B and UC3527B; +VIN = 20V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1525B/UC2525B UC1527B/UC2527B			UC3525B UC3527B			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	T_J = 25°C	5.062	5.10	5.138	5.036	5.10	5.164	V
Line Regulation	VIN = 8V to 35V		5	10		5	10	mV
Load Regulation	I_L = 0mA to 20mA		7	15		7	15	mV
Temperature Stability (Note 2)	Over Operating Range		10	50		10	50	mV
Total Output Variation	Line, Load, and Temperature	5.036		5.164	5.024		5.176	V
Short Circuit Current	VREF = 0, T_J =25°C		80	100		80	100	mA
Output Noise Voltage (Note 2)	10Hz ≤ f ≤10kHz, T_J = 25°C		40	200		40	200	μVrms
Long Term Stability (Note 2)	T_J = 125°C, 1000 Hrs.		3	10		3	10	mV

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PARAMETER	TEST CONDITIONS	UC1525B/UC2525B UC1527B/UC2527B			UC3525B UC3527B			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator Section (Note 3)								
Initial Accuracy (Notes 2 & 3)	T_J = 25°C		±2	±6		±2	±6	%
Voltage Stability (Notes 2 & 3)	VIN = 8V to 35V		±0.3	±1		±1	±2	%
Temperature Stability (Note 2)	Over Operating Range		±3	±6		±3	±6	%
Minimum Frequency	RT = 200kΩ, CT = 0.1µF			120			120	Hz
Maximum Frequency	RT = 2kΩ, CT = 470pF	400			400			kHz
Current Mirror	I_{RT} = 2mA	1.7	2.0	2.2	1.7	2.0	2.2	mA
Clock Amplitude (Notes 2 & 3)		3.0	3.5		3.0	3.5		V
Clock Width (Notes 2 & 3)	T_J = 25°C	0.3	0.5	1.0	0.3	0.5	1.0	µs
Sync Threshold		1.2	2.0	2.8	1.2	2.0	2.8	V
Sync Input Current	Sync Voltage = 3.5V		1.0	2.5		1.0	2.5	mA
Error Amplifier Section (VCM = 5.1V)								
Input Offset Voltage			0.5	5		2	10	mV
Input Bias Current			1	10		1	10	µA
Input Offset Current				1			1	µA
DC Open Loop Gain	RL ≥ 10 MegΩ	60	75		60	75		dB
Gain-Bandwidth Product (Note 2)	A_V = 0dB, T_J = 25°C	1	2		1	2		MHz
Output Low Level			0.2	0.5		0.2	0.5	V
Output HIgh Level		3.8	5.6		3.8	5.6		V
Common Mode Rejection	V_{CM} = 1.5V to 5.2V	60	75		60	75		dB
Supply Voltage Rejection	VIN = 8V to 35V	50	60		50	60		dB
PWM Comparator								
Minimum Duty Cycle				0			0	%
Maximum Duty Cycle (Note 3)		45	49		45	49		%
Input Threshold (Note 3)	Zero Duty Cycle	0.7	0.9		0.7	0.9		V
Input Threshold (Note 3)	Maximum Duty Cycle		3.3	3.6		3.3	3.6	V
Input Bias Current (Note 2)			0.05	1.0		0.05	1.0	µA
Shutdown Section								
Soft Start Current	$V_{SHUTDOWN}$ = 0V, $V_{SOFTSTART}$ = 0V	25	50	80	25	50	80	µA
Soft Start Low Level	$V_{SHUTDOWN}$ = 2.5V		0.4	0.7		0.4	0.7	V
Shutdown Threshold	To outputs, $V_{SOFTSTART}$ = 5.1V, T_J =25°C	0.6	0.8	1.0	0.6	0.8	1.0	V
Shutdown Input Current	$V_{SHUTDOWN}$ = 2.5V		0.4	1.0		0.4	1.0	mA
Shutdown Delay (Note 2)	$V_{SHUTDOWN}$ = 2.5V, T_J = 25°C		0.2	0.5		0.2	0.5	µs
Output Drivers (Each Output) (Vc = 20V)								
Output Low Level	I_{SINK} = 20mA		0.2	0.4		0.2	0.4	V
	I_{SINK} = 100mA		1.0	2.0		1.0	2.0	V
Output HIgh Level	I_{SOURCE} = 20mA	18	19		18	19		V
	I_{SOURCE} = 100mA	17	18		17	18		V
Undervoltage Lockout	V_{COMP} and $V_{SOFTSTART}$ = High	6	7	8	6	7	8	V
Collector Leakage	VC = 35V			200			200	µA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1525B and UC1527B; –40°C to +85°C for the UC2525B and UC2527B; 0°C to +70°C for the UC3525B and UC3527B; +VIN = 20V, $T_A = T_J$.

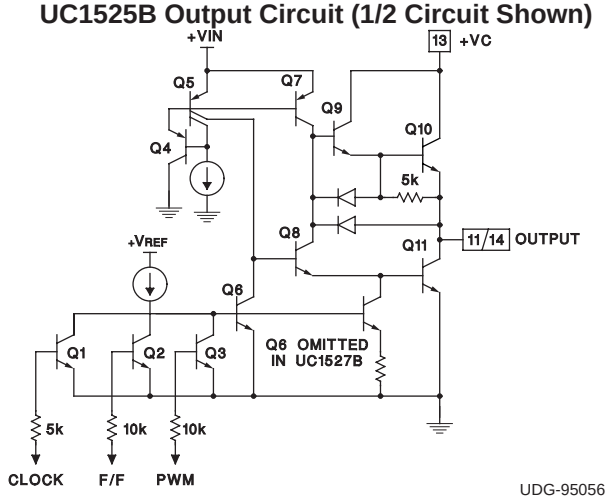
PARAMETER	TEST CONDITIONS	UC1525B/UC2525B UC1527B/UC2527B			UC3525B UC3527B			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Drivers (Each Output) (VC = 20V) (cont.)								
Rise Time (Note 2)	C_L = 1nF, T_J = 25°C		100	600		100	600	ns
Fall Time (Note 2)	C_L = 1nF, T_J = 25°C		50	300		50	300	ns
Cross conduction charge	Per cycle, T_J = 25°C		30			30		nc
Total Standby Current								
Supply Current	VIN = 35V		14	20		14	20	mA

Note 2: Ensured by design. Not 100% tested in production.
Note 3: Tested at fosc= 40kHz (R_T = 3.6KΩ, C_T = 0.01μF, R_D = 0Ω). Approximate oscillator frequency is defined by:

$$f = \frac{1}{C_T \bullet \left(0.7 \bullet R_T + 3R_D\right)}$$

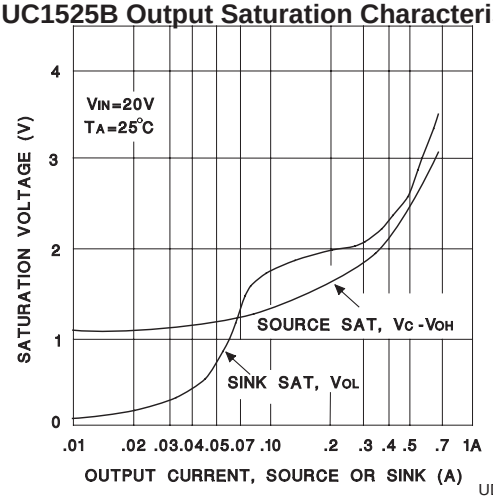
PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTICS

UC1525B Output Circuit (1/2 Circuit Shown)



UDG-95056

UC1525B Output Saturation Characteristics



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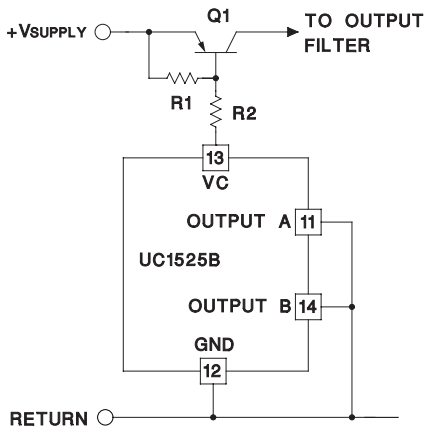

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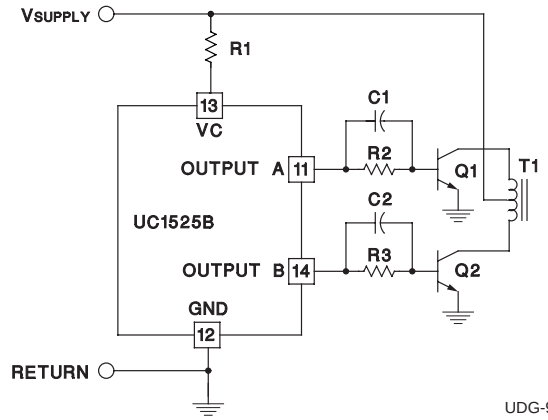
For single-ended supplies, the driver outputs are grounded. The VC terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.



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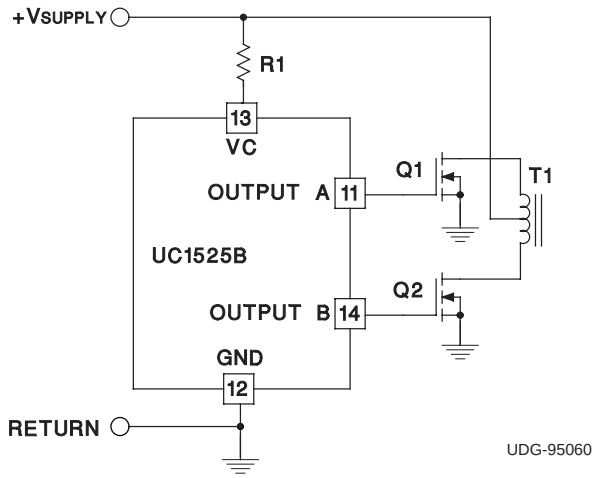
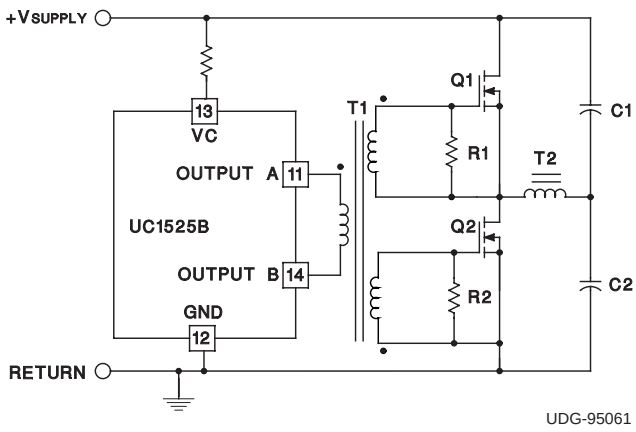
In conventional push-pull bipolar designs, forward base drive is controlled by R1-R3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C, and C2.



The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.



Low power transformers can be driven directly by the UC1525B. Automatic reset occurs during dead time, when both ends of the primary winding are switched to ground.

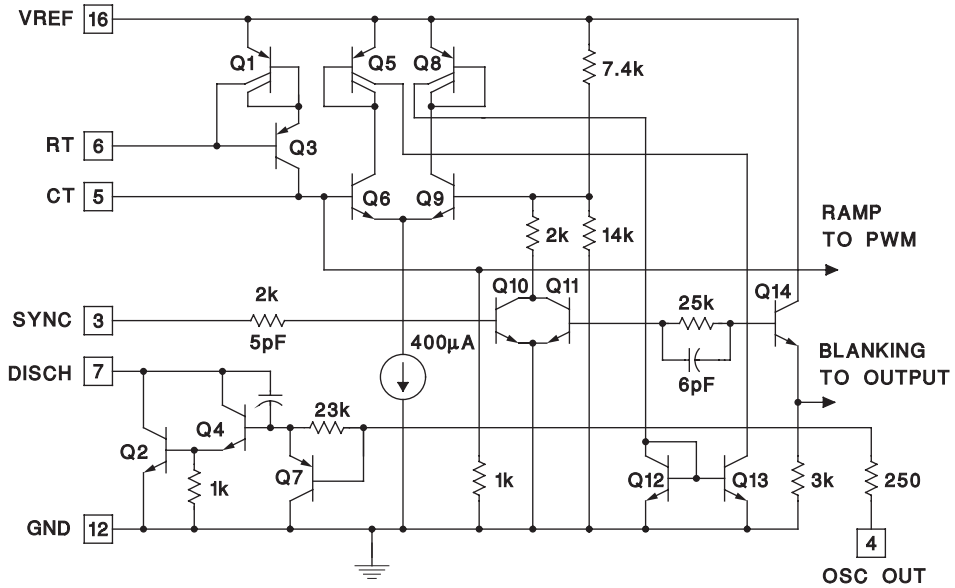
PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTICS

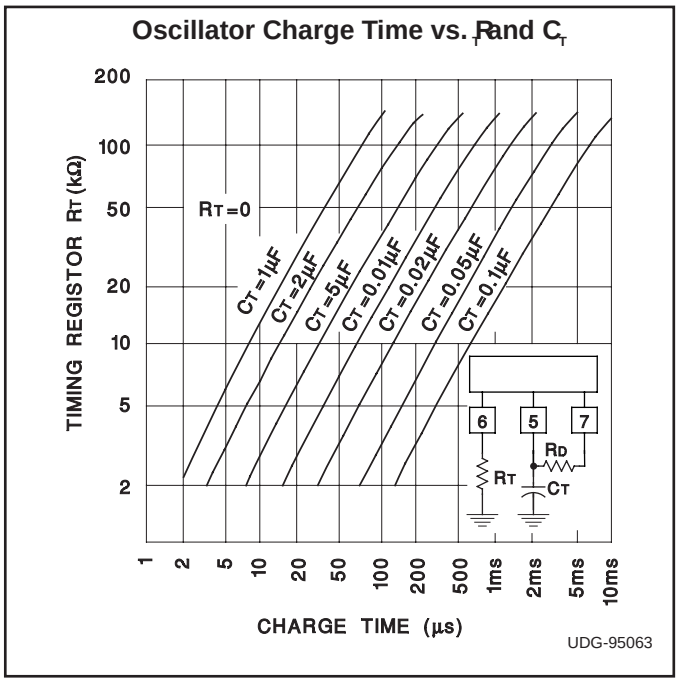
Shutdown Options (See Block Diagram)

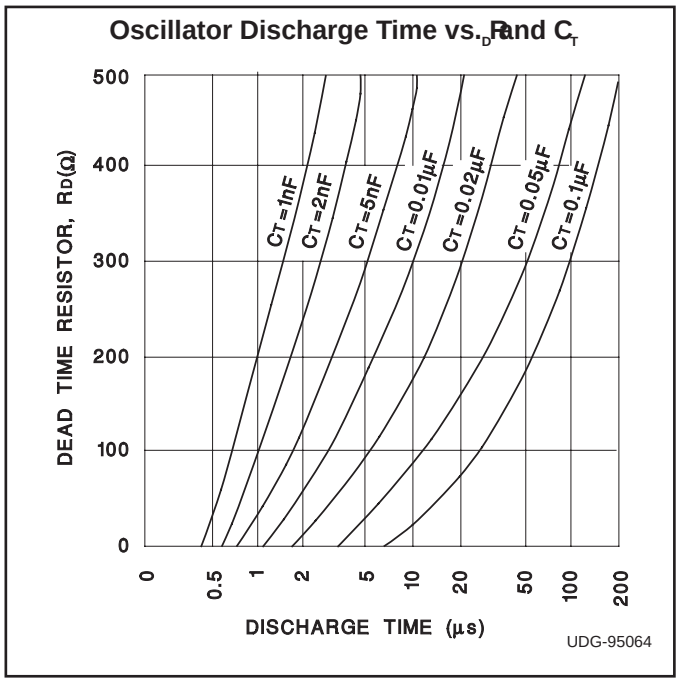
Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100μA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

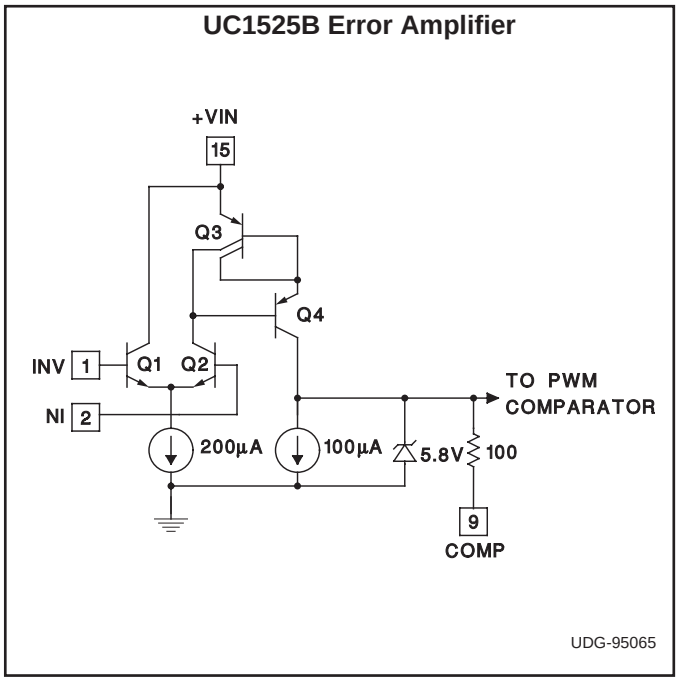
An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions: the PWM latch is immediately set providing the fastest turn-off signal to the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

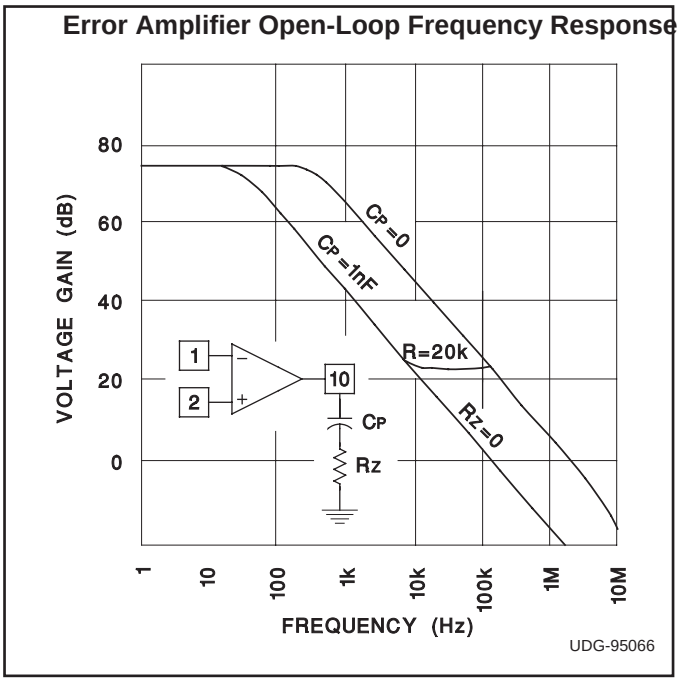
UC1525B Oscillator Schematic



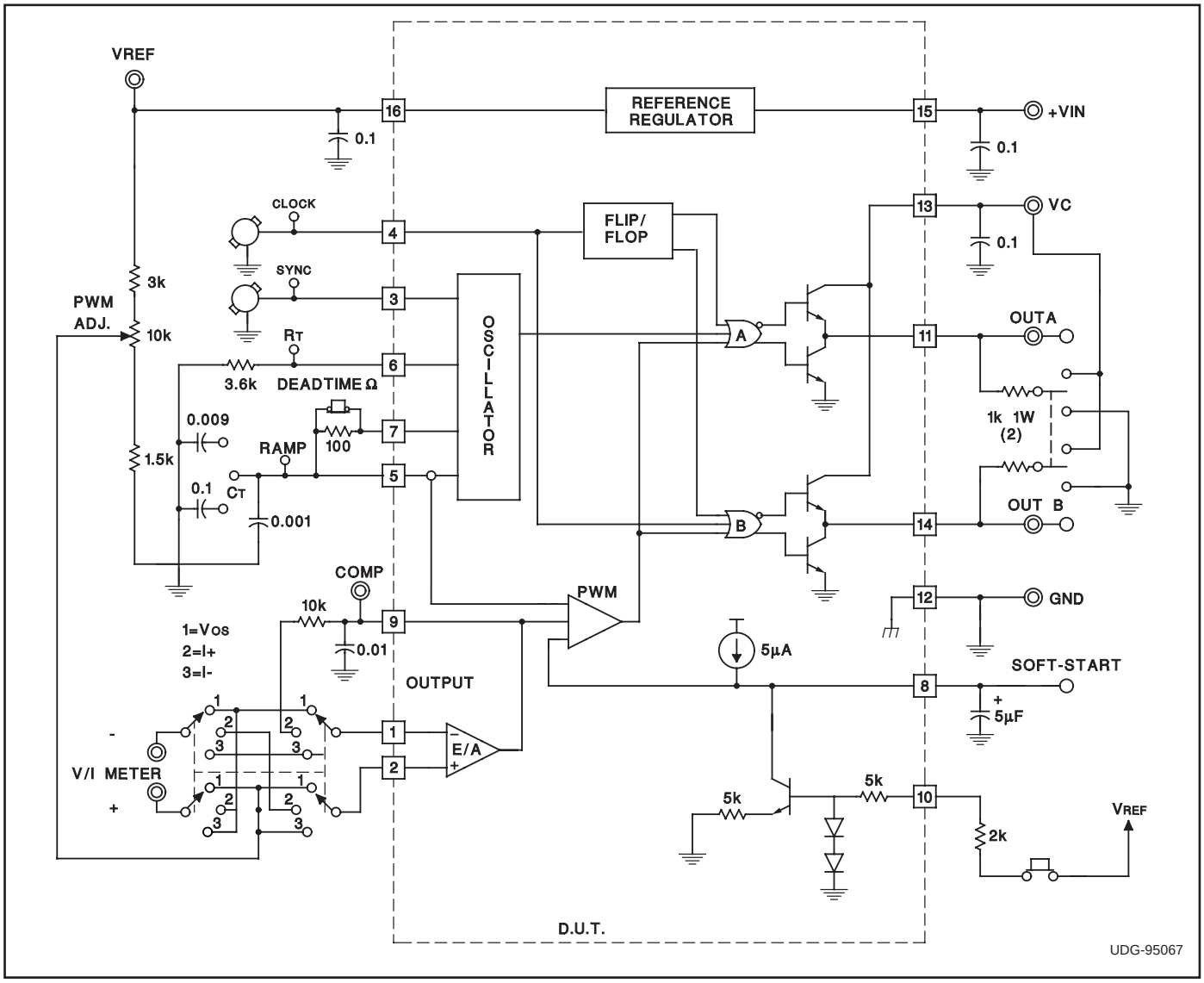

Oscillator Charge Time vs. R_T and C_T
TIMING REGISTOR R_T (kΩ)
200
100
50
20
10
5
2
R_T=0
C_T=1µF
C_T=2µF
C_T=5µF
C_T=0.01µF
C_T=0.02µF
C_T=0.05µF
C_T=0.1µF
6
5
7
R_D
R_T
C_T
1
2
5
10
20
50
100
200
500
1ms
2ms
5ms
10ms
CHARGE TIME (µs)
UDG-95063


Oscillator Discharge Time vs. R_D and C_T
DEAD TIME RESISTOR, R_D(Ω)
500
400
300
200
100
0
C_T=1nF
C_T=2nF
C_T=5nF
C_T=0.01µF
C_T=0.02µF
C_T=0.05µF
C_T=0.1µF
0
0.5
1
2
5
10
20
50
100
200
DISCHARGE TIME (µs)
UDG-95064


UC1525B Error Amplifier
+VIN
15
Q3
Q4
INV
1
Q1
Q2
NI
2
200µA
100µA
5.8V
100
TO PWM
COMPARATOR
9
COMP
UDG-95065


Error Amplifier Open-Loop Frequency Response
VOLTAGE GAIN (dB)
80
60
40
20
0
C_P=0
C_P=1nF
R=20k
R_Z=0
1
2
10
C_P
R_Z
1
10
100
1k
10k
100k
1M
10M
FREQUENCY (Hz)
UDG-95066

LAB TEST FIXTURE



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8951105EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8951105EA UC1525BJ/883B	Samples
UC1525BJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	UC1525BJ	Samples
UC1525BJ883B	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8951105EA UC1525BJ/883B	Samples
UC2525BDWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2525BDW	Samples
UC2525BDWTRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2525BDW	Samples
UC3525BDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3525BDW	Samples
UC3525BDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3525BDW	Samples
UC3525BDWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3525BDW	Samples
UC3525BDWTRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3525BDW	Samples
UC3525BN	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3525BN	Samples
UC3525BNG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3525BN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UC1525B, UC3525B :

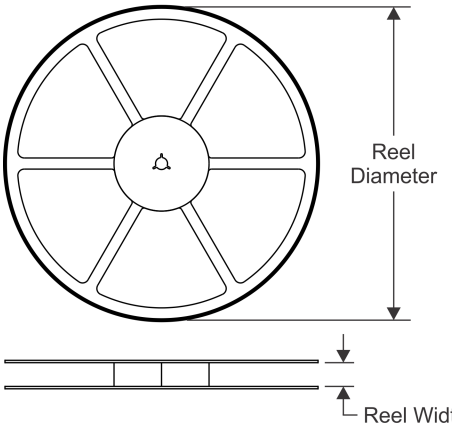
- Catalog: UC3525B
- Military: UC1525B
- Space: UC1525B-SP

NOTE: Qualified Version Definitions:

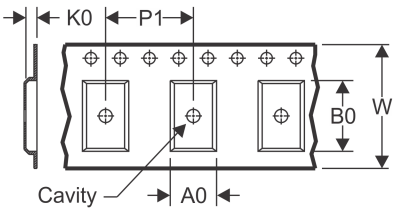
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

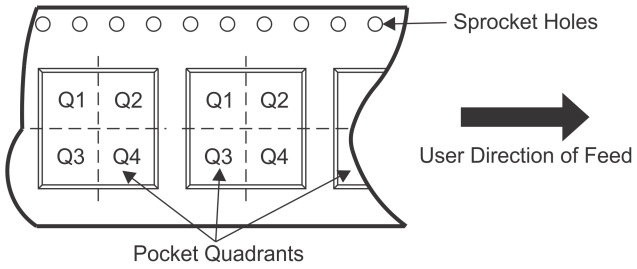


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

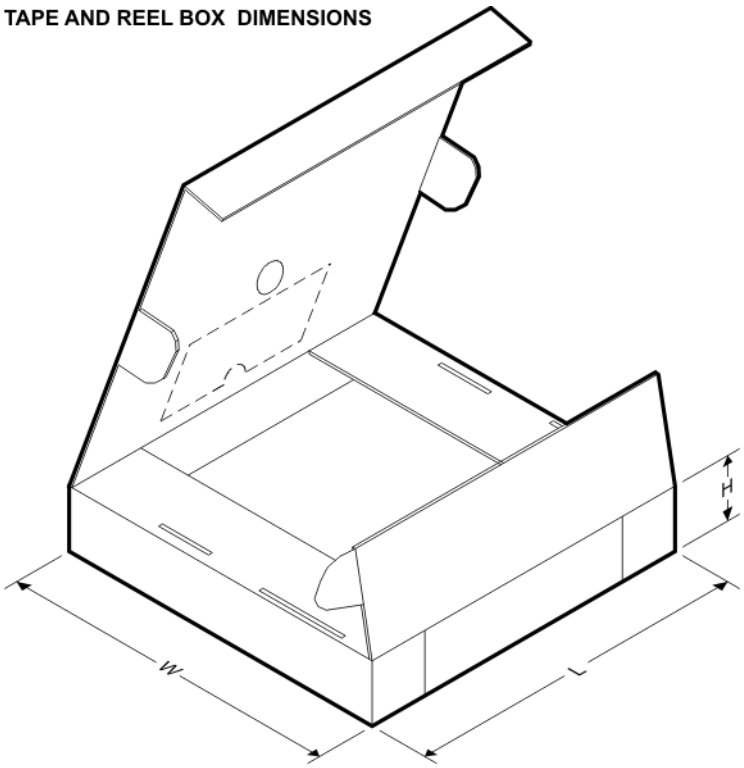
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2525BDWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



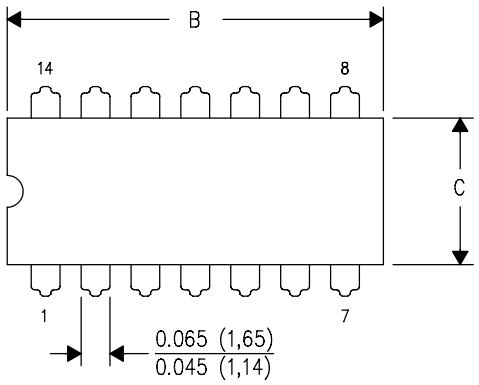
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2525BDWTR	SOIC	DW	16	2000	367.0	367.0	38.0

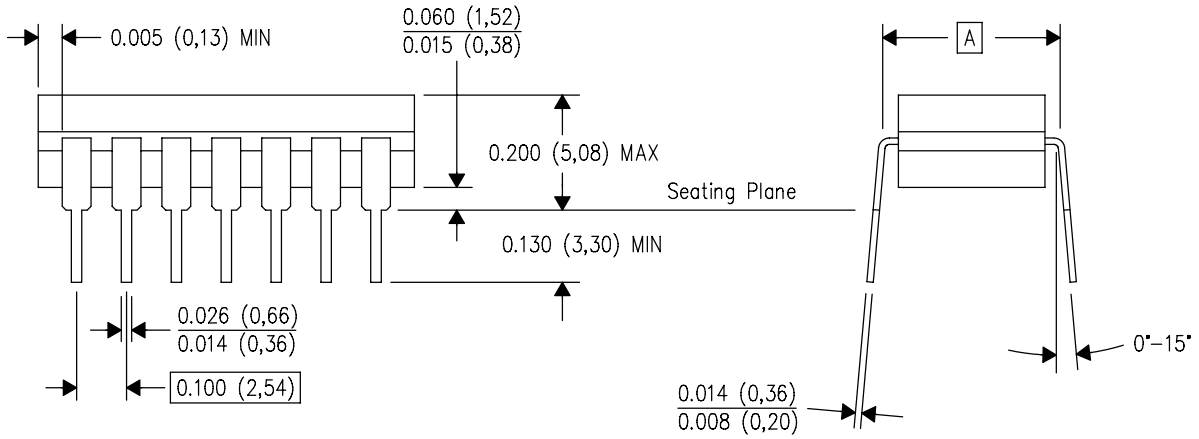
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



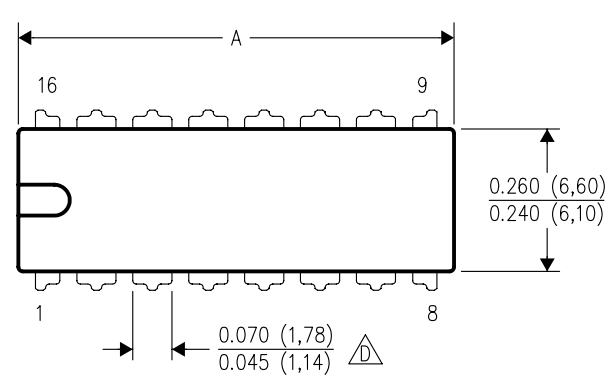
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

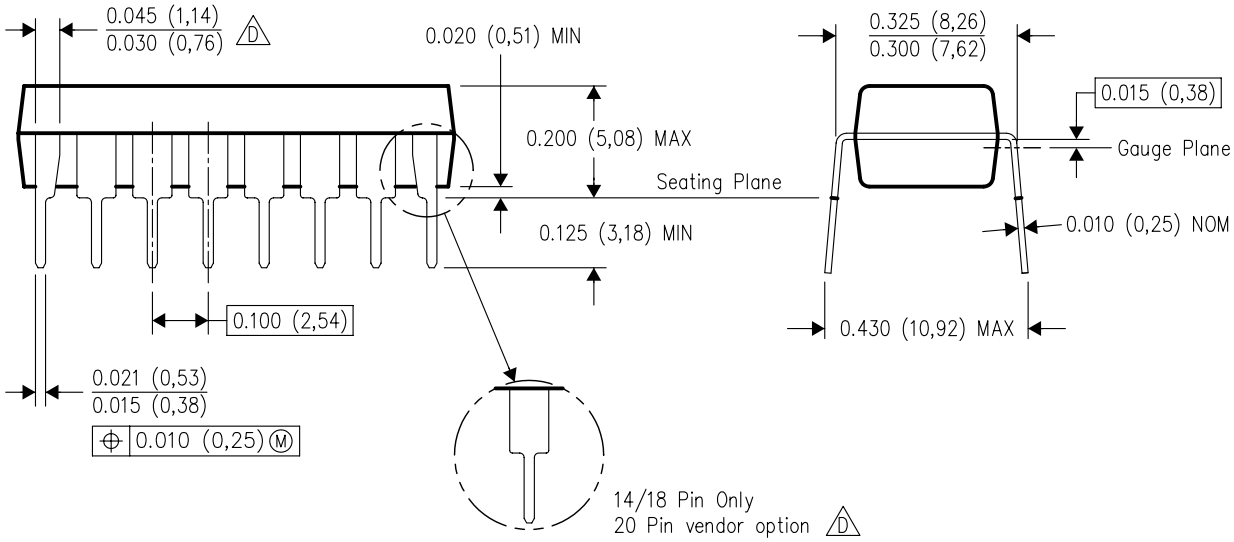
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



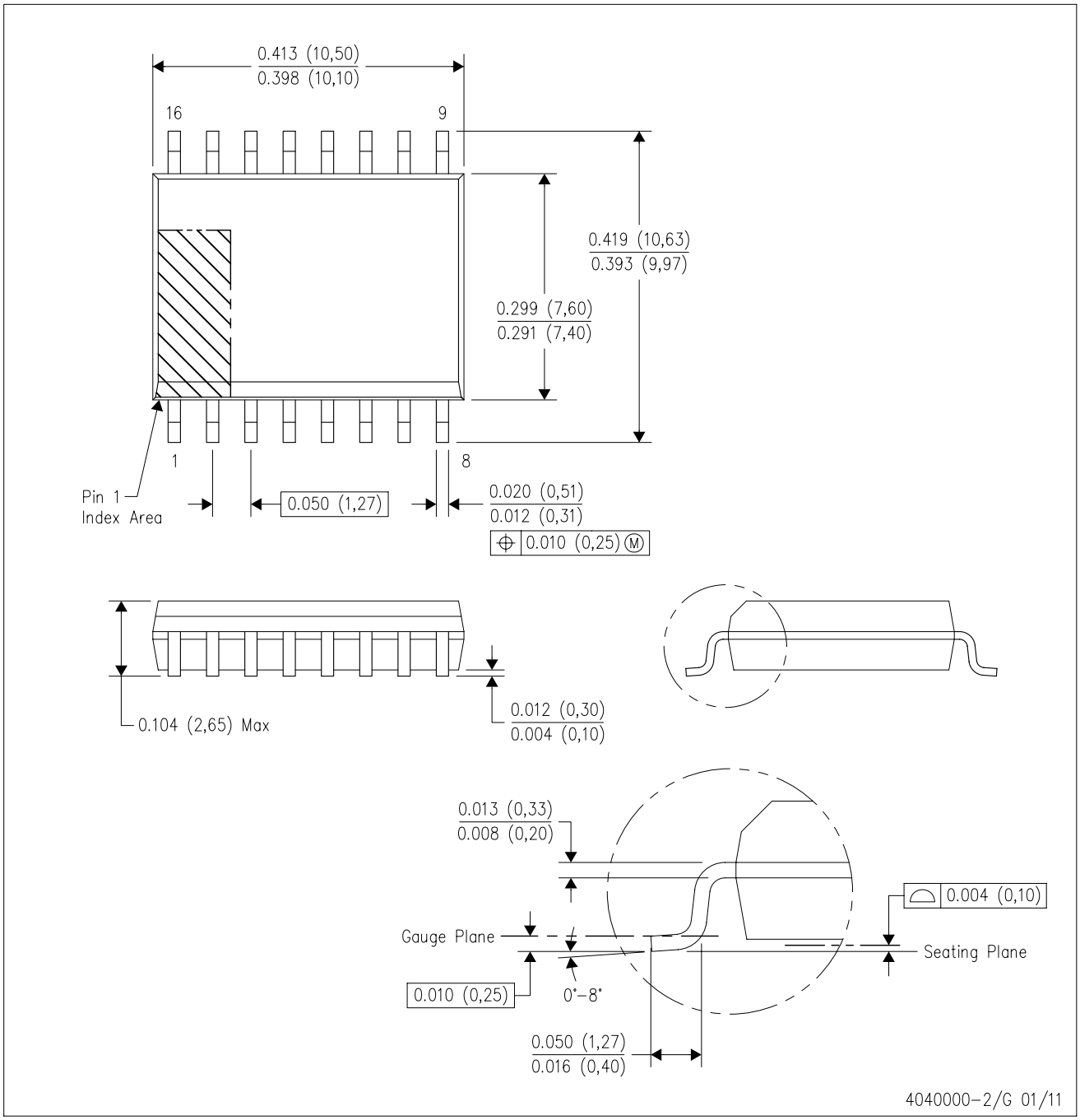
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

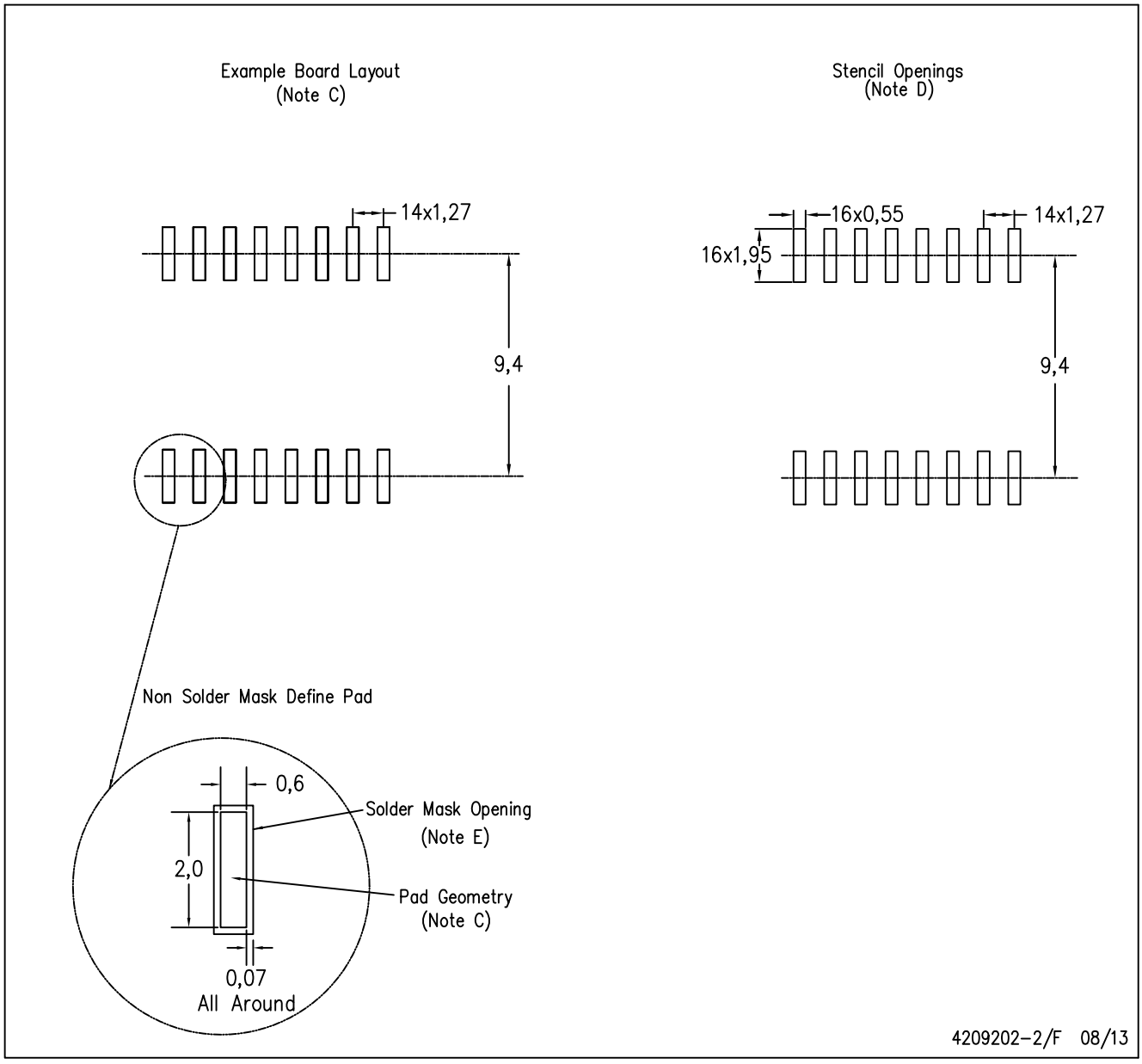
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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