

bq7716xy Overvoltage Protection for 2-Series to 4-Series Cell Li-Ion Batteries with External Delay Capacitor

1 Features

- 2-, 3-, and 4-Series Cell Overvoltage Protection
- External Capacitor-Programmed Delay Timer
- Fixed OVP Threshold
- High-Accuracy Overvoltage Protection: ± 10 mV
- Low Power Consumption $I_{CC} \approx 1$ μ A ($V_{CELL(ALL)} < V_{PROTECT}$)
- Low Leakage Current Per Cell Input < 100 nA
- Small Package Footprint
 - 8-pin WSON (3.00 mm $\times$ 4.00 mm)

2 Applications

- Power Tools
- UPS Battery Backup
- Light Electric Vehicles
 - eBike
 - eScooter
 - Pedal Assist Bicycles

3 Description

The bq7716xy device family provides an overvoltage monitor and protector for Li-Ion battery pack systems. Each cell is monitored independently for an overvoltage condition. For quicker production-line testing, the bq7716xy device provides a Customer Test Mode with greatly reduced delay time.

In the bq7716xy device, an external delay timer is initiated upon detection of an overvoltage condition on any cell. Upon expiration of the delay timer, the output is triggered into its active state (either high or low, depending on the configuration). The external delay timer feature also includes the ability to detect an open or shorted delay capacitor on the CD pin, which will similarly trigger the output driver in an overvoltage condition.

Table 1. Device Information Table⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq771600	WSON (8)	3.00 mm $\times$ 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet and the [Device Comparison Table](#).

4 Simplified Schematic

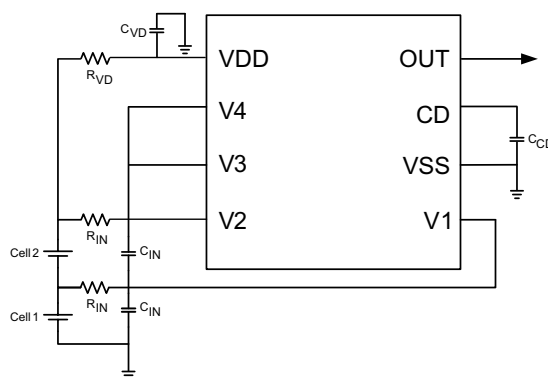


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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (August 2014) to Revision D	Page
• Changed QFN to WSON	1
• Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section	1
• Changed the bq771605 to Production Data	3
• Added table note 2, which was hidden inadvertently	4
• Moved Pin Details to Feature Description section	8
• Moved from Application Information section to Design Requirements section	13

Changes from Revision B (June 2014) to Revision C	Page
• Added the bq771612 device to Production Data.....	3

Changes from Revision A (September 2013) to Revision B	Page
• Changed the data sheet format.....	1
• Added the bq771611 device to Production Data.....	3

Changes from Original (December 2012) to Revision A	Page
• Added the bq771604 device to Production Data.....	3

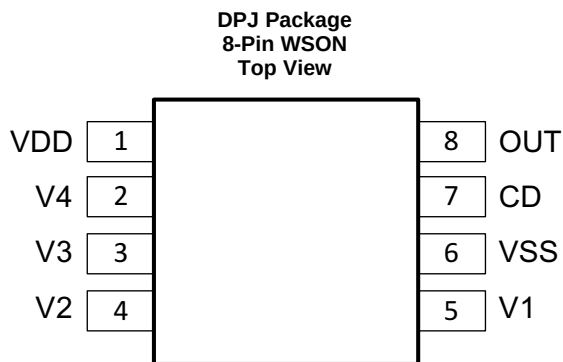
Table 2. Device Comparison Table

PART NUMBER	OVP (V)	OV HYSTERESIS (V)	OUTPUT DRIVE	TAPE AND REEL (LARGE)	TAPE AND REEL (SMALL)
bq771600	4.3	0.3	CMOS Active High	bq771600DPJR	bq771600DPJT
bq771601	4.225	0.05	CMOS Active High	bq771601DPJR	bq771601DPJT
bq771602	4.225	0.05	NCH Active Low, Open Drain	bq771602DPJR	bq771602DPJT
bq771603 ⁽¹⁾	4.325	0.05	NCH Active Low, Open Drain	bq771603DPJR	bq771603DPJT
bq771604	4.2	0.05	CMOS Active High	bq771604DPJR	bq771604DPJT
bq771605	3.85	0.25	NCH Active Low	bq771605DPJR	bq771605DPJT
bq771607 ⁽¹⁾	4.2	0.25	CMOS Active High	bq771607DPJR	bq771607DPJT
bq771608 ⁽¹⁾	4.225	0.25	CMOS Active High	bq771608DPJR	bq771608DPJT
bq771609 ⁽¹⁾	4.25	0.05	CMOS Active High	bq771609DPJR	bq771609DPJT
bq771610 ⁽¹⁾	4.250	0.25	CMOS Active High	bq771610DPJR	bq771610DPJT
bq771611	4.35	0.3	CMOS Active High	bq771611DPJR	bq771611DPJT
bq771612	3.9	0.3	CMOS Active High	bq771612DPJR	bq771612DPJT
bq771613 ⁽¹⁾	4.2	0.05	NCH Active Low	bq771613DPJR	bq771613DPJT
bq771614 ⁽¹⁾	4.225	0.25	NCH Active Low	bq771614DPJR	bq771614DPJT
bq771615 ⁽¹⁾	4.25	0.05	NCH Active Low	bq771615DPJR	bq771615DPJT
bq7716xy future options ⁽²⁾	3.85–4.65	0–0.3	CMOS Active High or NCH Active Low, Open Drain	bq7716xyTBD	bq7716xyTBD

(1) Product Preview only.

(2) Contact TI.

6 Pin Configuration and Functions


Pin Functions

PIN		TYPE I/O ⁽¹⁾	DESCRIPTION
NAME	NO.		
CD	7	I/O	External capacitor connection for delay timer
OUT	8	OA	Output drive for overvoltage fault signal
VDD	1	P	Power supply
VSS	6	P	Electrically connected to IC ground and negative terminal of the lowest cell in the stack
V1	5	I	Sense input for positive voltage of the lowest cell in the stack
V2	4	I	Sense input for positive voltage of the second cell from the bottom of the stack
V3	3	I	Sense input for positive voltage of the third cell from the bottom of the stack
V4	2	I	Sense input for positive voltage of the fourth cell from the bottom of the stack

(1) IA = Input Analog, OA = Output Analog, P = Power Connection

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage range ⁽²⁾	VDD–VSS	–0.3	30	V
Input voltage range ⁽²⁾	V4–V3, V3–V2, V2–V1, V1–VSS, or CD–VSS	–0.3	30	V
Output voltage range ⁽²⁾	OUT–VSS	–0.3	30	V
Continuous total power dissipation, P _{TOT}	See package dissipation rating.			
Functional temperature		–40	110	°C
Lead temperature (soldering, 10 s), T _{SOLDER}		300		°C
Storage temperature, T _{stg}		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Absolute maximum ratings for input voltage range, output voltage range, and supply voltage are assured by design and not tested in production.

7.2 ESD Ratings

		VALUE	UNIT
V _{ESD} Rating	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{DD} ⁽¹⁾	Supply voltage	3		20	V
V4–V3, V3–V2, V2–V1, V1–VSS, or CD–VSS	Input voltage range	0		5	V
T _A	Operating ambient temperature range	–40		110	°C

- (1) See [Typical Application](#).

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		bq7716xy	UNIT
		DPJ (WSON)	
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	56.6	°C/W
R _{θJC(top)}	Junction-to-case(top) thermal resistance	56.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	30.6	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	1.0	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	37.8	°C/W
R _{θJC(bot)}	Junction-to-case(bottom) thermal resistance	11.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

Typical values stated where $T_A = 25^\circ\text{C}$ and $V_{DD} = 14.4\text{ V}$, MIN/MAX values stated where $T_A = -40^\circ\text{C}$ to $+110^\circ\text{C}$ and $V_{DD} = 3\text{ V}$ to 20 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE PROTECTION THRESHOLD VCx						
V _{OV}	V ^(PROTECT) Overvoltage Detection	bq771600		4.300		V
		bq771601		4.225		V
		bq771602		4.225		V
		bq771603 ⁽¹⁾		4.325		V
		bq771604		4.200		V
		bq771605		3.850		V
		bq771607 ⁽¹⁾		4.200		V
		bq771608 ⁽¹⁾		4.225		V
		bq771609 ⁽¹⁾		4.250		V
		bq771610 ⁽¹⁾		4.250		V
		bq771611		4.350		V
		bq771612		3.900		V
		bq771613 ⁽¹⁾		4.200		V
		bq771614 ⁽¹⁾		4.225		V
		bq771615 ⁽¹⁾		4.250		V
V _{HYS}	OV Detection Hysteresis	bq771600	250	300	400	mV
		bq771601	25	50	75	mV
		bq771602	25	50	75	mV
		bq771603 ⁽¹⁾	25	50	75	mV
		bq771604	25	50	75	mV
		bq771605	200	250	300	mV
		bq771607 ⁽¹⁾	200	250	300	mV
		bq771608 ⁽¹⁾	200	250	300	mV
		bq771609 ⁽¹⁾	25	50	75	mV
		bq771610 ⁽¹⁾	200	250	300	mV
		bq771611	250	300	400	mV
		bq771612	250	300	400	mV
		bq771613 ⁽¹⁾	25	50	75	mV
		bq771614 ⁽¹⁾	200	250	300	mV
		bq771615 ⁽¹⁾	25	50	75	mV
V _{OA}	OV Detection Accuracy	T _A = 25°C	−10		10	mV
V _{OADRIFT}	OV Detection Accuracy Across Temperature	T _A = −40°C	−40		44	mV
		T _A = 0°C	−20		20	mV
		T _A = 60°C	−24		24	mV
		T _A = 110°C	−54		54	mV
SUPPLY AND LEAKAGE CURRENT						
I _{CC}	Supply Current	(V4−V3) = (V3−V2) = (V2−V1) = (V1−VSS) = 4.0 V (See Figure 10.)		1	2	μA
I _{IN}	Input Current at Vx Pins	(V4−V3) = (V3−V2) = (V2−V1) = (V1−VSS) = 4.0 V (See Figure 10.)	−0.1		0.1	μA

(1) Future option. Contact TI.

Electrical Characteristics (continued)

Typical values stated where $T_A = 25^\circ\text{C}$ and $V_{DD} = 14.4\text{ V}$, MIN/MAX values stated where $T_A = -40^\circ\text{C}$ to $+110^\circ\text{C}$ and $V_{DD} = 3\text{ V}$ to 20 V (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT DRIVE OUT, CMOS ACTIVE HIGH VERSIONS ONLY					
V_{OUT1} Output Drive Voltage, Active High	(V4–V3), (V3–V2), (V2–V1), or (V1–VSS) $> V_{OV}$, $V_{DD} = 14.4\text{ V}$, $I_{OH} = 100\text{ }\mu\text{A}$	6			V
	If three of four cells are short circuited, only one cell remains powered and $> V_{OV}$, $V_{DD} = V_x$ (cell voltage), $I_{OH} = 100\text{ }\mu\text{A}$		$V_{DD} - 0.3$		V
	(V4–V3), (V3–V2), (V2–V1), and (V1–VSS) $< V_{OV}$, $V_{DD} = 14.4\text{ V}$, $I_{OL} = 100\text{ }\mu\text{A}$ measured into OUT pin		250	400	mV
I_{OUTH1} OUT Source Current (During OV)	(V4–V3), (V3–V2), (V2–V1), or (V1–VSS) $> V_{OV}$, $V_{DD} = 14.4\text{ V}$, OUT = 0 V. Measured out of OUT pin			4.5	mA
I_{OUTL1} OUT Sink Current (No OV)	(V4–V3), (V3–V2), (V2–V1), and (V1–VSS) $< V_{OV}$, $V_{DD} = 14.4\text{ V}$, OUT = V_{DD} . Measured into OUT pin	0.5		14	mA
OUTPUT DRIVE OUT, NCH OPEN DRAIN ACTIVE LOW VERSIONS ONLY					
V_{OUT2} Output Drive Voltage, Active Low	(V4–V3), (V3–V2), (V2–V1), or (V1–VSS) $> V_{OV}$, $V_{DD} = 14.4\text{ V}$, $I_{OL} = 100\text{ }\mu\text{A}$ measured into OUT pin		250	400	mV
I_{OUTH2} OUT Sink Current (During OV)	(V4–V3), (V3–V2), (V2–V1), or (V1–VSS) $> V_{OV}$, $V_{DD} = 14.4\text{ V}$, OUT = V_{DD} . Measured into OUT pin	0.5		14	mA
I_{OUTLK} OUT Pin Leakage	(V4–V3), (V3–V2), (V2–V1), and (V1–VSS) $< V_{OV}$, $V_{DD} = 14.4\text{ V}$, OUT = V_{DD} . Measured out of OUT pin			100	nA
DELAY TIMER					
t_{CD} OV Delay Time	$C_{CD} = 0.1\text{ }\mu\text{F}$ (For capacitor sizing, see .)	1	1.5	2	s
V_{CD} CD Fault Detection External Comparator Threshold, Initial Charge Value	The CD pin will first be quickly charged to this value before being discharged back to VSS.		1.5		V
$t_{CHGDELAY}$ CD Charging Delay	OVP to OUT delay with CD shorted to ground	20		170	ms
I_{CHG} OV Detection Charging Current	CD pin fast charging current from VSS to V_{CD} to begin delay countdown		300		μA
I_{DSG} OV Detection Discharging Current	CD pin discharging current from V_{DELAY} to VSS		100		nA

7.6 Typical Characteristics

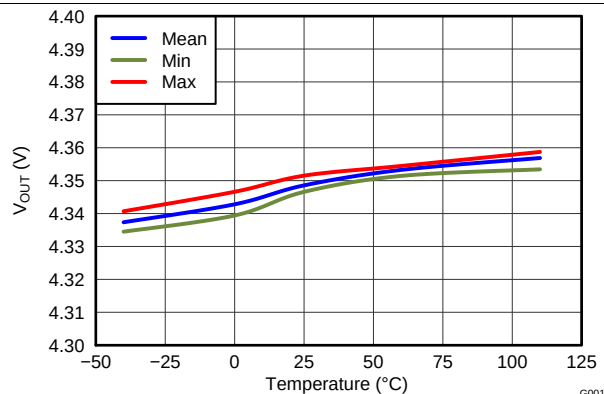


Figure 2. Overvoltage Threshold (OVT) vs. Temperature

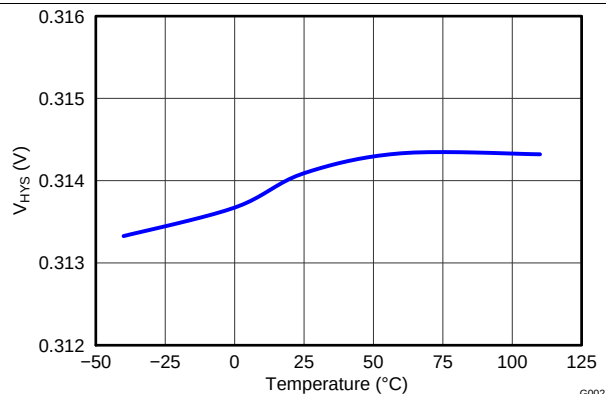


Figure 3. Hysteresis V_{HYS} vs. Temperature

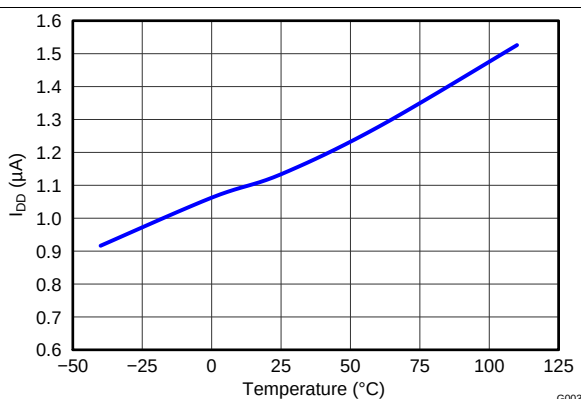


Figure 4. I_{DD} Current Consumption vs. Temperature at $V_{DD} = 16$ V

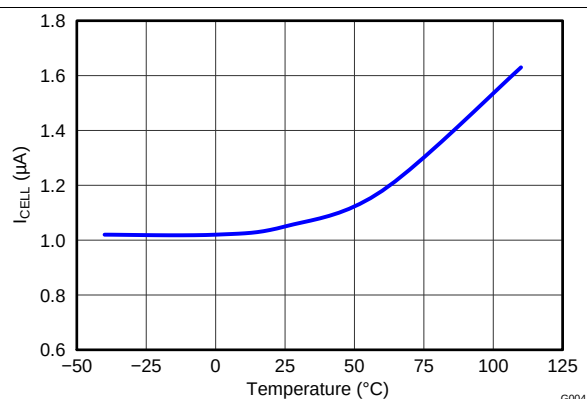


Figure 5. I_{CELL} vs. Temperature at $V_{CELL} = 9.2$ V

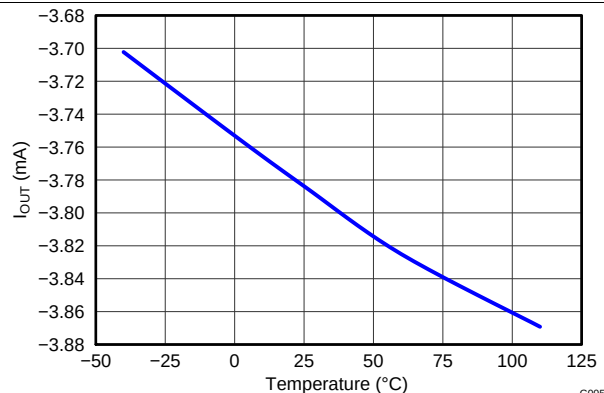


Figure 6. Output Current I_{OUT} vs. Temperature

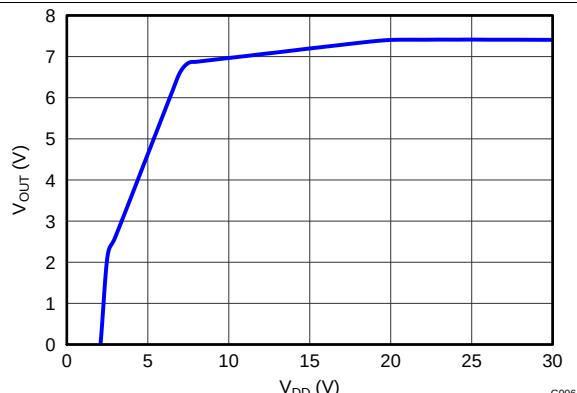


Figure 7. V_{OUT} vs. V_{DD}

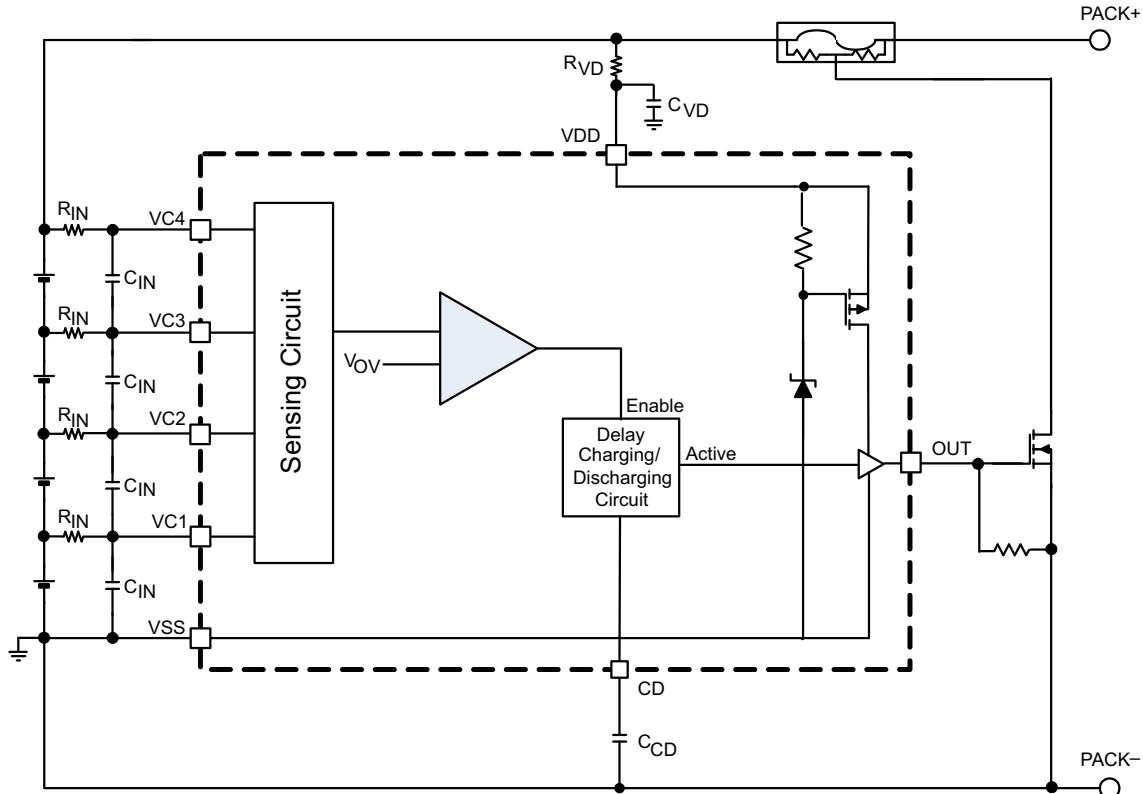
8 Detailed Description

8.1 Overview

In the bq7716xy family of devices for overvoltage protection, each cell is monitored independently and an external delay timer is initiated if an overvoltage condition is detected when any cell voltage is higher than the protection voltage threshold, VOV. After the delay time expires, the OUT pin is inserted.

For quicker production-line testing, the device provides a Customer Test Mode with greatly reduced delay time.

8.2 Functional Block Diagram



8.3 Feature Description

In the bq7716xy device, each cell is monitored independently. Overvoltage is detected by comparing the actual cell voltage to a protection voltage reference, VOV. If any cell voltage exceeds the programmed OV value, a timer circuit is activated. This timer circuit charges the CD pin to a nominal value, then slowly discharges it with a fixed current back down to VSS. When the CD pin falls below a nominal threshold near VSS, the OUT terminal goes from inactive to active state. Additionally, a timeout detection circuit checks to ensure that the CD pin successfully begins charging to above VSS and subsequently drops back down to VSS, and if a timeout error is detected in either direction, it will similarly trigger the OUT pin to become active. See [Figure 8](#) for reference.

For an NCH Open Drain Active Low configuration, the OUT pin pulls down to VSS when active (OV present), and is high impedance when inactive (no OV).

Feature Description (continued)

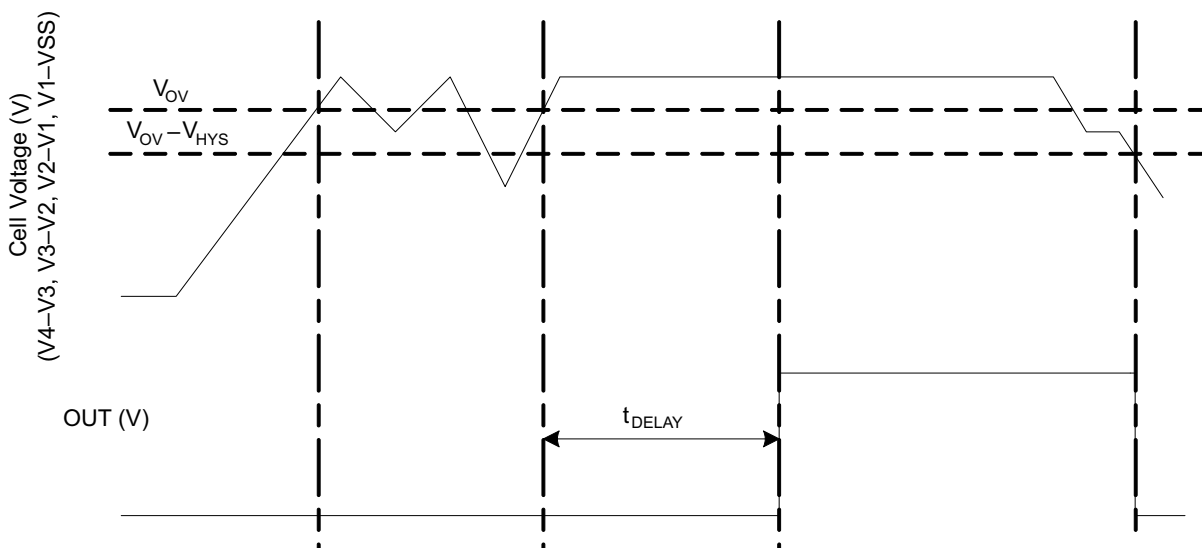


Figure 8. Timing for Overvoltage Sensing

Figure 9 shows an overview of the behavior of the CD pin during an OV sequence.

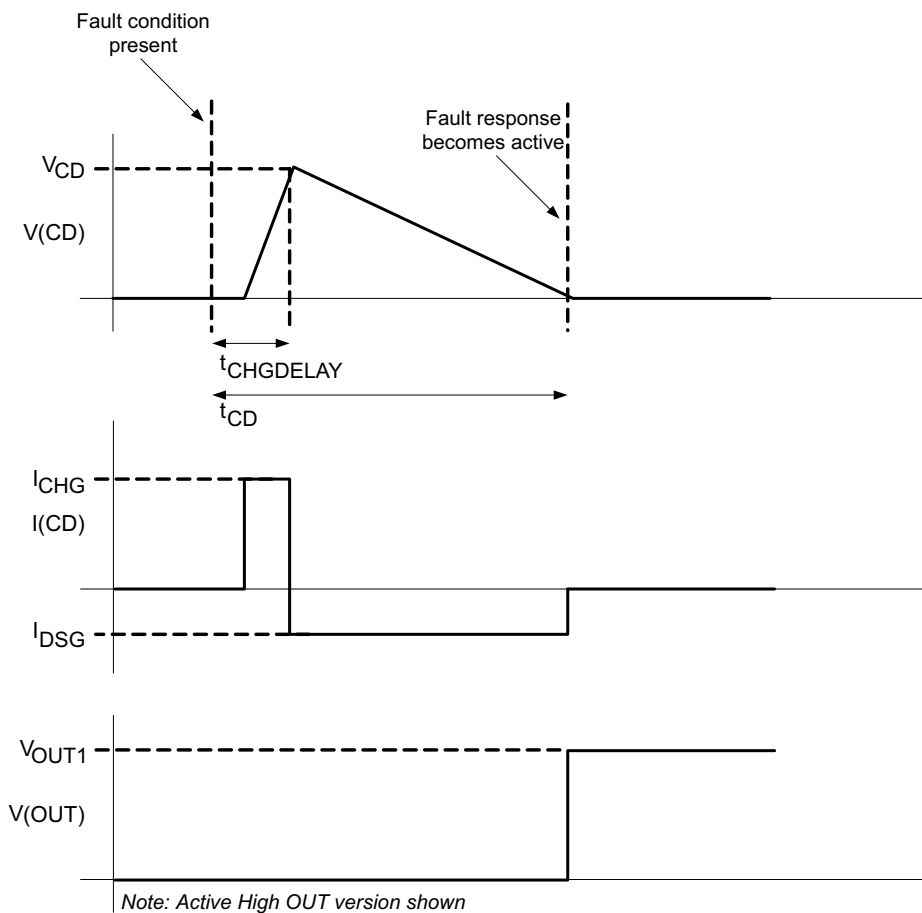


Figure 9. CD Pin Mechanism

Feature Description (continued)

8.3.1 Sense Positive Input for V_x

This is an input to sense each single battery cell voltage. A series resistor and a capacitor across the cell for each input is required for noise filtering and stable voltage monitoring.

8.3.2 Output Drive, OUT

This terminal serves as the fault signal output, and may be ordered in either active HIGH or LOW options.

8.3.3 Supply Input, VDD

This terminal is the unregulated input power source for the IC. A series resistor is connected to limit the current, and a capacitor is connected to ground for noise filtering.

8.3.4 External Delay Capacitor, CD

This terminal is connected to an external capacitor that is used for setting the delay timer during an overvoltage fault event.

The CD pin includes a timeout detection circuit to ensure that the output drives active even with a shorted or open capacitor during an overvoltage event.

The capacitor connected on the CD pin rapidly charges to a voltage if any one of the cell inputs exceeds the OV threshold. Then the delay circuit gradually discharges the capacitor on the CD pin. Once this capacitor discharges below a set voltage, the OUT transitions from an inactive to active state.

To calculate the delay, use the following equation:

$$t_{CD} (s) = K \times C_{CD} (\mu F), \text{ where } K = 10 \text{ to } 20 \text{ range.} \quad (1)$$

Example: If $C_{CD} = 0.1 \mu F$ (typical), then the delay timer range is

$$t_{CD} (s) = 10 \times 0.1 = 1 \text{ s (Minimum)}$$

$$t_{CD} (s) = 20 \times 0.1 = 2 \text{ s (Maximum)}$$

NOTE

The tolerance on the capacitor used for C_{CD} increases the range of the t_{CD} timer.

8.4 Device Functional Modes

8.4.1 NORMAL Mode

When all of the cell voltages are below the overvoltage threshold, VOV, the device operates in NORMAL mode. The device monitors the differential cell voltages connected across (V1–VSS), (V2–V1), (V3–V2), and (V4–V3). The OUT pin is inactive and if configured:

- Active high is low
- Active low is being externally pulled up and is an open drain

8.4.2 OVERVOLTAGE Mode

OVERVOLTAGE mode is detected if any of the cell voltages exceeds the overvoltage threshold, VOV for configured OV delay time. The OUT pin is activated after a delay time set by the capacitance in the CD pin. The OUT pin will either pull high internally, if configured as active high, or will be pulled low internally, if configured as active low. When all of the cell voltages fall below the (VOV–VHYS), the device returns to NORMAL mode

8.4.3 Customer Test Mode

It is possible to reduce test time for checking the overvoltage function by simply shorting the external CD capacitor to VSS. In this case, the OV delay would be reduced to the $t_{(CHGDELAY)}$ value, which has a maximum of 170 ms.

Device Functional Modes (continued)

CAUTION

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the part into Customer Test Mode. Also avoid exceeding Absolute Maximum Voltages for the individual cell voltages (V4–V3), (V3–V2), (V2–V1), and (V1–VSS). Stressing the pins beyond the rated limits may cause permanent damage to the device.

Figure 10 shows the timing for the Customer Test Mode.

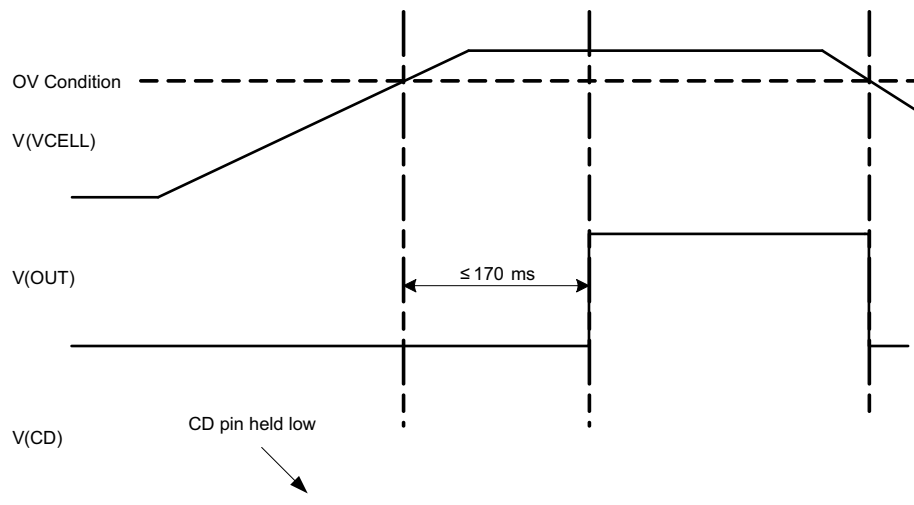


Figure 10. Timing for Customer Test Mode

Figure 11 shows the measurement for current consumption for the product for both VDD and Vx.

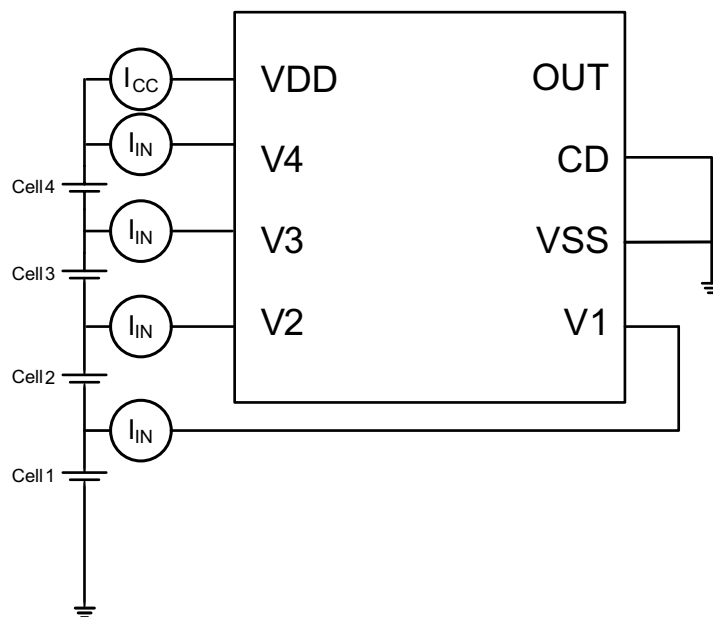


Figure 11. Configuration for IC Current Consumption Test

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Figure 12 shows each external component.

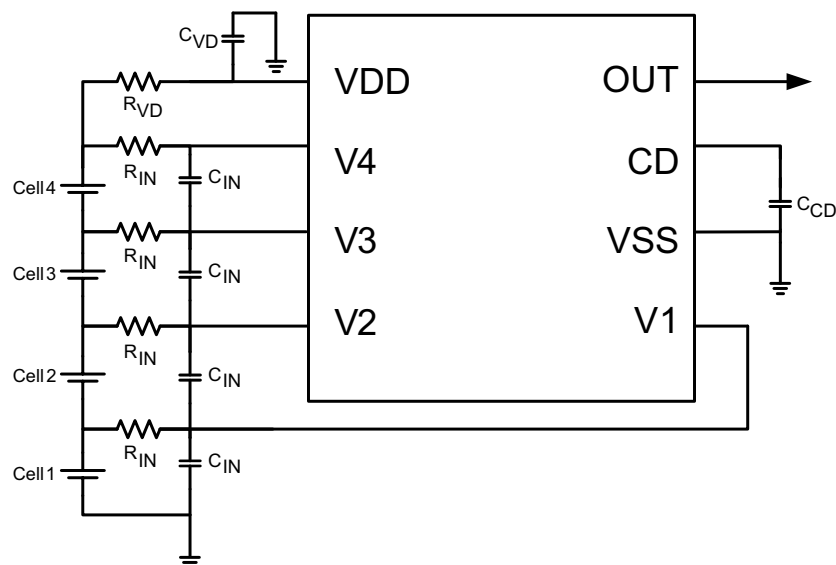


Figure 12. Application Configuration

NOTE

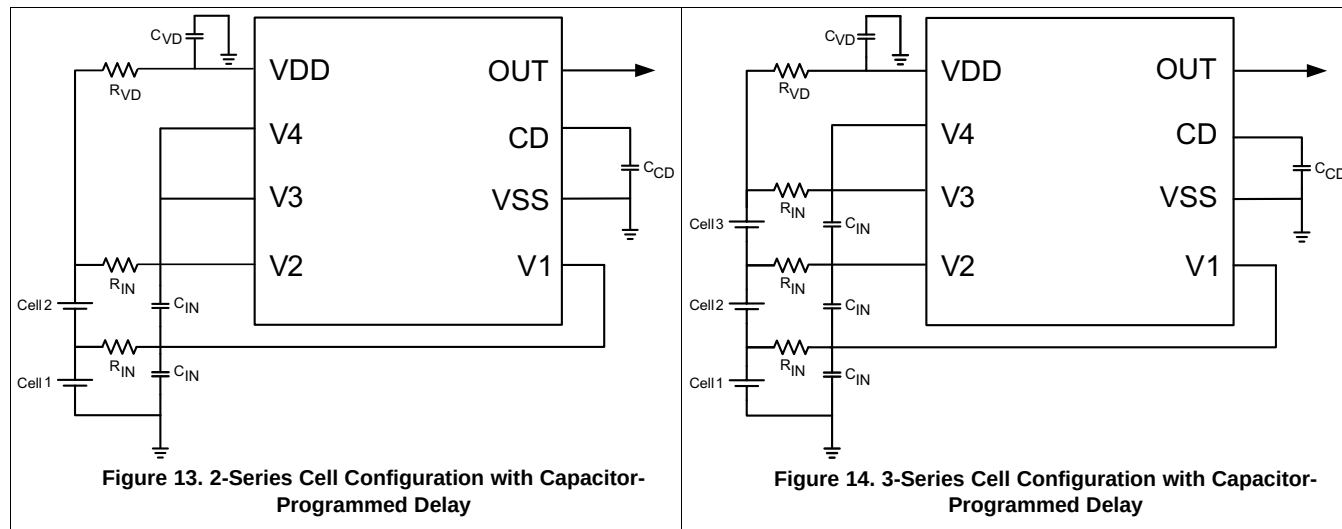
In the case of an Open Drain Active Low configuration, an external pull-up resistor is required on the OUT terminal.

Changes to the ranges stated in [Table 3](#) will impact the accuracy of the cell measurements.

NOTE

The device is calibrated using an R_{IN} value = 1 k Ω . Using a value other than this recommended value changes the accuracy of the cell voltage measurements and V_{OV} trigger level.

9.2 Typical Application



NOTE

In these application examples of 2 s and 3 s, an external pull-up resistor is required on the OUT terminal to configure for an Open Drain Active Low operation.

9.2.1 Design Requirements

Changes to the ranges stated in [Table 3](#) will impact the accuracy of the cell measurements.

Table 3. Design Parameters

PARAMETER	EXTERNAL COMPONENT	MIN	NOM	MAX	UNIT
Voltage monitor filter resistance	R_{IN}	900	1000	1100	Ω
Voltage monitor filter capacitance	C_{IN}	0.01		0.1	μF
Supply voltage filter resistance	R_{VD}	100		1K	Ω
Supply voltage filter capacitance	C_{VD}		0.1		μF
CD external delay capacitance	C_{CD}		0.1	1	μF
OUT Open drain version pull-up resistance to PACK+	R_{OUT}		100k		Ω

9.2.2 Detailed Design Procedure

1. Determine the number of cells in series. The device supports a 2-S to 4-S cell configuration. For 2S and 3S, the top unused pin(s) should be shorted as shown in [Figure 13](#) and [Figure 14](#).
2. Determine the overvoltage protection delay. Follow the calculation example described in [External Delay Capacitor, CD](#). Select the correct capacitor to connect to the CD pin.
3. Follow the application schematic to connect the device. If the OUT pin is configured to open drain, an external pull-up resistor should be used. Refer to the Out Sink Current specification, IOUTH2 to ensure a proper pull-up resistor value is used, so that the OUT pin sink current is able to pull down the pin during OV condition.

9.2.3 Application Curves

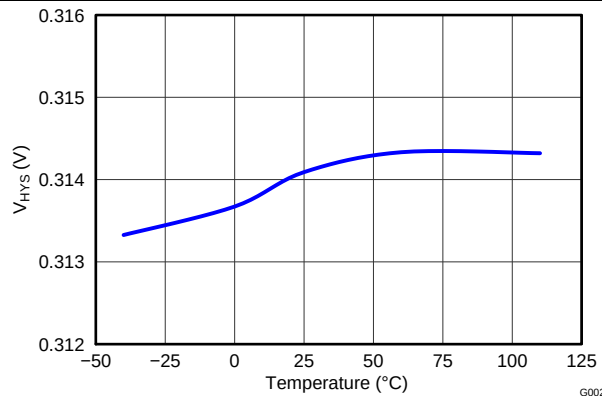


Figure 15. Hysteresis V_{HYS} vs. Temperature

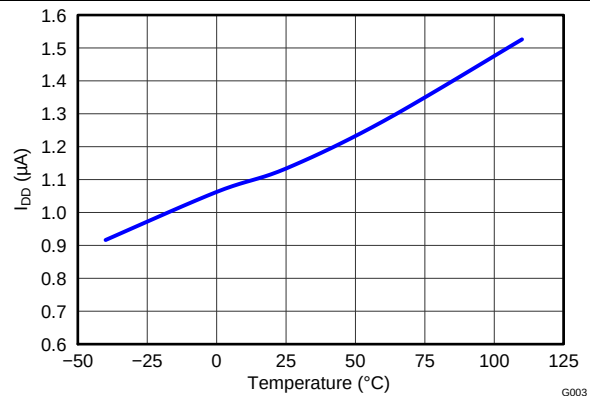


Figure 16. I_{DD} Current Consumption vs. Temperature at $V_{DD} = 16$ V

10 Power Supply Recommendations

The maximum power of this device is 20 V on V_{DD} .

11 Layout

11.1 Layout Guidelines

1. Ensure the RC filters for the V_x pins and V_{DD} pin are placed as close as possible to the target terminal, reducing the tracing loop area.
2. The capacitor for CD pin should be placed close to the IC terminals.

11.2 Layout Example

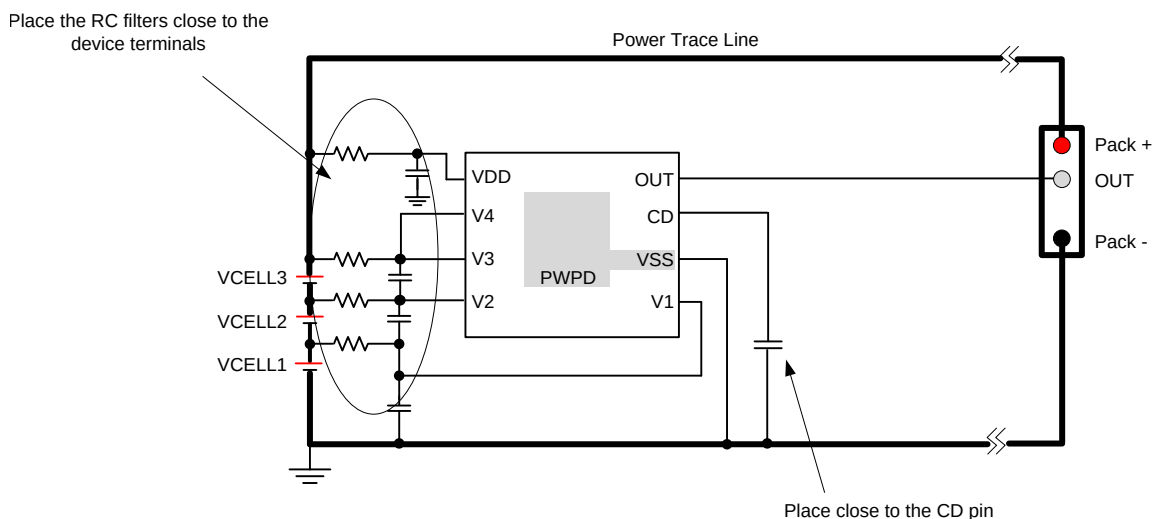


Figure 17. Layout

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
bq771600	Click here	Click here	Click here	Click here	Click here
bq771601	Click here	Click here	Click here	Click here	Click here
bq771602	Click here	Click here	Click here	Click here	Click here
bq771604	Click here	Click here	Click here	Click here	Click here
bq771605	Click here	Click here	Click here	Click here	Click here
bq771611	Click here	Click here	Click here	Click here	Click here
bq771612	Click here	Click here	Click here	Click here	Click here

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

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All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ771600DPJR	ACTIVE	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		771600	Samples
BQ771600DPJT	ACTIVE	WSON	DPJ	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		771600	Samples
BQ771601DPJR	ACTIVE	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		771601	Samples
BQ771601DPJT	ACTIVE	WSON	DPJ	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		771601	Samples
BQ771602DPJR	ACTIVE	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		771602	Samples
BQ771602DPJT	ACTIVE	WSON	DPJ	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		771602	Samples
BQ771604DPJR	ACTIVE	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771604	Samples
BQ771604DPJT	ACTIVE	WSON	DPJ	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771604	Samples
BQ771605DPJR	ACTIVE	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771605	Samples
BQ771605DPJT	ACTIVE	WSON	DPJ	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771605	Samples
BQ771611DPJR	ACTIVE	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771611	Samples
BQ771611DPJT	ACTIVE	WSON	DPJ	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771611	Samples
BQ771612DPJR	ACTIVE	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771612	Samples
BQ771612DPJT	ACTIVE	WSON	DPJ	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771612	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

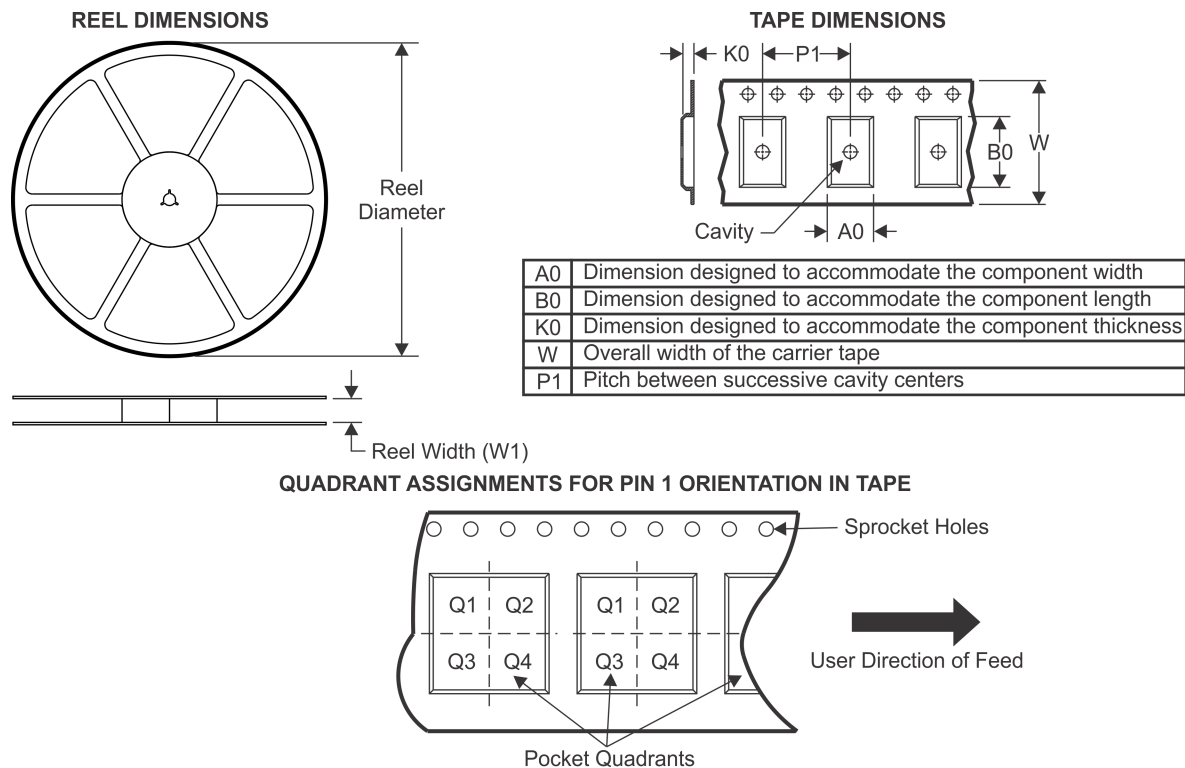
⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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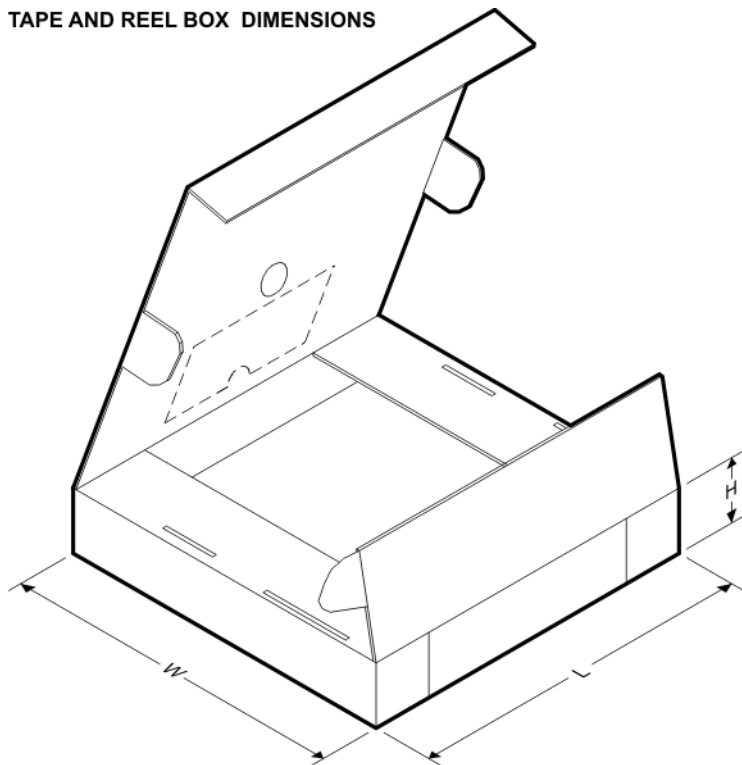
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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ771600DPJR	WSO	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771600DPJT	WSO	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771601DPJR	WSO	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771601DPJT	WSO	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771602DPJR	WSO	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771602DPJT	WSO	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771604DPJR	WSO	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771604DPJT	WSO	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771605DPJR	WSO	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771605DPJT	WSO	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771611DPJR	WSO	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771611DPJT	WSO	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771612DPJR	WSO	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771612DPJT	WSO	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

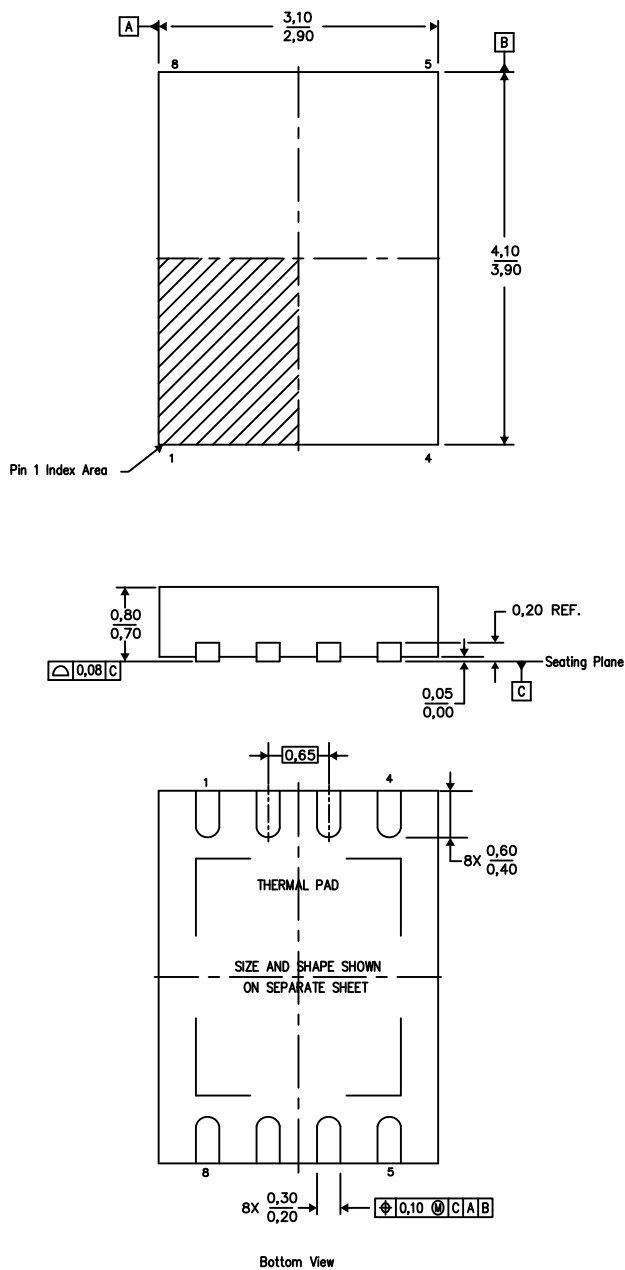


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ771600DPJR	WSN	DPJ	8	3000	367.0	367.0	35.0
BQ771600DPJT	WSN	DPJ	8	250	210.0	185.0	35.0
BQ771601DPJR	WSN	DPJ	8	3000	367.0	367.0	35.0
BQ771601DPJT	WSN	DPJ	8	250	210.0	185.0	35.0
BQ771602DPJR	WSN	DPJ	8	3000	367.0	367.0	35.0
BQ771602DPJT	WSN	DPJ	8	250	210.0	185.0	35.0
BQ771604DPJR	WSN	DPJ	8	3000	367.0	367.0	35.0
BQ771604DPJT	WSN	DPJ	8	250	210.0	185.0	35.0
BQ771605DPJR	WSN	DPJ	8	3000	367.0	367.0	35.0
BQ771605DPJT	WSN	DPJ	8	250	210.0	185.0	35.0
BQ771611DPJR	WSN	DPJ	8	3000	367.0	367.0	35.0
BQ771611DPJT	WSN	DPJ	8	250	210.0	185.0	35.0
BQ771612DPJR	WSN	DPJ	8	3000	367.0	367.0	35.0
BQ771612DPJT	WSN	DPJ	8	250	210.0	185.0	35.0

DPJ (R-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



4212590/B 04/12

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Small Outline No-Lead (SON) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

THERMAL PAD MECHANICAL DATA

DPJ (R-PWSON-N8)

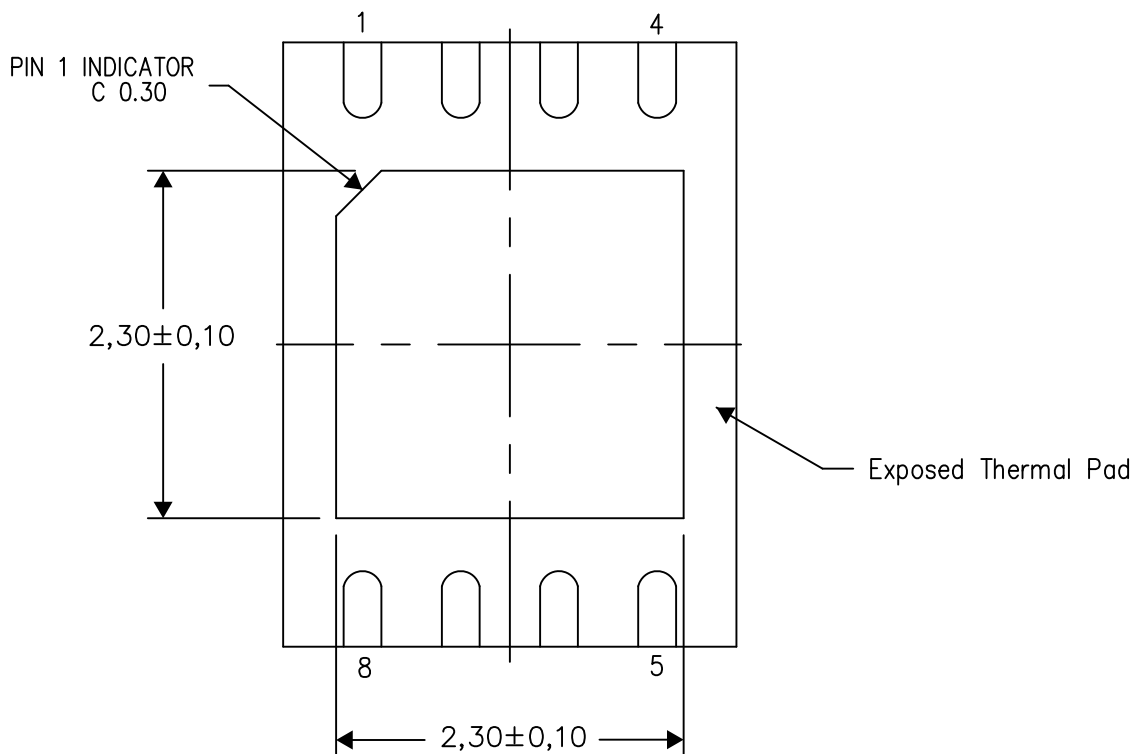
PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4212605/A 04/12

NOTE: All linear dimensions are in millimeters

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