

SBOS026A – JANUARY 1994 – REVISED APRIL 2007

## Ultra-Low Bias Current *Difet*<sup>®</sup> OPERATIONAL AMPLIFIER

### FEATURES

- ULTRA-LOW BIAS CURRENT: 100fA max
- LOW OFFSET: 2mV max
- LOW DRIFT: 10 $\mu$ V/°C max
- HIGH OPEN-LOOP GAIN: 94dB min
- LOW NOISE: 15nV/ $\sqrt{\text{Hz}}$  at 10kHz
- PLASTIC DIP AND SO PACKAGES

### APPLICATIONS

- PHOTODETECTOR PREAMPS
- CHROMATOGRAPHY
- ELECTROMETER AMPLIFIERS
- MASS SPECTROMETERS
- pH PROBE AMPLIFIERS
- ION GAGE MEASUREMENT

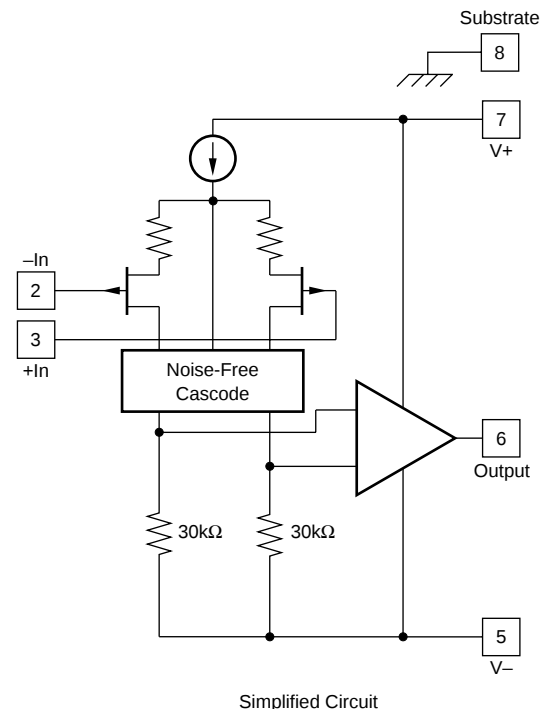
### DESCRIPTION

The OPA129 is an ultra-low bias current monolithic operational amplifier offered in an 8-pin PDIP and SO-8 package. Using advanced geometry dielectrically-isolated FET (*Difet*<sup>®</sup>) inputs, this monolithic amplifier achieves a high performance level.

*Difet* fabrication eliminates isolation-junction leakage current—the main contributor to input bias current with conventional monolithic FETs. This reduces input bias current by a factor of 10 to 100. Very low input bias current can be achieved without resorting to small-geometry FETs or CMOS designs which can suffer from much larger offset voltage, voltage noise, drift, and poor power-supply rejection.

The OPA129 special pinout eliminates leakage current that occurs with other op amps. Pins 1 and 4 have no internal connection, allowing circuit board guard traces—even with the surface-mount package version.

OPA129 is available in 8-pin DIP and SO packages, specified for operation from –40°C to +85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

*Difet* is a registered trademark of Texas Instruments.  
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# SPECIFICATIONS

## ELECTRICAL

At  $V_S = \pm 15V$  and  $T_A = +25^\circ C$ , unless otherwise noted. Pin 8 connected to ground.

| PARAMETER                                                                                                                                                                       | CONDITION                                                                                                                      | OPA129PB, UB        |                                                |                                  | OPA129P, U  |                                |              | UNITS                                                                                                  |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------|---------------------|------------------------------------------------|----------------------------------|-------------|--------------------------------|--------------|--------------------------------------------------------------------------------------------------------|
|                                                                                                                                                                                 |                                                                                                                                | MIN                 | TYP                                            | MAX                              | MIN         | TYP                            | MAX          |                                                                                                        |
| <b>INPUT BIAS CURRENT<sup>(1)</sup></b><br>vs Temperature                                                                                                                       | $V_{CM} = 0V$                                                                                                                  |                     | $\pm 30$                                       | $\pm 100$                        |             | *                              | $\pm 250$    | fA                                                                                                     |
|                                                                                                                                                                                 |                                                                                                                                |                     | Doubles every $10^\circ C$                     |                                  |             | *                              |              |                                                                                                        |
| <b>INPUT OFFSET CURRENT</b>                                                                                                                                                     | $V_{CM} = 0V$                                                                                                                  |                     | $\pm 30$                                       |                                  |             | *                              |              | fA                                                                                                     |
| <b>OFFSET VOLTAGE</b><br>Input Offset Voltage<br>vs Temperature<br>Supply Rejection                                                                                             | $V_{CM} = 0V$<br><br>$V_S = \pm 5V$ to $\pm 18V$                                                                               |                     | $\pm 0.5$<br>$\pm 3$<br>$\pm 3$                | $\pm 2$<br>$\pm 10$<br>$\pm 100$ |             | $\pm 1$<br>$\pm 5$<br>*        | $\pm 5$<br>* | mV<br>$\mu V/^\circ C$<br>$\mu V/V$                                                                    |
| <b>NOISE</b><br>Voltage<br><br><br>Current                                                                                                                                      | $f = 10Hz$<br>$f = 100Hz$<br>$f = 1kHz$<br>$f = 10kHz$<br>$f_B = 0.1Hz$ to $10Hz$<br>$f = 10kHz$                               |                     | 85<br>28<br>17<br>15<br>4<br>0.1               |                                  |             | *<br>*<br>*<br>*<br>*<br>*     |              | $nV/\sqrt{Hz}$<br>$nV/\sqrt{Hz}$<br>$nV/\sqrt{Hz}$<br>$nV/\sqrt{Hz}$<br>$\mu V_{PP}$<br>$fA/\sqrt{Hz}$ |
| <b>INPUT IMPEDANCE</b><br>Differential<br>Common-Mode                                                                                                                           |                                                                                                                                |                     | $10^{13} \parallel 1$<br>$10^{15} \parallel 2$ |                                  |             | *<br>*                         |              | $\Omega \parallel pF$<br>$\Omega \parallel pF$                                                         |
| <b>VOLTAGE RANGE</b><br>Common-Mode Input Range<br>Common-Mode Rejection                                                                                                        | $V_{IN} = \pm 10V$                                                                                                             | $\pm 10$<br>80      | $\pm 12$<br>118                                |                                  | *<br>*      | *<br>*                         |              | V<br>dB                                                                                                |
| <b>OPEN-LOOP GAIN, DC</b><br>Open-Loop Voltage Gain                                                                                                                             | $R_L \geq 2k\Omega$                                                                                                            | 94                  | 120                                            |                                  | *           | *                              |              | dB                                                                                                     |
| <b>FREQUENCY RESPONSE</b><br>Unity Gain, Small Signal<br>Full Power Response<br>Slew Rate<br>Settling Time:<br>0.1%<br>0.01%<br>Overload Recovery, 50% Overdrive <sup>(2)</sup> | $20V_{p-p}$ , $R_L = 2k\Omega$<br>$V_O = \pm 10V$ , $R_L = 2k\Omega$<br>$G = -1$ , $R_L = 2k\Omega$ , 10V Step<br><br>$G = -1$ | 1                   | 1<br>47<br>2.5<br><br>5<br>10<br>5             |                                  | *           | *<br>*<br>*<br><br>*<br>*<br>* |              | MHz<br>kHz<br>V/ $\mu s$<br><br>$\mu s$<br>$\mu s$<br>$\mu s$                                          |
| <b>RATED OUTPUT</b><br>Voltage Output<br>Current Output<br>Load Capacitance Stability<br>Short-Circuit Current                                                                  | $R_L = 2k\Omega$<br>$V_O = \pm 12V$<br>Gain = +1                                                                               | $\pm 12$<br>$\pm 6$ | $\pm 13$<br>$\pm 10$<br>1000<br>$\pm 35$       | $\pm 55$                         | *<br>*      | *<br>*<br>*<br>*               | *            | V<br>mA<br>pF<br>mA                                                                                    |
| <b>POWER SUPPLY</b><br>Rated Voltage<br>Voltage Range, Derated Performance<br>Current, Quiescent                                                                                | $I_O = 0mA$                                                                                                                    | $\pm 5$             | $\pm 15$<br>1.2                                | $\pm 18$<br>1.8                  | *           | *<br>*                         | *<br>*       | V<br>V<br>mA                                                                                           |
| <b>TEMPERATURE</b><br>Specification<br>Operating<br>Storage<br>Thermal Resistance<br>DIP-8<br>SO-8                                                                              | Ambient Temperature<br>Ambient Temperature<br><br>$\theta_{JA}$ , Junction-to-Ambient                                          | -40<br>-40<br>-40   |                                                | +85<br>+125<br>+125              | *<br>*<br>* |                                | *<br>*<br>*  | $^\circ C$<br>$^\circ C$<br>$^\circ C$<br><br>$^\circ C/W$<br>$^\circ C/W$                             |

NOTES: (1) High-speed automated test.

(2) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive.

## ABSOLUTE MAXIMUM RATINGS

|                                                    |                                  |
|----------------------------------------------------|----------------------------------|
| Power Supply Voltage .....                         | ±18V                             |
| Differential Input Voltage .....                   | V <sup>-</sup> to V <sup>+</sup> |
| Input Voltage Range .....                          | V <sup>-</sup> to V <sup>+</sup> |
| Storage Temperature Range .....                    | -40°C to +125°C                  |
| Operating Temperature Range .....                  | -40°C to +125°C                  |
| Output Short Circuit Duration <sup>(1)</sup> ..... | Continuous                       |
| Junction Temperature (T <sub>J</sub> ) .....       | +150°C                           |

NOTE: (1) Short circuit may be to power supply common at +25°C ambient.



## ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

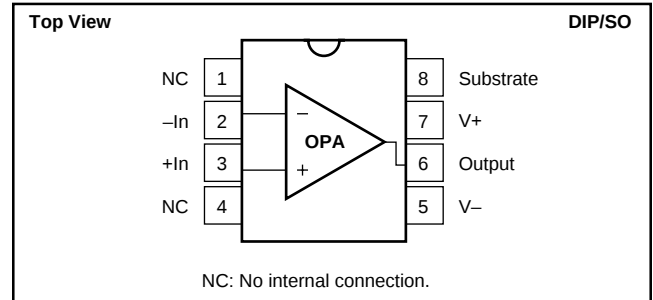
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PACKAGE INFORMATION<sup>(1)</sup>

| PRODUCT  | PACKAGE-LEAD | PACKAGE DESIGNATOR |
|----------|--------------|--------------------|
| OPA129P  | DIP-8        | P                  |
| OPA129PB | DIP-8        | P                  |
| OPA129U  | SO-8         | D                  |
| OPA129UB | SO-8         | D                  |

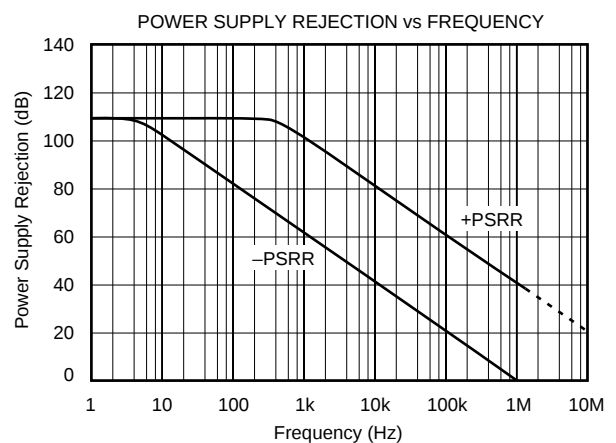
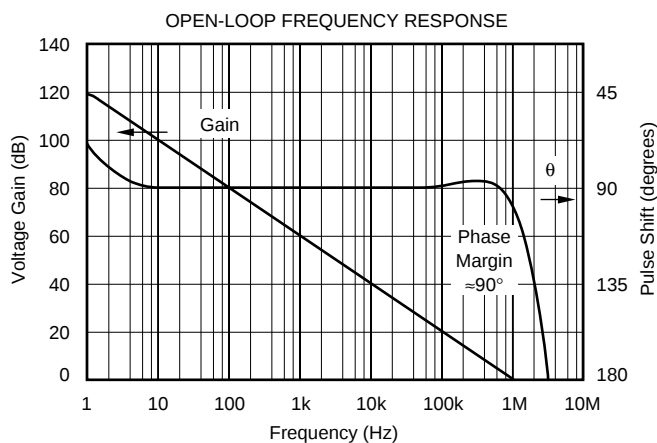
NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at [www.ti.com](http://www.ti.com).

## CONNECTION DIAGRAM



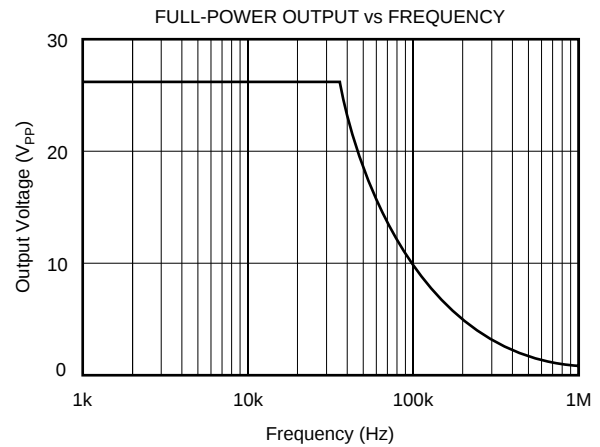
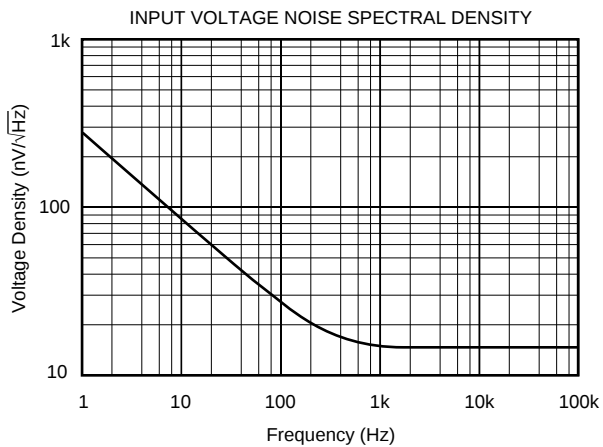
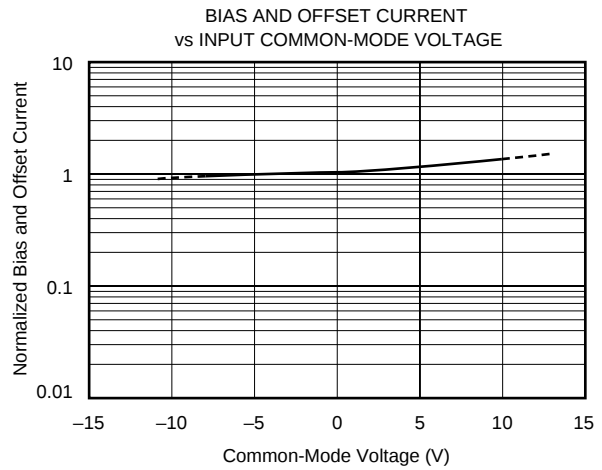
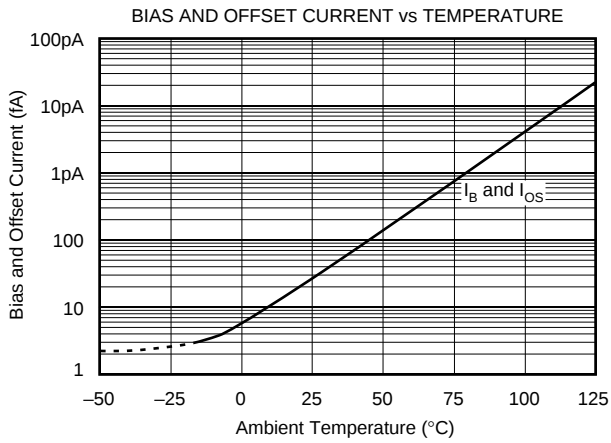
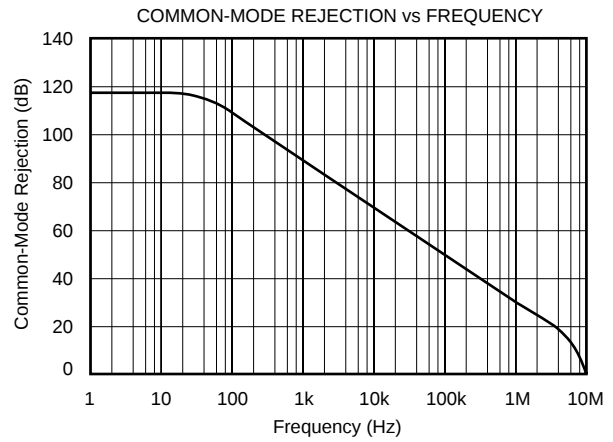
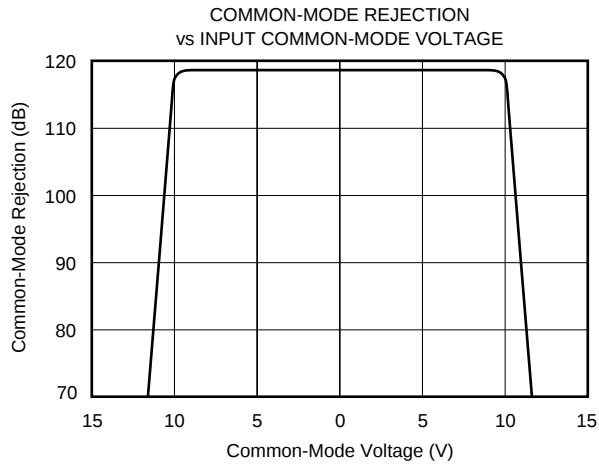
## TYPICAL PERFORMANCE CURVES

At T<sub>A</sub> = +25°C, +15VDC, unless otherwise noted.



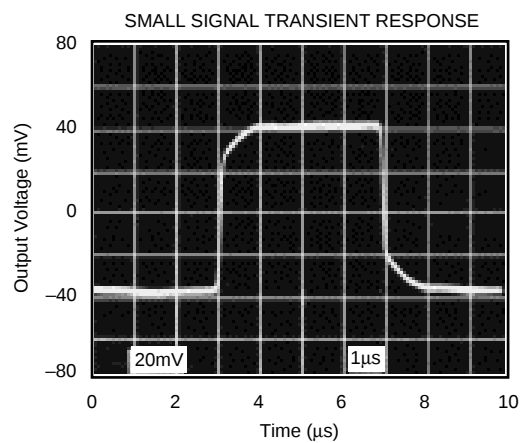
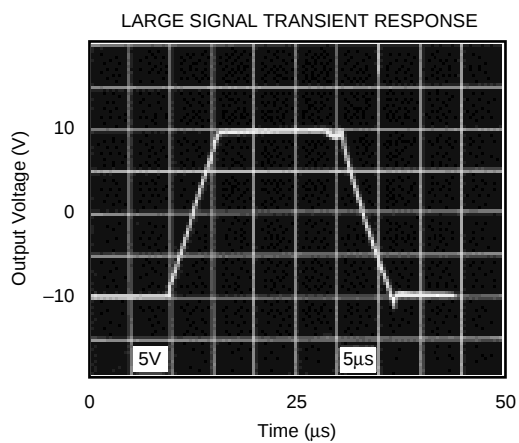
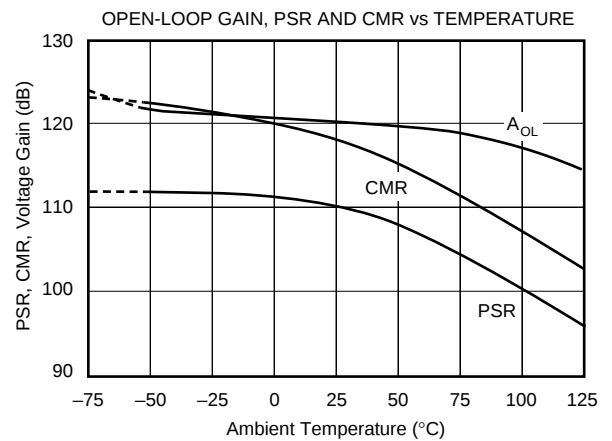
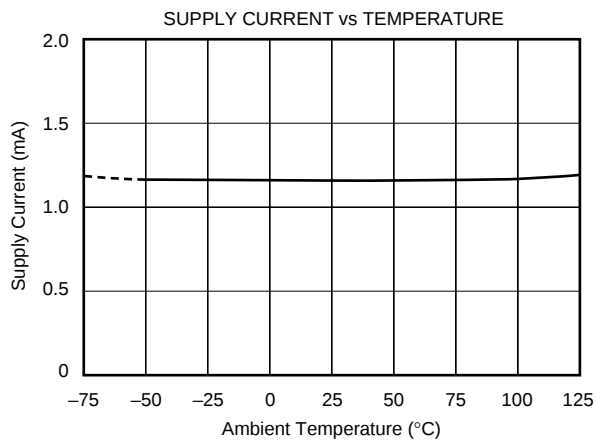
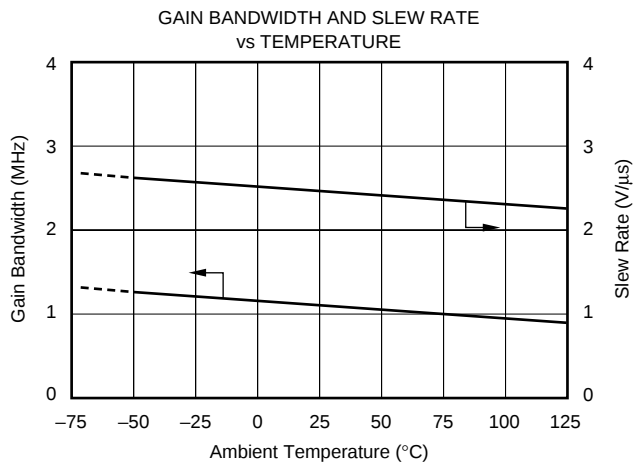
# TYPICAL PERFORMANCE CURVES (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $+15\text{VDC}$ , unless otherwise noted.



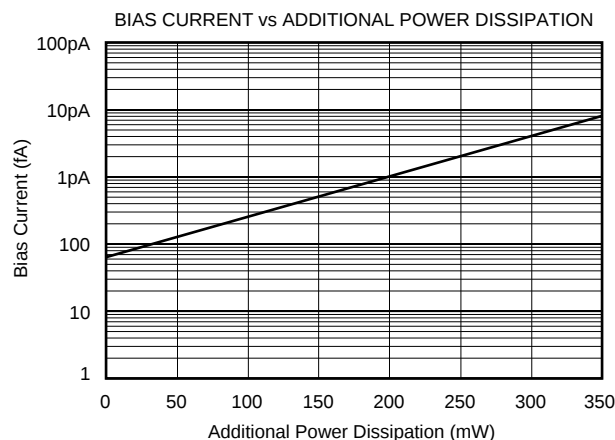
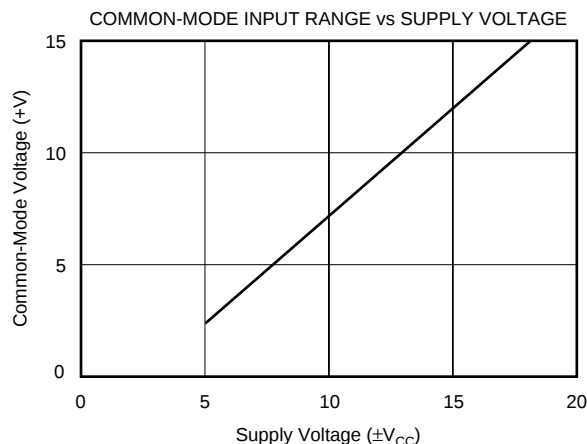
# TYPICAL PERFORMANCE CURVES (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $+15\text{VDC}$ , unless otherwise noted.



# TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$ , +15VDC, unless otherwise noted.



## APPLICATIONS INFORMATION

### NON-STANDARD PINOUT

The OPA129 uses a non-standard pinout to achieve lowest possible input bias current. The negative power supply is connected to pin 5—see Figure 1. This is done to reduce the leakage current from the V<sup>-</sup> supply (pin 4 on conventional op amps) to the op amp input terminals. With this new pinout, sensitive inputs are separated from both power supply pins.

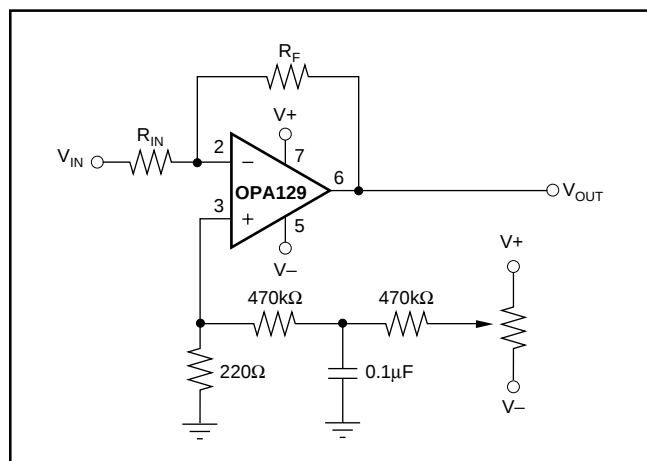


FIGURE 1. Offset Adjust Circuit.

### OFFSET VOLTAGE TRIM

The OPA129 has no conventional offset trim connections. Pin 1, next to the critical inverting input, has no internal connection. This eliminates a source of leakage current and allows guarding of the input terminals. Pin 1 and pin 4, next to the two input pins, have no internal connection. This allows an optimized circuit board layout with guarding—see the *Circuit Board Layout* section.

Due to its laser-trimmed input stage, most applications do not require external offset voltage trimming. If trimming is required, the circuit shown in Figure 1 can be used. Power supply voltages are divided down, filtered and applied to the non-inverting input. The circuit shown is sensitive to variation in the supply voltages. Regulation can be added, if needed.

### GUARDING AND SHIELDING

Ultra-low input bias current op amps require precautions to achieve best performance. Leakage current on the surface of circuit board can exceed the input bias current of the amplifier. For example, a circuit board resistance of  $10^{12}\Omega$  from a power supply pin to an input pin produces a current of 15pA—more than 100 times the input bias current of the op amp.

To minimize surface leakage, a guard trace should completely surround the input terminals and other circuitry connecting to the inputs of the op amp. The DIP package should have a guard trace on both sides of the circuit board. The guard ring should be driven by a circuit node equal in potential to the op amp inputs—see Figure 2. The substrate, pin 8, should also be connected to the circuit board guard to assure that the amplifier is fully surrounded by the guard potential. This minimizes leakage current and noise pick-up.

Careful shielding is required to reduce noise pickup. Shielding near feedback components may also help reduce noise pick-up.

Triboelectric effects (friction-generated charge) can be a troublesome source of errors. Vibration of the circuit board, input connectors and input cables can cause noise and drift. Make the assembly as rigid as possible. Attach cables to avoid motion and vibration. Special low noise or low leakage cables may help reduce noise and leakage current. Keep all input connections as short possible. Surface-mount components may reduce circuit board size and allow a more rigid assembly.

## CIRCUIT BOARD LAYOUT

The OPA129 uses a new pinout for ultra low input bias current. Pin 1 and pin 4 have no internal connection. This allows ample circuit board space for a guard ring surrounding the op amp input pins—even with the tiny SO-8 surface-mount package. Figure 3 shows suggested circuit board layouts. The guard ring should be connected to pin 8 (substrate) as shown. It should be driven by a circuit node equal in potential to the input terminals of the op amp—see Figure 2 for common circuit configurations.

## TESTING

Accurately testing the OPA129 is extremely difficult due to its high performance. Ordinary test equipment may not be able to resolve the amplifier's extremely low bias current. Inaccurate bias current measurements can be due to:

1. Test socket leakage.
2. Unclean package.
3. Humidity or dew point condensations.
4. Circuit contamination from fingerprints or anti-static treatment chemicals.
5. Test ambient temperature.
6. Load power dissipation.
7. Mechanical stress.
8. Electrostatic and electromagnetic interference.

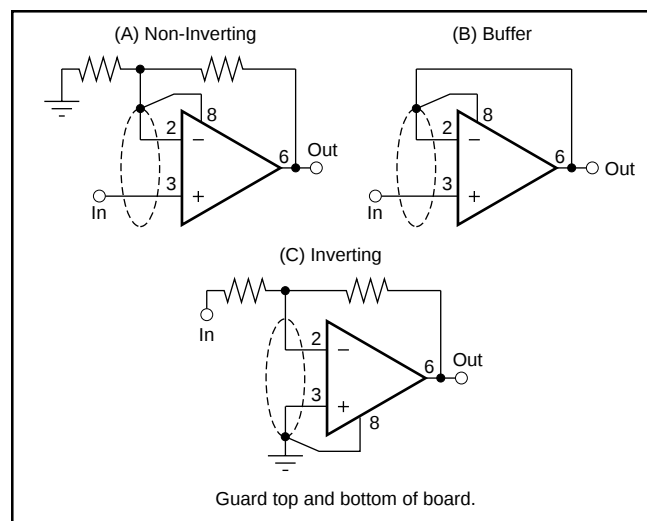


FIGURE 2. Connection of Input Guard.

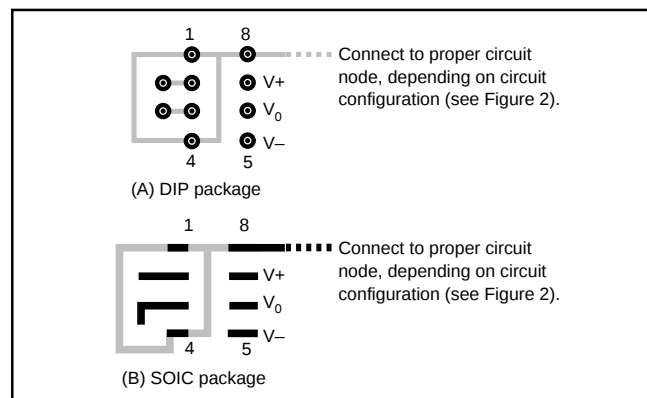


FIGURE 3. Suggested Board Layout for Input Guard.

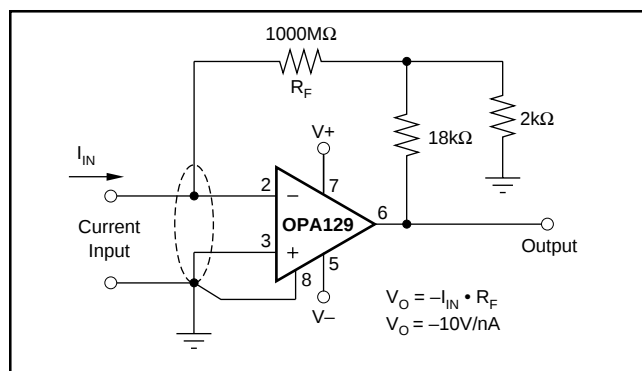


FIGURE 4. Current-to-Voltage Converter.

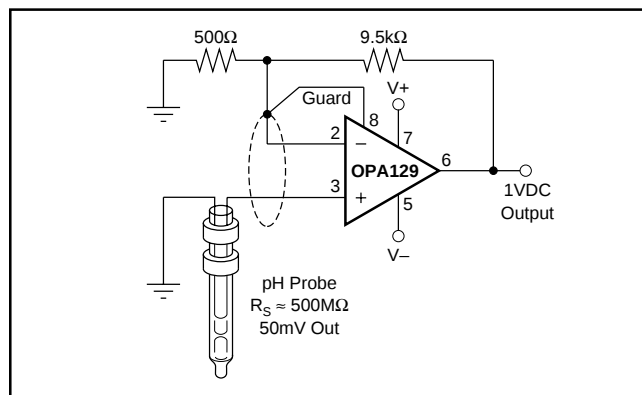


FIGURE 5. High Impedance ( $10^{15}\Omega$ ) Amplifier.

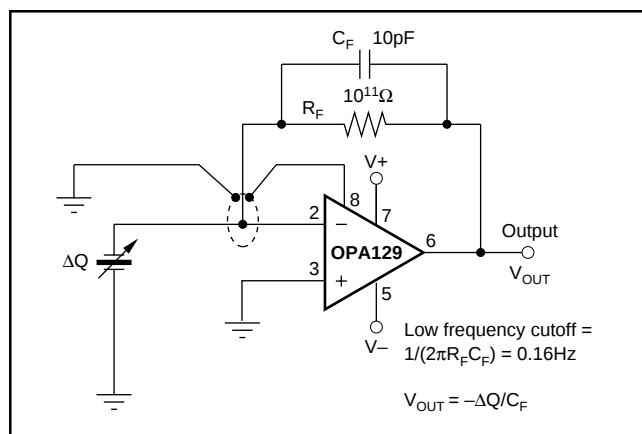


FIGURE 6. Piezoelectric Transducer Charge Amplifier.

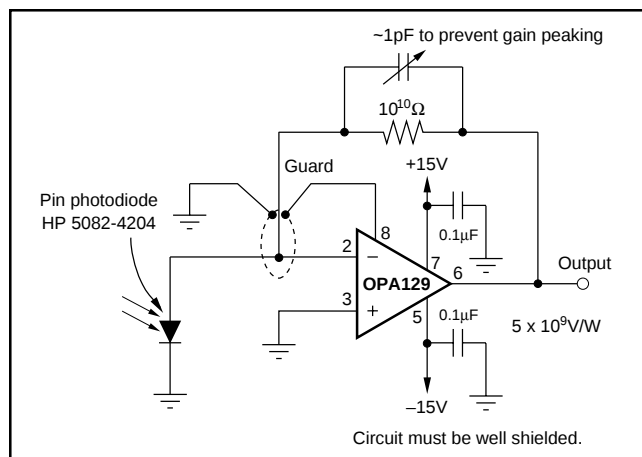


FIGURE 7. Sensitive Photodiode Amplifier.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| OPA129P          | OBSOLETE      | PDIP         | P                  | 8    |                | TBD                        | Call TI                 | Call TI              |              |                         |                         |
| OPA129PB         | OBSOLETE      | PDIP         | P                  | 8    |                | TBD                        | Call TI                 | Call TI              |              |                         |                         |
| OPA129U          | ACTIVE        | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 125   | OPA<br>129U             | <a href="#">Samples</a> |
| OPA129UB         | ACTIVE        | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 125   | OPA<br>129U<br>B        | <a href="#">Samples</a> |
| OPA129UB/2K5     | ACTIVE        | SOIC         | D                  | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 125   | OPA<br>129U<br>B        | <a href="#">Samples</a> |
| OPA129UBE4       | ACTIVE        | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 125   | OPA<br>129U<br>B        | <a href="#">Samples</a> |
| OPA129UBG4       | ACTIVE        | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 125   | OPA<br>129U<br>B        | <a href="#">Samples</a> |
| OPA129UE4        | ACTIVE        | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 125   | OPA<br>129U             | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

- <sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- <sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- <sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


|    |                                                           |
|----|-----------------------------------------------------------|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| OPA129UB/2K5 | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS

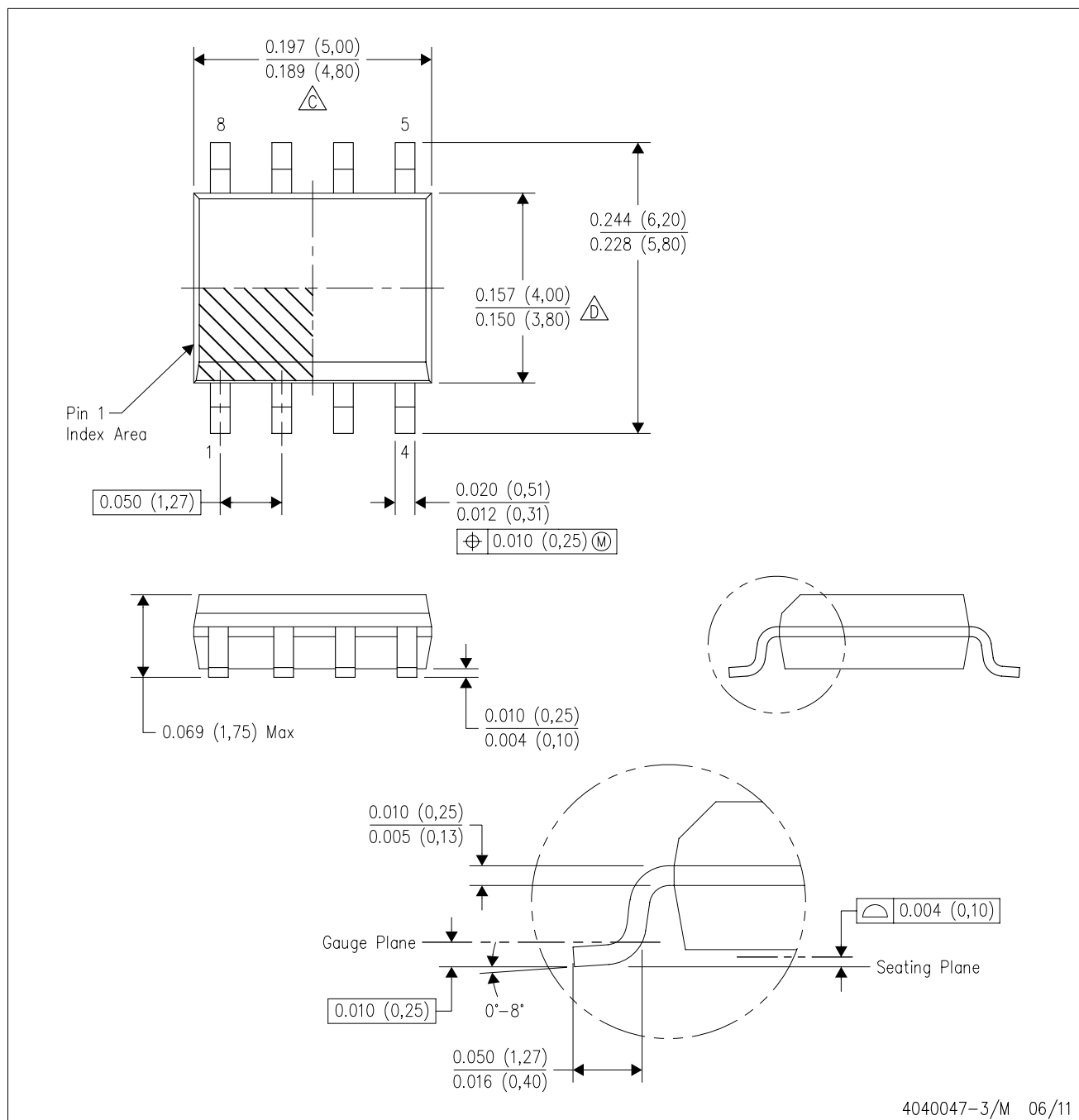


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| OPA129UB/2K5 | SOIC         | D               | 8    | 2500 | 367.0       | 367.0      | 35.0        |

D (R-PDSO-G8)

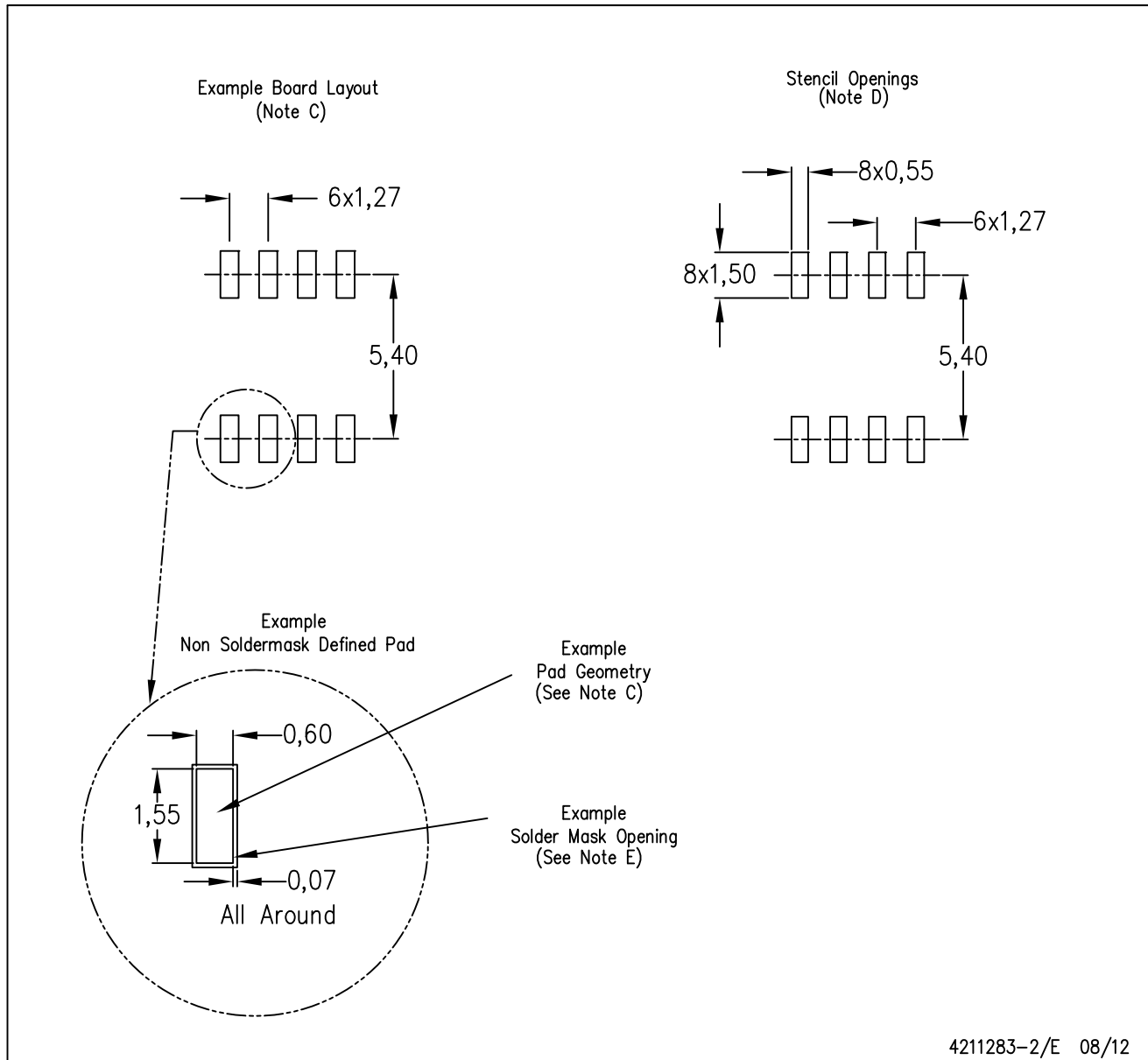
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

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