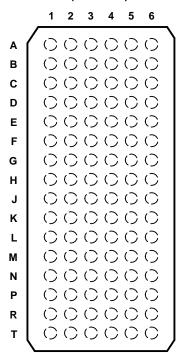




### **FEATURES**

- Member of the Texas Instruments Widebus+™
   Family
- Operates From 2.7 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t<sub>pd</sub> of 3.7 ns at 3.3 V
- I<sub>off</sub> and Power-Up 3-State Support Hot Insertion

GKE PACKAGE (TOP VIEW)



- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V<sub>CC</sub>)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

### **TERMINAL ASSIGNMENTS**

	1	2	3	4	5	6
Α	1B2	1B1	1DIR	1 <del>OE</del>	1A1	1A2
В	1B4	1B3	GND	GND	1A3	1A4
С	1B6	1B5	$V_{CC}$	V <sub>CC</sub>	1A5	1A6
D	1B8	1B7	GND	GND	1A7	1A8
Е	2B2	2B1	GND	GND	2A1	2A2
F	2B4	2B3	$V_{CC}$	V <sub>CC</sub>	2A3	2A4
G	2B6	2B5	GND	GND	2A5	2A6
Н	2B7	2B8	2DIR	2 <del>OE</del>	2A8	2A7
J	3B2	3B1	3DIR	3 <del>OE</del>	3A1	3A2
K	3B4	3B3	GND	GND	3A3	3A4
L	3B6	3B5	$V_{CC}$	V <sub>CC</sub>	3A5	3A6
М	3B8	3B7	GND	GND	3A7	3A8
N	4B2	4B1	GND	GND	4A1	4A2
Р	4B4	4B3	V <sub>CC</sub>	V <sub>CC</sub>	4A3	4A4
R	4B6	4B5	GND	GND	4A5	4A6
Т	4B7	4B8	4DIR	4 <del>OE</del>	4A8	4A7

## **DESCRIPTION/ORDERING INFORMATION**

This 32-bit (quad-octal) noninverting bus transceiver is designed for 2.7-V to 3.6-V V<sub>CC</sub> operation.

The SN74LVCZ32245A is designed for asynchronous communication between data buses. The control-function implementation minimizes external timing requirements.

## **ORDERING INFORMATION**

T <sub>A</sub>	PACK	AGE <sup>(1)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	LFBGA – GKE	Tape and reel	SN74LVCZ32245AGKER	ZC245A

 Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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SCES423-JANUARY 2003-REVISED JUNE 2005



## DESCRIPTION/ORDERING INFORMATION (CONTINUED)

This device can be used as four 8-bit transceivers, two 16-bit transceivers, or one 32-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable  $(\overline{OE})$  input can be used to disable the device so that the buses effectively are isolated.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

When  $V_{CC}$  is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using  $I_{\text{off}}$  and power-up 3-state. The  $I_{\text{off}}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

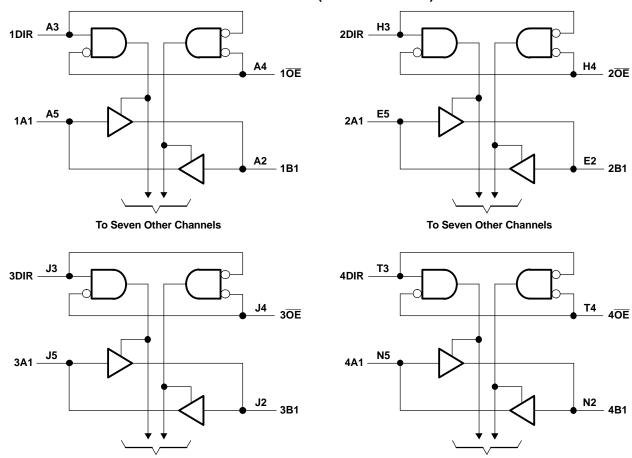
# FUNCTION TABLE (EACH 8-BIT SECTION)

INP	UTS	OPERATION
ŌΕ	DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	Χ	Isolation

To Seven Other Channels



## **LOGIC DIAGRAM (POSITIVE LOGIC)**



# Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

To Seven Other Channels

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage range		-0.5	6.5	V
VI	Input voltage range (2)		-0.5	6.5	V
Vo	Voltage range applied to any output in t	Itage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>			
Vo	Voltage range applied to any output in t	tage range applied to any output in the high or low state (2)(3)			
I <sub>IK</sub>	Input clamp current	V <sub>1</sub> < 0		<b>–</b> 50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		<b>–</b> 50	mA
Io	Continuous output current			±50	mA
	Continuous current through each V <sub>CC</sub> o	r GND		±100	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	Package thermal impedance <sup>(4)</sup>			
T <sub>stg</sub>	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

# **SN74LVCZ32245A 32-BIT BUS TRANSCEIVER** WITH 3-STATE OUTPUTS

SCES423-JANUARY 2003-REVISED JUNE 2005



# Recommended Operating Conditions<sup>(1)</sup>

			MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage		2.7	3.6	V	
$V_{IH}$	High-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		V	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		8.0	V	
VI	Input voltage		0	5.5	V	
V	Output valtage	High or low state	0	$V_{CC}$	V	
Vo	Output voltage	3-state	0	5.5	V	
	I limb lavel autout august	V <sub>CC</sub> = 2.7 V		-12	A	
IOH	Output voltage  High-level output current	V <sub>CC</sub> = 3 V		-24	mA	
	Landard autout annual	V <sub>CC</sub> = 2.7 V		12	1	
I <sub>OL</sub>		V <sub>CC</sub> = 3 V		24	mA	
Δt/Δν	Input transition rise or fall rate			6	ns/V	
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		150		μs/V	
T <sub>A</sub>	Operating free-air temperature		-40	85	°C	

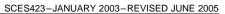
All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## **Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITION	IS	V <sub>cc</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT	
	$I_{OH} = -100 \mu A$		2.7 V to 3.6 V	V <sub>CC</sub> - 0.2				
	1. 40		2.7 V	2.2			V	
V <sub>OH</sub>	$I_{OH} = -12 \text{ mA}$		3 V	2.4			V	
	I <sub>OH</sub> = -24 mA		3 V	2.2				
	I <sub>OL</sub> = 100 μA		2.7 V to 3.6 V			0.2		
V <sub>OL</sub>	I <sub>OL</sub> = 12 mA	I <sub>OL</sub> = 12 mA					V	
	I <sub>OL</sub> = 24 mA	3 V			0.55			
I <sub>I</sub> Control inputs	V <sub>I</sub> = 0 to 5.5 V	3.6 V			±5	μΑ		
l <sub>off</sub>	$V_I$ or $V_O = 5.5 \text{ V}$		0			±5	μΑ	
I <sub>OZ</sub> <sup>(2)</sup>	V <sub>O</sub> = 0 to 5.5 V		3.6 V			±5	μΑ	
I <sub>OZPU</sub>	V <sub>O</sub> = 0.5 V to 2.5 V,	OE = don't care	0 to 1.5 V			±5	μΑ	
I <sub>OZPD</sub>	V <sub>O</sub> = 0.5 V to 2.5 V,	OE = don't care	1.5 V to 0			±5	μΑ	
1	V <sub>I</sub> = V <sub>CC</sub> or GND		261/			120	^	
Icc	$3.6 \text{ V} \le \text{V}_{\text{I}} \le 5.5 \text{ V}^{(3)}$	I <sub>O</sub> = 0	3.6 V	120			μΑ	
Δl <sub>CC</sub>	One input at V <sub>CC</sub> – 0.6 V, Other input	s at V <sub>CC</sub> or GND	2.7 V to 3.6 V			500	μΑ	
C <sub>i</sub> Control inputs	$C_i$ Control inputs $V_I = V_{CC}$ or GND		3.3 V		5		pF	
C <sub>io</sub> A or B ports	$V_O = V_{CC}$ or GND		3.3 V		6.5		pF	

All typical values are at V $_{\rm CC}$  = 3.3 V, T $_{\rm A}$  = 25°C. For I/O ports, the parameter I $_{\rm OZ}$  includes the input leakage current. This applies in the disabled state only.





# **Switching Characteristics**

over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 2	2.7 V	V <sub>CC</sub> = 3 ± 0.3	UNIT	
	(INPOT)	(001701)	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	B or A		4.2	1.3	4	ns
t <sub>en</sub>	ŌĒ	A or B		6.1	1.4	5.6	ns
t <sub>dis</sub>	ŌĒ	A or B		7.1	2	6.6	ns

## **Switching Characteristics**

over recommended operating free-air temperature range,  $C_L = 30 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO	V <sub>CC</sub> = 2	2.7 V	V <sub>CC</sub> = 3 ± 0.3	UNIT	
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	B or A		3.9	1	3.7	ns
t <sub>en</sub>	ŌĒ	A or B		5.9	1.1	5.4	ns
t <sub>dis</sub>	ŌĒ	A or B		6.7	1.6	6.2	ns

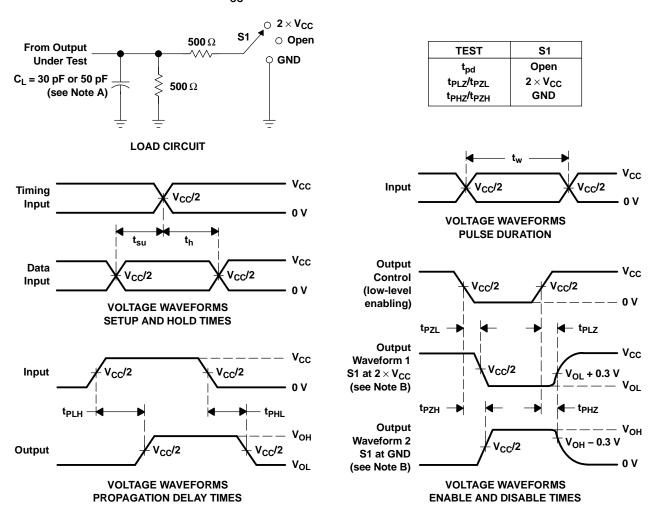
# **Operating Characteristics**

 $T_A = 25^{\circ}C$ 

ſ	Α	PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 3.3 V TYP	UNIT
Ī	C	Power dissipation capacitance per transceiver	Outputs enabled	f = 10 MHz	42	pF
	$C_{pd}$	rower dissipation capacitance per transceiver	Outputs disabled	I = IO WINZ	4	рг



# PARAMETER MEASUREMENT INFORMATION $V_{cc}$ = 2.7 V AND 3.3 V $\pm$ 0.3 V



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O$  = 50  $\Omega$ ,  $t_f \leq$  2 ns.
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - G. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>.
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



## PACKAGE OPTION ADDENDUM

11-Apr-2013

#### PACKAGING INFORMATION

Orderable Device	Status	Package Type	U	Pins	U	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
	(1)		Drawing		Qty	(2)		(3)		(4)	
SN74LVCZ32245AGKER	NRND	LFBGA	GKE	96	1000	TBD	SNPB	Level-2-235C-1 YEAR	-40 to 85	ZC245A	
SN74LVCZ32245AZKER	ACTIVE	LFBGA	ZKE	96	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	ZC245A	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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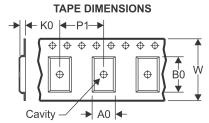
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# PACKAGE MATERIALS INFORMATION

www.ti.com 19-May-2016

## TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

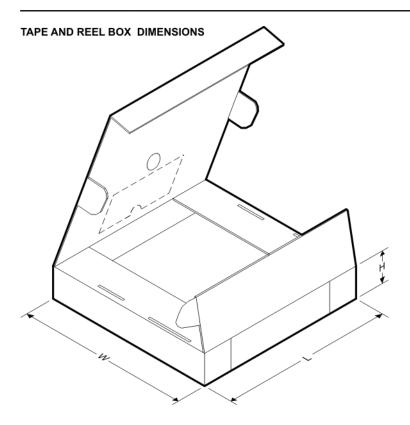


### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCZ32245AGKER	LFBGA	GKE	96	1000	330.0	24.4	5.7	13.7	2.0	8.0	24.0	Q1
SN74LVCZ32245AZKER	LFBGA	ZKE	96	1000	330.0	24.4	5.7	13.7	2.0	8.0	24.0	Q1

**PACKAGE MATERIALS INFORMATION** 

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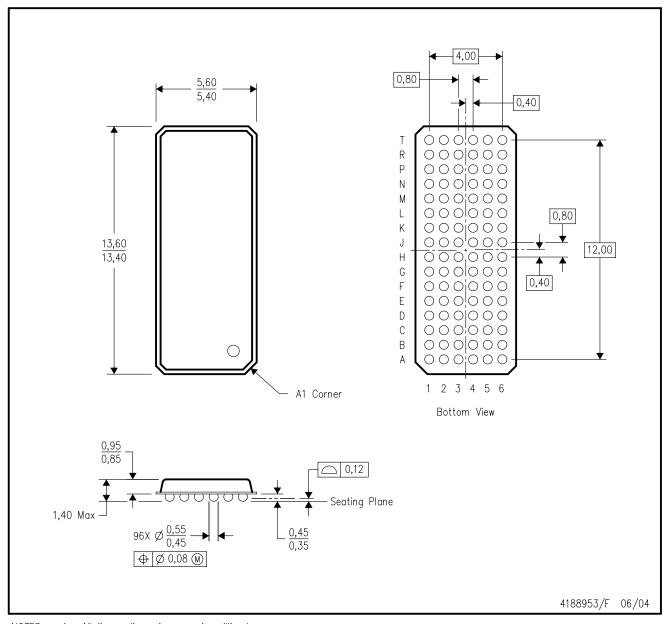


### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCZ32245AGKER	LFBGA	GKE	96	1000	336.6	336.6	41.3
SN74LVCZ32245AZKER	LFBGA	ZKE	96	1000	336.6	336.6	41.3

# GKE (R-PBGA-N96)

# PLASTIC BALL GRID ARRAY



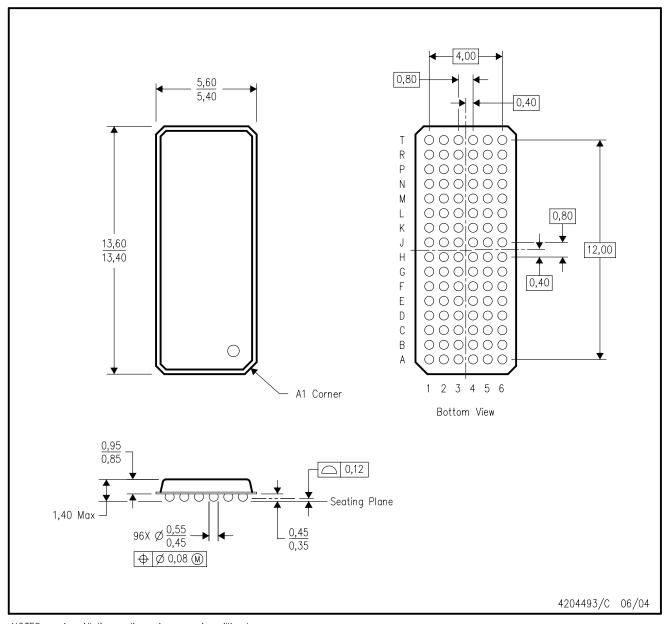
NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-205 variation CC.
- D. This package is tin-lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead-free.



# ZKE (R-PBGA-N96)

# PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-205 variation CC.
- D. This package is lead-free. Refer to the 96 GKE package (drawing 4188953) for tin-lead (SnPb).



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