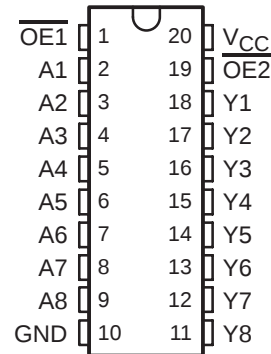


- **Controlled Baseline**
  - One Assembly/Test Site, One Fabrication Site
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree<sup>†</sup>**
- **State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**

<sup>†</sup> Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- **Typical  $V_{OLP}$  (Output Ground Bounce) <1 V** at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$
- **High-Impedance State During Power Up and Power Down**
- **High-Drive Outputs ( $\sim 32\text{-mA } I_{OH}$ ,  $64\text{-mA } I_{OL}$ )**

**PW PACKAGE**  
(TOP VIEW)



## description/ordering information

The SN74ABT541B octal buffer and line driver is ideal for driving bus lines or buffering memory address registers. The device features inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a two-input AND gate with active-low inputs so that if either output-enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all eight outputs are in the high-impedance state.

When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## ORDERING INFORMATION

| $T_A$                                     | PACKAGE <sup>‡</sup> |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|-------------------------------------------|----------------------|---------------|-----------------------|------------------|
| $-40^\circ\text{C}$ to $85^\circ\text{C}$ | TSSOP – PW           | Tape and reel | SN74ABT541BIPWREP     | ABT541EP         |

<sup>‡</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

**FUNCTION TABLE**

| INPUTS           |                  |   | OUTPUT<br>Y |
|------------------|------------------|---|-------------|
| $\overline{OE1}$ | $\overline{OE2}$ | A |             |
| L                | L                | L | L           |
| L                | L                | H | H           |
| H                | X                | X | Z           |
| X                | H                | X | Z           |



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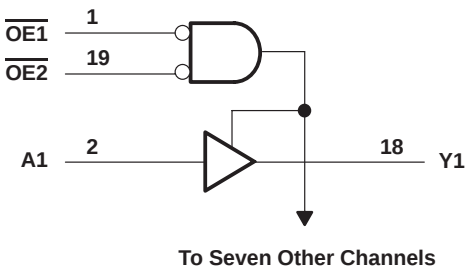
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SN74ABT541B-EP
OCTAL BUFFER/DRIVER
WITH 3-STATE OUTPUTS

SCBS797 – JANUARY 2004

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                           |                 |
|---------------------------------------------------------------------------|-----------------|
| Supply voltage range, $V_{CC}$                                            | −0.5 V to 7 V   |
| Input voltage range, $V_I$ (see Note 1)                                   | −0.5 V to 7 V   |
| Voltage range applied to any output in the high or power-off state, $V_O$ | −0.5 V to 5.5 V |
| Current into any output in the low state, $I_O$                           | 128 mA          |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )                               | −18 mA          |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ )                              | −50 mA          |
| Package thermal impedance, $\theta_{JA}$ (see Note 2)                     | 128°C/W         |
| Storage temperature range, $T_{stg}$                                      | −65°C to 150°C  |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
- The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  - The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

|                                      | MIN | MAX | UNIT |
|--------------------------------------|-----|-----|------|
| $V_{CC}$ Supply voltage              | 4.5 | 5.5 | V    |
| $V_{IH}$ High-level input voltage    | 2   |     | V    |
| $V_{IL}$ Low-level input voltage     |     | 0.8 | V    |
| $I_{OH}$ High-level output current   |     | −32 | mA   |
| $I_{OL}$ Low-level output current    |     | 64  | mA   |
| $T_A$ Operating free-air temperature | −40 | 85  | °C   |

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER                     | TEST CONDITIONS                                                                           | T <sub>A</sub> = 25°C |                  |      | MIN  | MAX  | UNIT |
|-------------------------------|-------------------------------------------------------------------------------------------|-----------------------|------------------|------|------|------|------|
|                               |                                                                                           | MIN                   | TYP <sup>†</sup> | MAX  |      |      |      |
| V <sub>IK</sub>               | V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA                                          |                       |                  | -1.2 | -1.2 |      | V    |
| V <sub>OH</sub>               | V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA                                          | 2.5                   |                  |      | 2.5  |      | V    |
|                               | V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA                                            | 3                     |                  |      | 3    |      |      |
|                               | V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -32 mA                                         | 2                     |                  |      | 2    |      |      |
| V <sub>OL</sub>               | V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA                                          |                       |                  | 0.55 | 0.55 |      | V    |
| V <sub>hys</sub>              |                                                                                           | 100                   |                  |      |      |      | mV   |
| I <sub>I</sub>                | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND                          |                       | ±1               |      | ±1   |      | μA   |
| I <sub>OZPU</sub>             | V <sub>CC</sub> = 0 to 2.1 V, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{\text{OE}}$ = X |                       | ±50              |      | ±50  |      | μA   |
| I <sub>OZPD</sub>             | V <sub>CC</sub> = 2.1 V to 0, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{\text{OE}}$ = X |                       | ±50              |      | ±50  |      | μA   |
| I <sub>OZH</sub>              | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V                                           |                       | 10               |      | 10   |      | μA   |
| I <sub>OZL</sub>              | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V                                           |                       | -10              |      | -10  |      | μA   |
| I <sub>off</sub>              | V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V                             |                       | ±100             |      | ±100 |      | μA   |
| I <sub>CEX</sub>              | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V, Outputs high                             |                       | 50               |      | 50   |      | μA   |
| I <sub>O</sub> <sup>‡</sup>   | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V                                           | -50                   | -140             | -180 | -50  | -180 | mA   |
| I <sub>CC</sub>               | V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND      |                       | 5                | 250  |      | 250  | μA   |
|                               |                                                                                           |                       | 22               | 30   |      | 30   | mA   |
|                               |                                                                                           |                       | 1                | 250  |      | 250  | μA   |
| ΔI <sub>CC</sub> <sup>§</sup> | V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND       |                       | 1.5              |      |      | 1.5  | mA   |
|                               |                                                                                           |                       | 50               |      |      | 50   | μA   |
|                               |                                                                                           |                       | 1.5              |      |      | 1.5  | mA   |
| C <sub>i</sub>                | V <sub>I</sub> = 2.5 V or 0.5 V                                                           |                       | 3                |      |      |      | pF   |
| C <sub>O</sub>                | V <sub>O</sub> = 2.5 V or 0.5 V                                                           |                       | 6                |      |      |      | pF   |

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V.

<sup>‡</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>§</sup> This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V<sub>CC</sub> or GND.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)**

| PARAMETER                       | FROM (INPUT)           | TO (OUTPUT) | V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C |     |     | MIN | MAX | UNIT |
|---------------------------------|------------------------|-------------|----------------------------------------------|-----|-----|-----|-----|------|
|                                 |                        |             | MIN                                          | TYP | MAX |     |     |      |
| t <sub>PLH</sub>                | A                      | Y           | 1                                            | 2   | 3.2 | 1   | 3.6 | ns   |
| t <sub>PHL</sub>                |                        |             | 1                                            | 2.6 | 3.5 | 1   | 3.9 |      |
| t <sub>PZH</sub>                | $\overline{\text{OE}}$ | Y           | 2                                            | 3.5 | 4.5 | 2   | 4   | ns   |
| t <sub>PZL</sub>                |                        |             | 1.9                                          | 4   | 5.1 | 1.9 | 5.9 |      |
| t <sub>PHZ</sub>                | $\overline{\text{OE}}$ | Y           | 2.2                                          | 4.4 | 5.4 | 2.2 | 5.8 | ns   |
| t <sub>PLZ</sub>                |                        |             | 1.5                                          | 3   | 4   | 1.5 | 4.4 |      |
| t <sub>sk(o)</sub> <sup>¶</sup> |                        |             |                                              |     | 0.5 |     | 0.5 | ns   |

<sup>¶</sup> Skew between any two outputs of the same package switching in the same direction

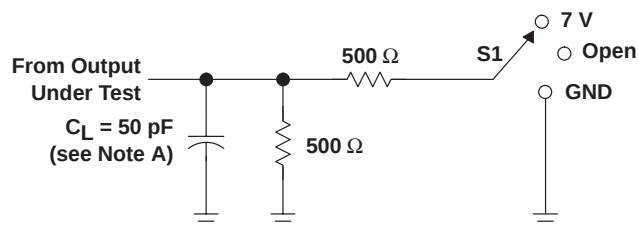
# SN74ABT541B-EP

## OCTAL BUFFER/DRIVER

### WITH 3-STATE OUTPUTS

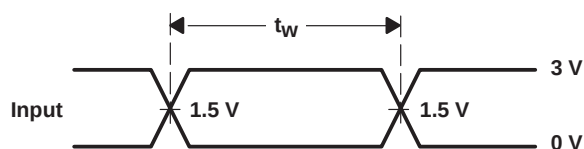
SCBS797 – JANUARY 2004

#### PARAMETER MEASUREMENT INFORMATION

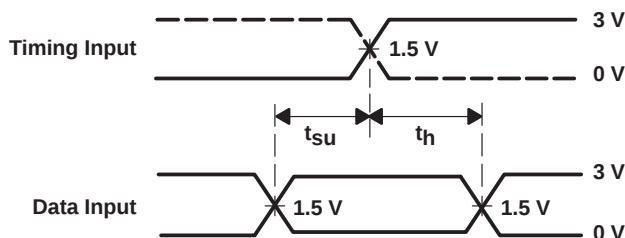


LOAD CIRCUIT

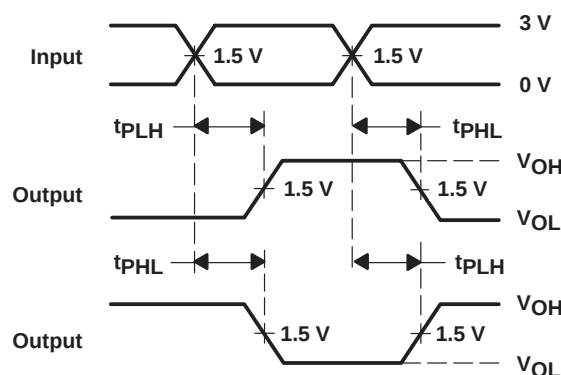
| TEST              | S1   |
|-------------------|------|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V  |
| $t_{PHZ}/t_{PZH}$ | Open |



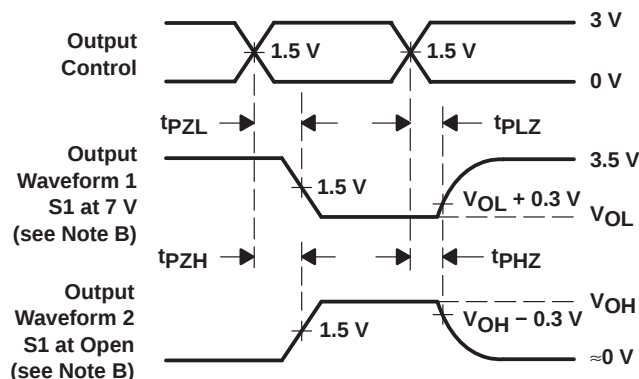
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

| Orderable Device  | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|-------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74ABT541BIPWREP | ACTIVE        | TSSOP        | PW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | ABT541EP                | <a href="#">Samples</a> |
| V62/04700-01XE    | ACTIVE        | TSSOP        | PW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | ABT541EP                | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74ABT541B-EP :**

- Catalog: [SN74ABT541B](#)
- Automotive: [SN74ABT541B-Q1](#)

**NOTE:** Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ABT541BIPWREP | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS

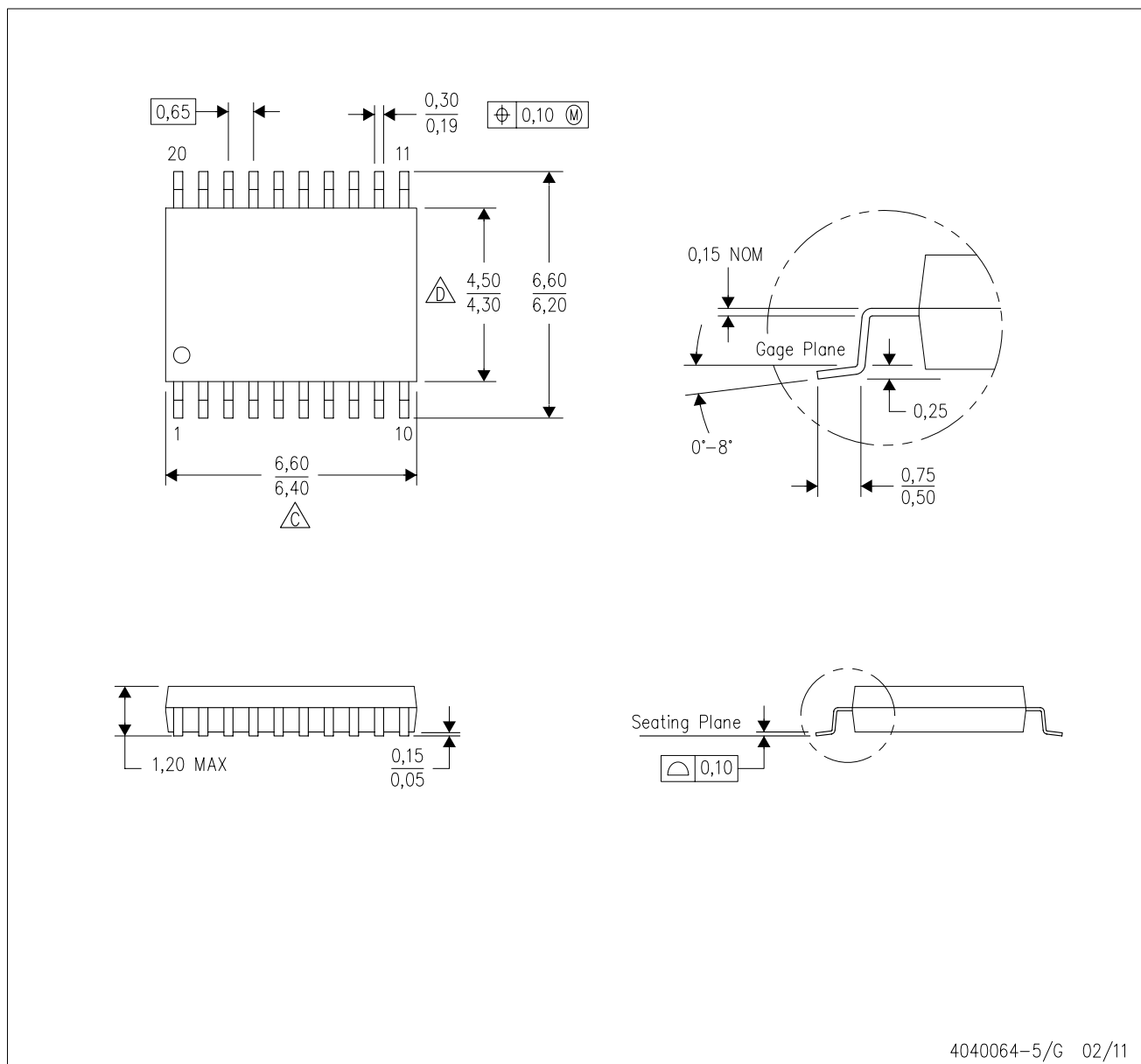


\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ABT541BIPWREP | TSSOP        | PW              | 20   | 2000 | 367.0       | 367.0      | 38.0        |

PW (R-PDSO-G20)

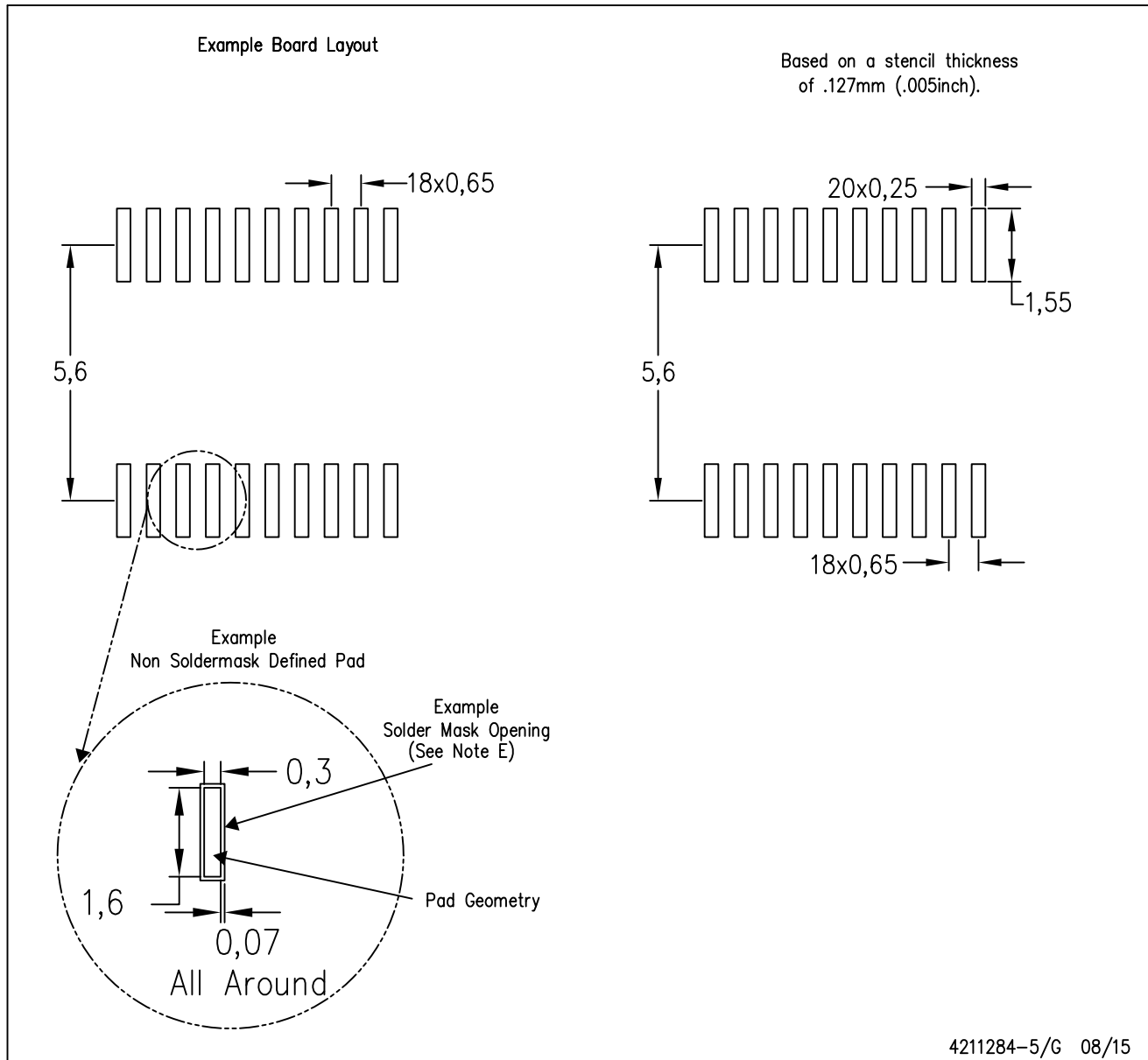
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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### Products

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### Applications

|                               |                                                                                          |
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