TEXAS INSTRUMENTS

SN74CBTLV3257

SCDS040L − DECEMBER 1997 − REVISED OCTOBER 2016

SN74CBTLV3257 Low-Voltage 4-Bit 1-of-2 FET Multiplexer/Demultiplexer

1 Features

- 5-Ω Switch Connection Between Two Ports
- Rail-to-Rail Switching on Data I/O Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

2 Applications

- Internet of Things
- Wireless Headphones
- Television Set
- 4-Bit Bus Multiplexing and Demultiplexing

3 Description

The SN74CBTLV3257 device is a 4-bit 1-of-2 high-speed FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The select (S) input controls the data flow. The FET multiplexers/demultiplexers are disabled when the output-enable ($\overline{OE}$) input is high.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.
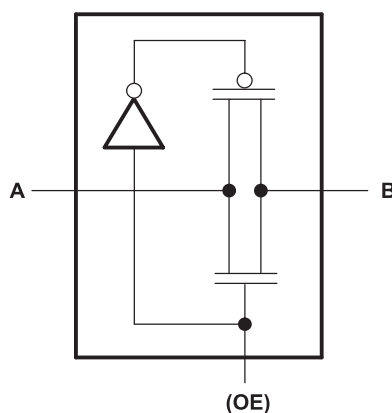
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74CBTLV3257DBQ	SSOP (16)	4.90 mm × 3.90 mm
SN74CBTLV3257PW	TSSOP (16)	5.00 mm × 4.40 mm
SN74CBTLV3257DGV	TVSOP (16)	3.60 mm × 4.40 mm
SN74CBTLV3257D	SOIC (16)	9.90 mm × 3.91 mm
SN74CBTLV3257RGY	VQFN (16)	4.00 mm × 3.50 mm
SN74CBTLV3257RSV	UQFN (16)	2.60 mm × 1.80 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic (Each FET Switch)

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision K (April 2015) to Revision L	**Page**
• Added TSSOP (16) to *Device Information* table	1
• Added Junction temperature, T_J in *Absolute Maximum Ratings*	4
• Changed wording in *Detailed Design Procedure* to clarify device operation	9
• Added *Receiving Notification of Documentation Updates* section and *Community Resources* section	11

Changes from Revision J (December 2012) to Revision K	**Page**
• Removed *Ordering Information* table, see *Mechanical, Packaging, and Orderable Information*	1
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Added *Applications*.	1
• Added *Device Information* table.	1

Changes from Revision I (October 2003) to Revision J	**Page**
• Added QFN ordering info and package pinout	1

Product Folder Links: *SN74CBTLV3257*

5 Pin Configuration and Functions

D, DBQ, DGV, and PW Package
16-Pin SOIC, SSOP, TVSOP, and TSSOP
(Top View)

```
         S  [ 1      16 ] V_CC
        1B1 [ 2      15 ] OE
        1B2 [ 3      14 ] 4B1
        1A  [ 4      13 ] 4B2
        2B1 [ 5      12 ] 4A
        2B2 [ 6      11 ] 3B1
        2A  [ 7      10 ] 3B2
        GND [ 8       9 ] 3A
```
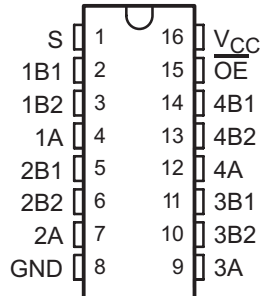
RGY Package
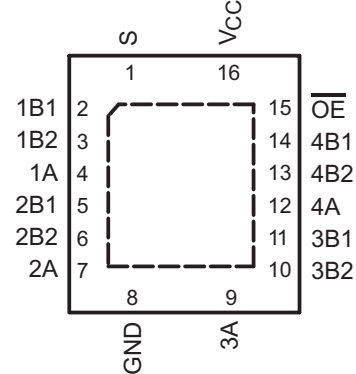**16-Pin VQFN**
(Top View)

```
              S       V_CC
              1        16
        1B1 [ 2      15 ] OE
        1B2 [ 3      14 ] 4B1
        1A  [ 4      13 ] 4B2
        2B1 [ 5      12 ] 4A
        2B2 [ 6      11 ] 3B1
        2A  [ 7      10 ] 3B2
              8        9
             GND      3A
```

RSV Package
16-Pin UQFN
(Top View)

```
        1B1   S    V_CC   OE
         16   15    14    13
    1B2 [ 1                12 ] 4B1
    1A  [ 2                11 ] 4B2
    2B1 [ 3                10 ] 4A
    2B2 [ 4                 9 ] 3B1
          5    6     7      8
         2A   GND   3A    3B2
```

Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOIC, SSOP, TVSOP, TSSOP, VQFN	UQFN		
1A	4	2	I/O	Channel 1 out/in common
1B1	2	16	I/O	Channel 1 in/out 1
1B2	3	1	I/O	Channel 1 in/out 2
2A	7	5	I/O	Channel 2 out/in common
2B1	5	3	I/O	Channel 2 in/out 1
2B2	6	4	I/O	Channel 2 in/out 2
3A	9	7	I/O	Channel 3 out/in common
3B1	11	9	I/O	Channel 3 in/out 1
3B2	10	8	I/O	Channel 3 in/out 2
4A	12	10	I/O	Channel 4 out/in common
4B1	14	12	I/O	Channel 4 in/out 1
4B2	13	11	I/O	Channel 4 in/out 2
GND	8	6	—	Ground
OE	15	13	I	Output Enable, active low
S	1	15	I	Select
V_CC	16	14	—	Power

Product Folder Links: *SN74CBTLV3257*

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		−0.5	4.6	V
V_I	Input voltage [2]		−0.5	4.6	V
	Continuous channel current			128	mA
I_{IK}	Input clamp current	$V_{I/O} < 0$		−50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
T_A	Operating free-air temperature		−40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC[1]	SN74CBTLV3257					UNIT
	D	DBQ	DGV	PW	RGY	
	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	73	90	120	108	39	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[1]	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 3.6 V,	$V_I = V_{CC}$ or GND				±1	µA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 3.6 V				15	µA
I_{CC}		V_{CC} = 3.6 V,	I_O = 0,	$V_I = V_{CC}$ or GND			10	µA
ΔI_{CC}[2]	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	µA
C_i		V_I = 3 V or 0					3	pF
$C_{io(OFF)}$	A port	V_O = 3 V or 0,	$\overline{OE} = V_{CC}$			10.5		pF
	B port					5.5		
r_{on}[3]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0	I_I = 64 mA		5	8	Ω
				I_I = 24 mA		5	8	
			V_I = 1.7 V	I_I = 15 mA		27	40	
		V_{CC} = 3 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 24 mA		5	7	
			V_I = 2.4 V	I_I = 15 mA		10	15	

(1) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(2) This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.
(3) Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.
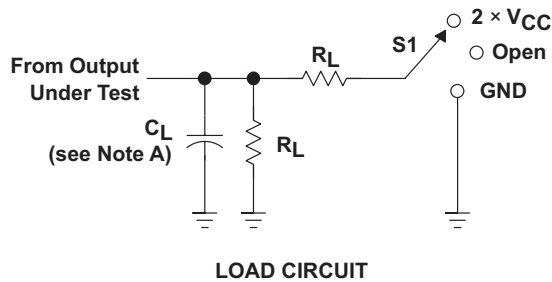
6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (See Figure 1)

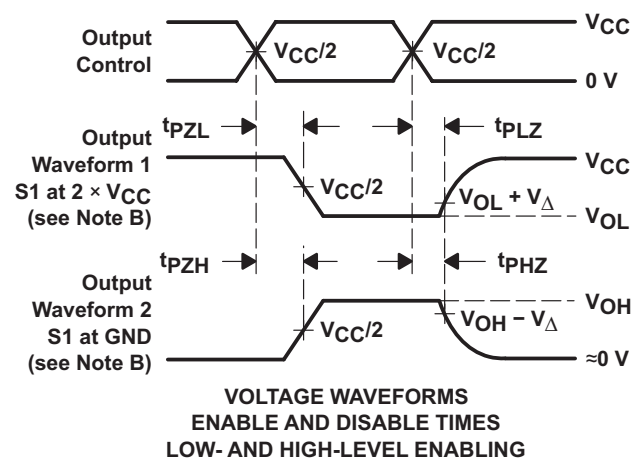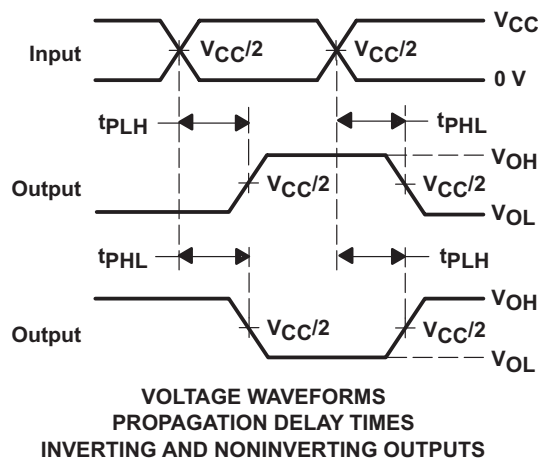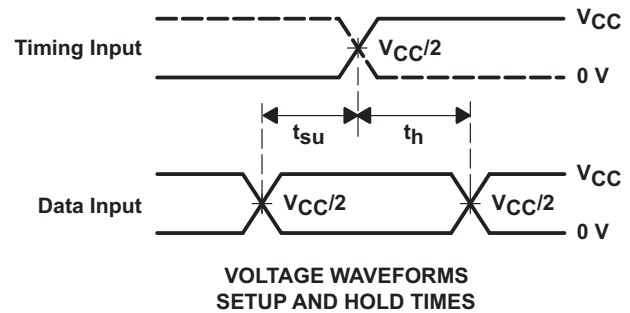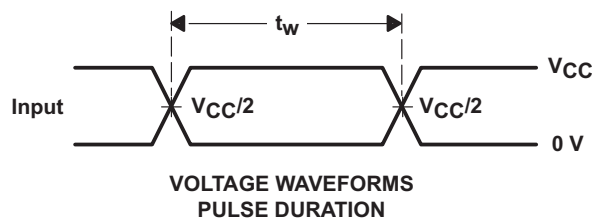| PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A or B[1]	B or A		0.15		0.25	ns
	S	A or B	1.8	6.1	1.8	5.3	
t_{en}	S	A or B	1.7	6.1	1.7	5.3	ns
t_{dis}	S	A or B	1	4.8	1	4.5	ns
t_{en}	$\overline{OE}$	A or B	1.9	5.6	2	5	ns
t_{dis}	$\overline{OE}$	A or B	1	5.5	1.6	5.5	ns

(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

7 Parameter Measurement Information

LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

V_{CC}	C_L	R_L	V_Δ
2.5 V ± 0.2 V	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	50 pF	500 Ω	0.3 V

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
     Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
   D. The outputs are measured one at a time with one transition per measurement.
   E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
   F. t_{PZL} and t_{PZH} are the same as t_{en}.
   G. t_{PLH} and t_{PHL} are the same as t_{pd}.
   H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

Product Folder Links: *SN74CBTLV3257*

8 Detailed Description

8.1 Overview

The SN74CBTLV3257 device is a 4-bit 1-of-2 high-speed FET multiplexer and demultiplexer. The low ON-state resistance of the switch allows connections to be made with minimal propagation delay.

The select (S) input controls the data flow. The FET multiplexers and demultiplexers are disabled when the output-enable ($\overline{OE}$) input is high.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

8.2 Functional Block Diagram
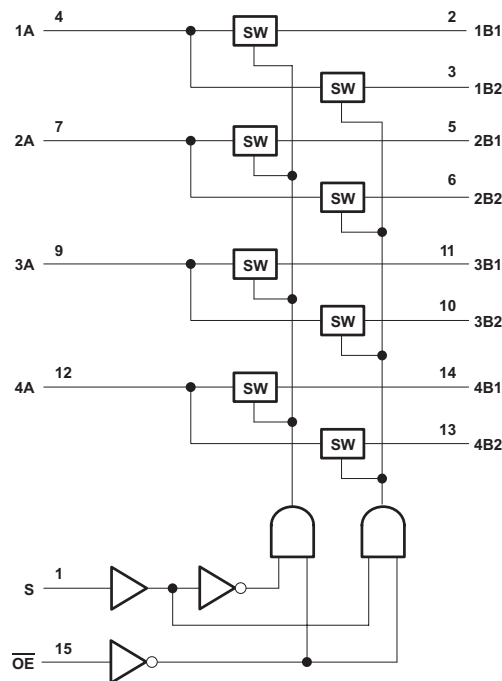
8.3 Feature Description

The SN74CBTLV3257 features 5-Ω switch connection between ports, allowing for low signal loss across the switch. Rail-to-rail switching on data I/O allows for full voltage swing outputs. I_{off} supports partial-power-down mode operation, protecting the chip from voltages at output ports when it is not powered on. Latch-up performance exceeds 100 mA per JESD 78, Class II.

8.4 Device Functional Modes

Table 1 shows the functional modes of SN74CBTLV3257.

Table 1. Function Table

INPUTS		FUNCTION
$\overline{OE}$	S	
L	L	A port = B1 port
L	H	A port = B2 port
H	X	Disconnect

Product Folder Links: *SN74CBTLV3257*

9 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74CBTLV3257 can be used to multiplex and demultiplex up to 4 channels simultaneously in a 2:1 configuration. The application shown here is a 4-bit bus being multiplexed between two devices. the $\overline{OE}$ and S pins are used to control the chip from the bus controller. This is a very generic example, and could apply to many situations. If an application requires less than 4 bits, be sure to tie the A side to either high or low on unused channels.

9.2 Typical Application
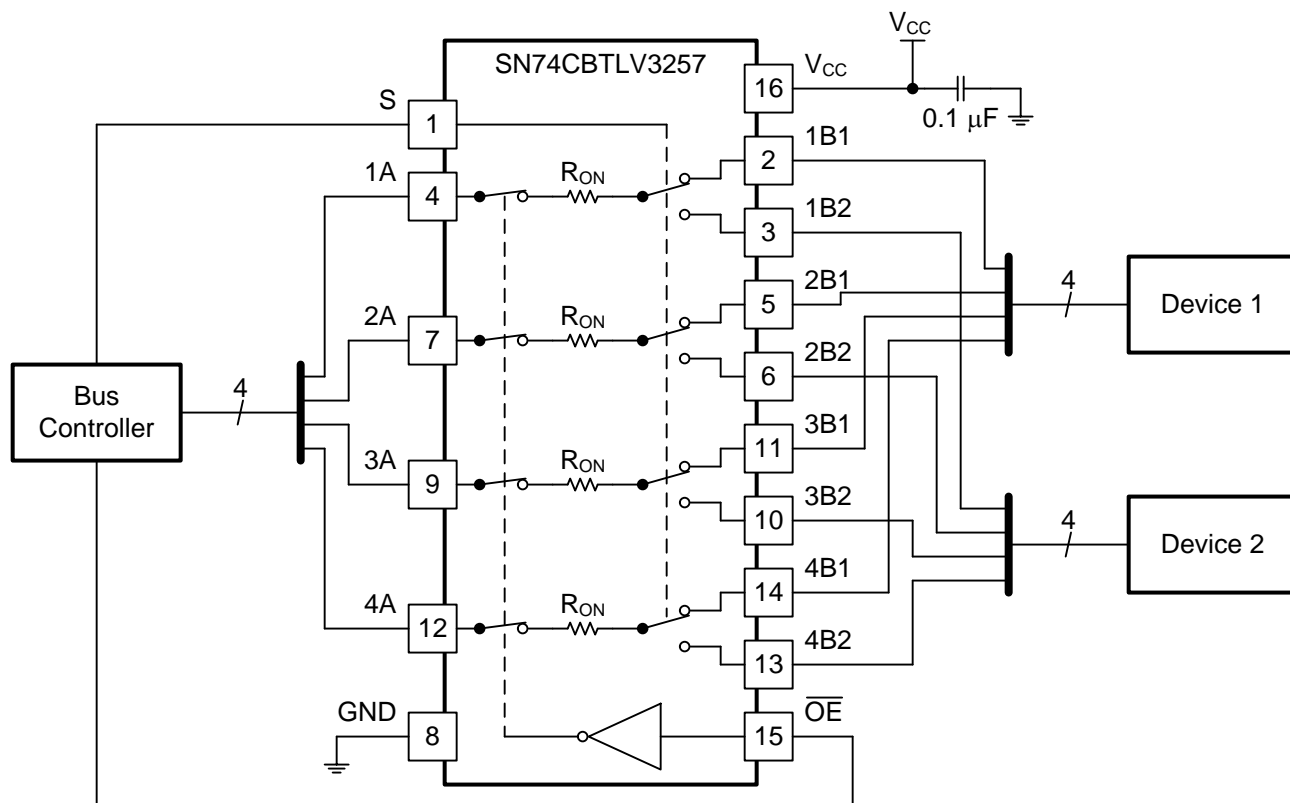
Figure 2. Typical Application of the SN74CBTLV3257

9.2.1 Design Requirements

1. Recommended Input Conditions:
   – For specified high and low levels, see V_{IH} and V_{IL} in *Recommended Operating Conditions*.
   – Inputs and outputs are overvoltage tolerant slowing them to go as high as 4.6 V at any valid V_{CC}.
2. Recommended Output Conditions:
   – Load currents should not exceed ±128 mA per channel.
3. Frequency Selection Criterion:
   – Maximum frequency tested is 200 MHz.

Typical Application (continued)

– Added trace resistance/capacitance can reduce maximum frequency capability; use layout practices as directed in *Layout*.

9.2.2 Detailed Design Procedure

The 4-bit bus is connected directly to the 1A, 2A, 3A, and 4A ports (known as the xA port) on the SN74CBTLV3257, which essentially splits it into two busses, coming out of the xB1 and xB2 ports. When S is high, xB2 is the active bus, and when S is low, xB1 is the active bus. This means that Device 2 is connected to the bus controller when S is high, and Device 1 is connected to the bus controller when S is low. This setup is especially useful when two devices are hard coded with the same address and only one bus is available. The $\overline{OE}$ connection can be used to disconnect all devices from the bus controller if necessary.

The 0.1-µF capacitor on V_{CC} is a decoupling capacitor and should be placed as close as possible to the device.

9.2.3 Application Curve
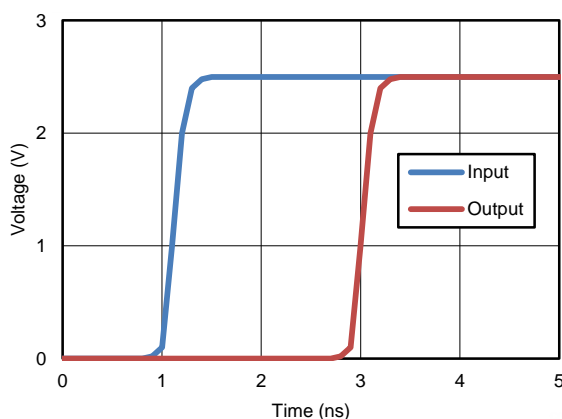
Figure 3. Propagation Delay (t_{pd}) Simulation Result at V_{CC} = 2.5 V

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions* table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF bypass capacitor is recommended. If multiple pins are labeled V_{CC}, then a 0.01-µF or 0.022-µF capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-µF bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

Submit Documentation Feedback   9

Product Folder Links: *SN74CBTLV3257*

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 4 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

11.2 Layout Example

WORST   BETTER   BEST

2W

1W min.

W
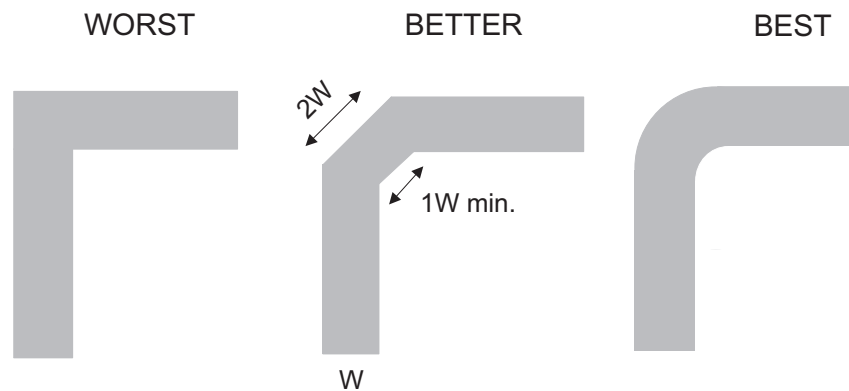
Figure 4. Trace Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:
- *Implications of Slow or Floating CMOS Inputs*, SCBA004
- *Selecting the Right Texas Instruments Signal Switch*, SZZA030

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74CBTLV3257DBQRE4	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL257	Samples
74CBTLV3257DBQRG4	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL257	Samples
74CBTLV3257PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL257	Samples
74CBTLV3257PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL257	Samples
74CBTLV3257RGYRG4	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL257	Samples
SN74CBTLV3257D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3257	Samples
SN74CBTLV3257DBQR	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL257	Samples
SN74CBTLV3257DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3257	Samples
SN74CBTLV3257DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3257	Samples
SN74CBTLV3257DGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL257	Samples
SN74CBTLV3257DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3257	Samples
SN74CBTLV3257DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3257	Samples
SN74CBTLV3257DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3257	Samples
SN74CBTLV3257PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL257	Samples
SN74CBTLV3257PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL257	Samples
SN74CBTLV3257PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL257	Samples
SN74CBTLV3257PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	CL257	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CBTLV3257RGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL257	Samples
SN74CBTLV3257RSVR	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZTR	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM

OTHER QUALIFIED VERSIONS OF SN74CBTLV3257 :

● Enhanced Product: SN74CBTLV3257-EP

NOTE: Qualified Version Definitions:

● Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74CBTLV3257PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBTLV3257DBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
SN74CBTLV3257DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74CBTLV3257DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74CBTLV3257PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBTLV3257PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBTLV3257RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74CBTLV3257PWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74CBTLV3257DBQR	SSOP	DBQ	16	2500	340.5	338.1	20.6
SN74CBTLV3257DGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
SN74CBTLV3257DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74CBTLV3257PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74CBTLV3257PWR	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74CBTLV3257RGYR	VQFN	RGY	16	3000	367.0	367.0	35.0

DGV (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

PINS ** DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0.394 (10,00)
0.386 (9,80)
△C

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) △D

1   8

Pin 1
Index Area

0.050 (1,27)   0.020 (0,51)
                            0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.069 (1,75) Max   0.010 (0,25)
                                    0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

△ | 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−6/M   06/11

NOTES: A. All linear dimensions are in inches (millimeters).
          B. This drawing is subject to change without notice.
        △C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0.006 (0,15) each side.
        △D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
          E. Reference JEDEC MS−012 variation AC.

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INSTRUMENTS
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D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

←14x1,27

←16x0,55

←14x1,27

16x1,50

5,40

5.40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

─0,60

1,55

Example
Solder Mask Opening
(See Note E)

─0,07

All Around

4211283−4/E 08/12

NOTES: A. All linear dimensions are in millimeters.
           B. This drawing is subject to change without notice.
           C. Publication IPC−7351 is recommended for alternate designs.
           D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
               contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
           E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
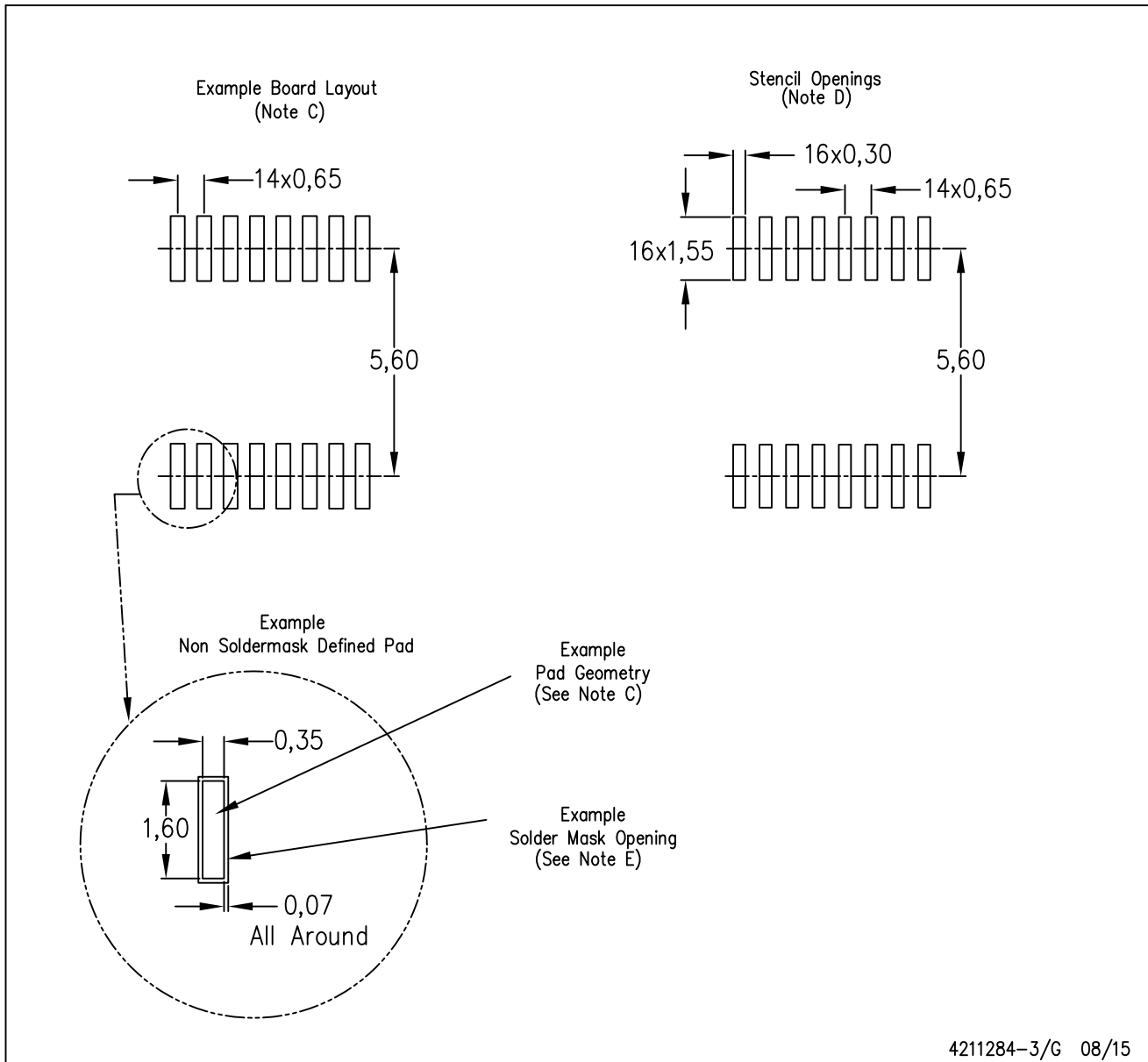
PW (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0,65   0,30/0,19   ⊕ 0,10 Ⓜ

16   9

⟨D⟩ 4,50/4,30   6,60/6,20

1   8

5,10/4,90
⟨C⟩

0,15 NOM

Gage Plane

0°−8°   0,75/0,50   0,25

1,20 MAX   0,15/0,05

Seating Plane   ⌓ 0,10

4040064−4/G 02/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
          B.   This drawing is subject to change without notice.
        ⟨C⟩   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
               not exceed 0,15 each side.
        ⟨D⟩   Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
          E.   Falls within JEDEC MO−153

PW (R-PDSO-G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

├─14x0,65

5,60

Stencil Openings
(Note D)

├─ 16x0,30

├─14x0,65

16x1,55

5,60

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

├─0,35

1,60

Example
Solder Mask Opening
(See Note E)

├─0,07
All Around

4211284-3/G 08/15

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC-7351 is recommended for alternate designs.
         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
         E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (R−PVQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD

4203539−3/I 06/2011

Bottom View

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        C. QFN (Quad Flatpack No−Lead) package configuration.
        D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
        E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
        F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
            The Pin 1 identifiers are either a molded, marked, or metal feature.
        G. Package complies to JEDEC MO−241 variation BA.

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RGY (R−PVQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.
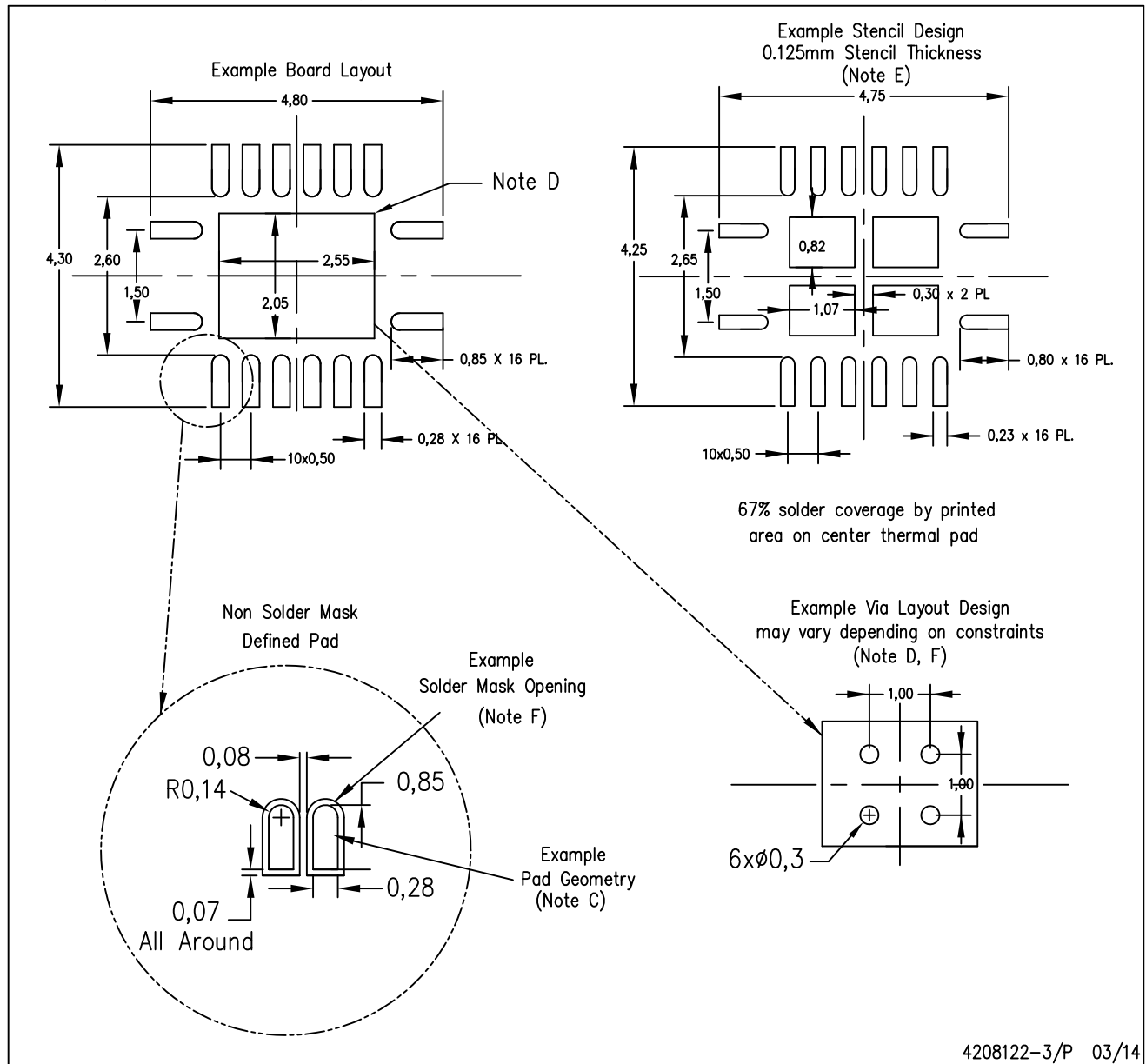

Bottom View

Exposed Thermal Pad Dimensions

4206353−3/P   03/14

NOTE: All linear dimensions are in millimeters

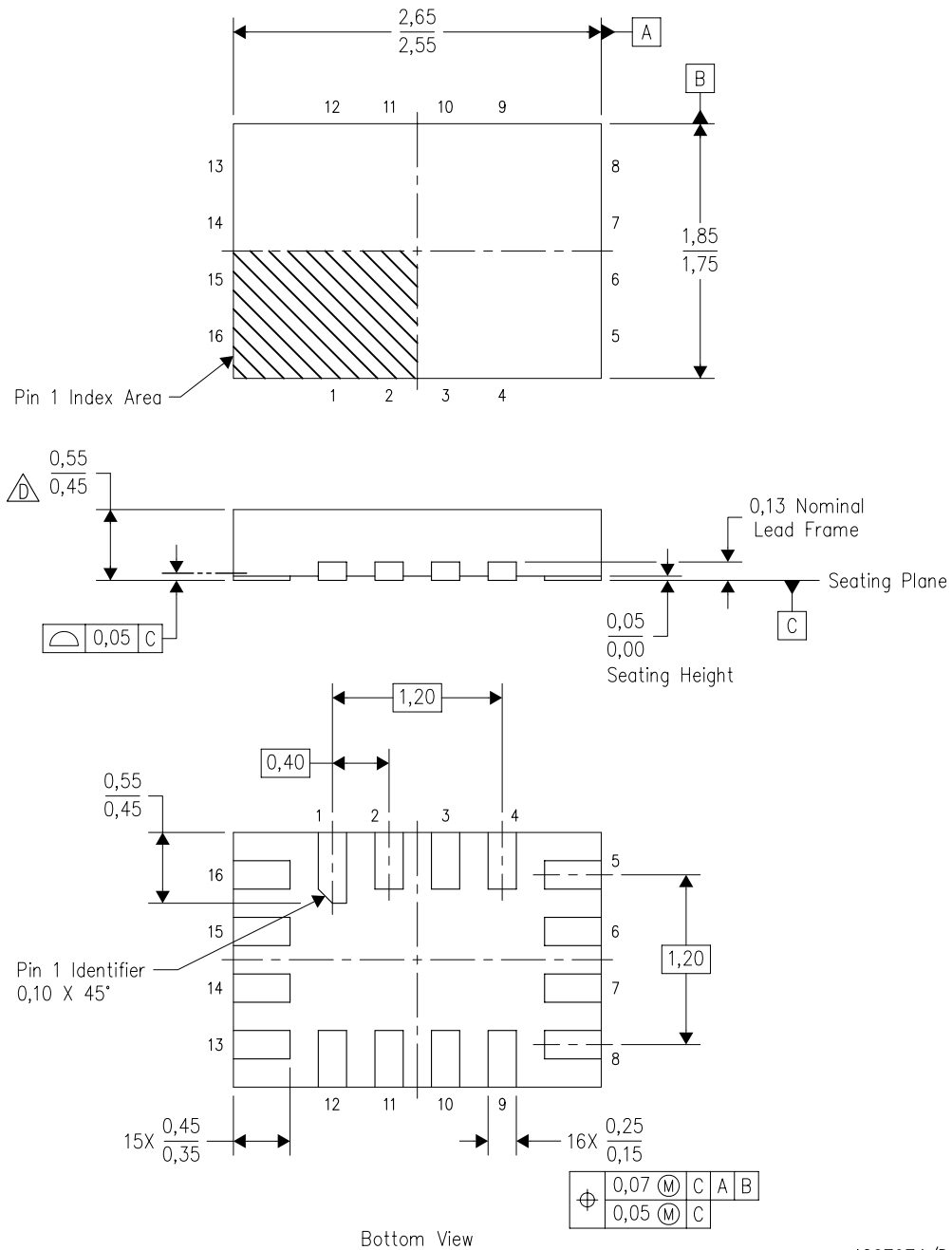RGY (R−PVQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD

Example Board Layout

Note D

4,80
4,30   2,60
1,50
2,55
2,05
0,85 X 16 PL.
0,28 X 16 PL.
10x0,50

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

4,75
4,25   2,65
1,50
0,82
0,30 x 2 PL
1,07
0,80 x 16 PL.
0,23 x 16 PL.
10x0,50

67% solder coverage by printed
area on center thermal pad

Non Solder Mask
Defined Pad

Example
Solder Mask Opening
(Note F)

0,08
R0,14
0,85
0,07
0,28
All Around

Example
Pad Geometry
(Note C)

Example Via Layout Design
may vary depending on constraints
(Note D, F)

1,00
1,00
6x∅0,3

4208122−3/P 03/14

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate designs.
        D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat−Pack
            QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
            for specific thermal information, via requirements, and recommended board layout.
            These documents are available at www.ti.com <http://www.ti.com>.
        E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
        F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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RSV (R−PUQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD

2,65 / 2,55

1,85 / 1,75

Pin 1 Index Area

0,55 / 0,45

0,13 Nominal Lead Frame

Seating Plane

0,05 C

0,05 / 0,00
Seating Height

1,20

0,40

0,55 / 0,45

Pin 1 Identifier
0,10 X 45°

1,20

15X 0,45 / 0,35

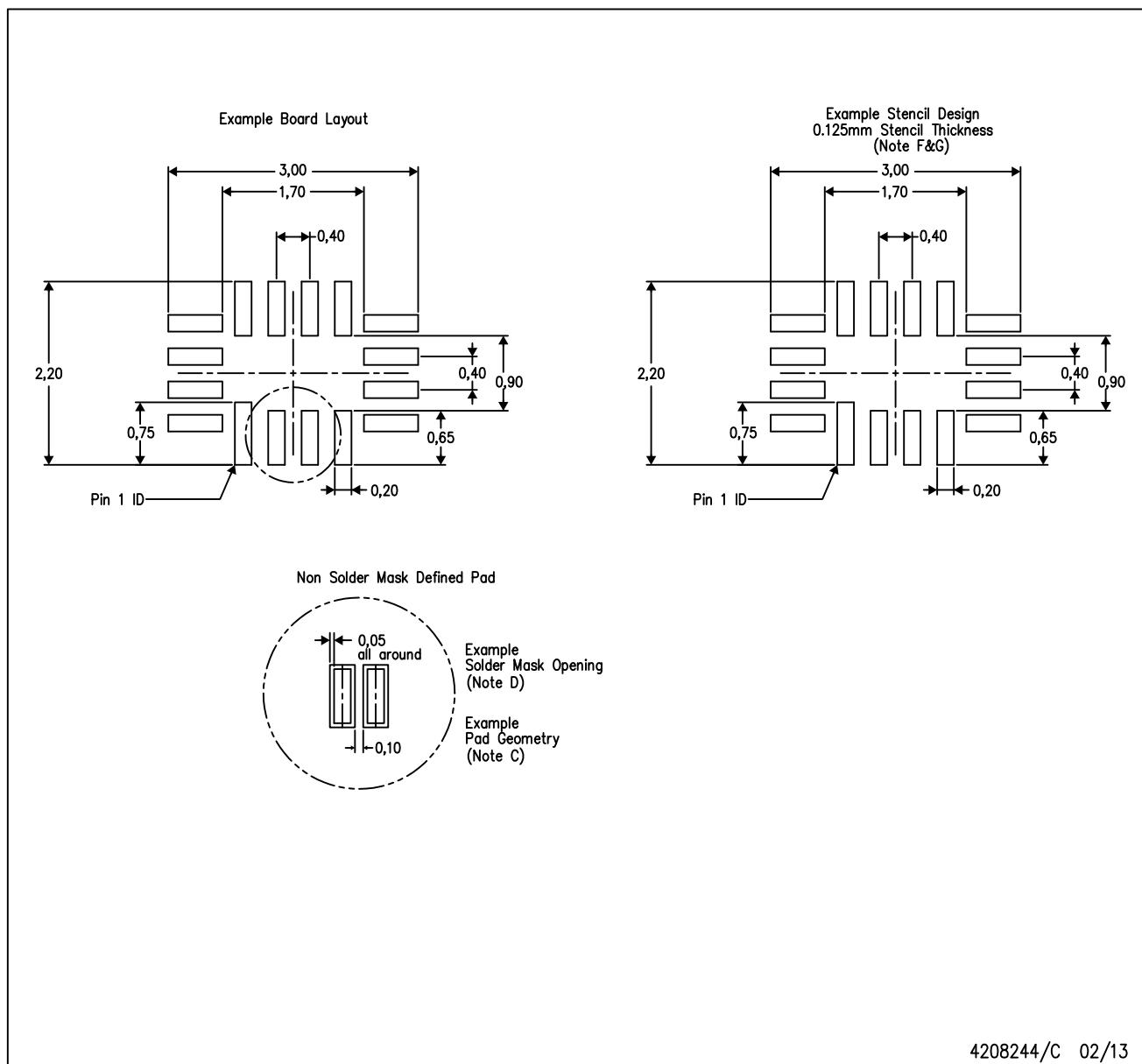16X 0,25 / 0,15

⊕ 0,07 Ⓜ C A B
0,05 Ⓜ C

Bottom View

4207974/D 12/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   QFN (Quad Flatpack No−Lead) package configuration.
         D.   This package complies to JEDEC MO−288 variation UFHE, except minimum package thickness.
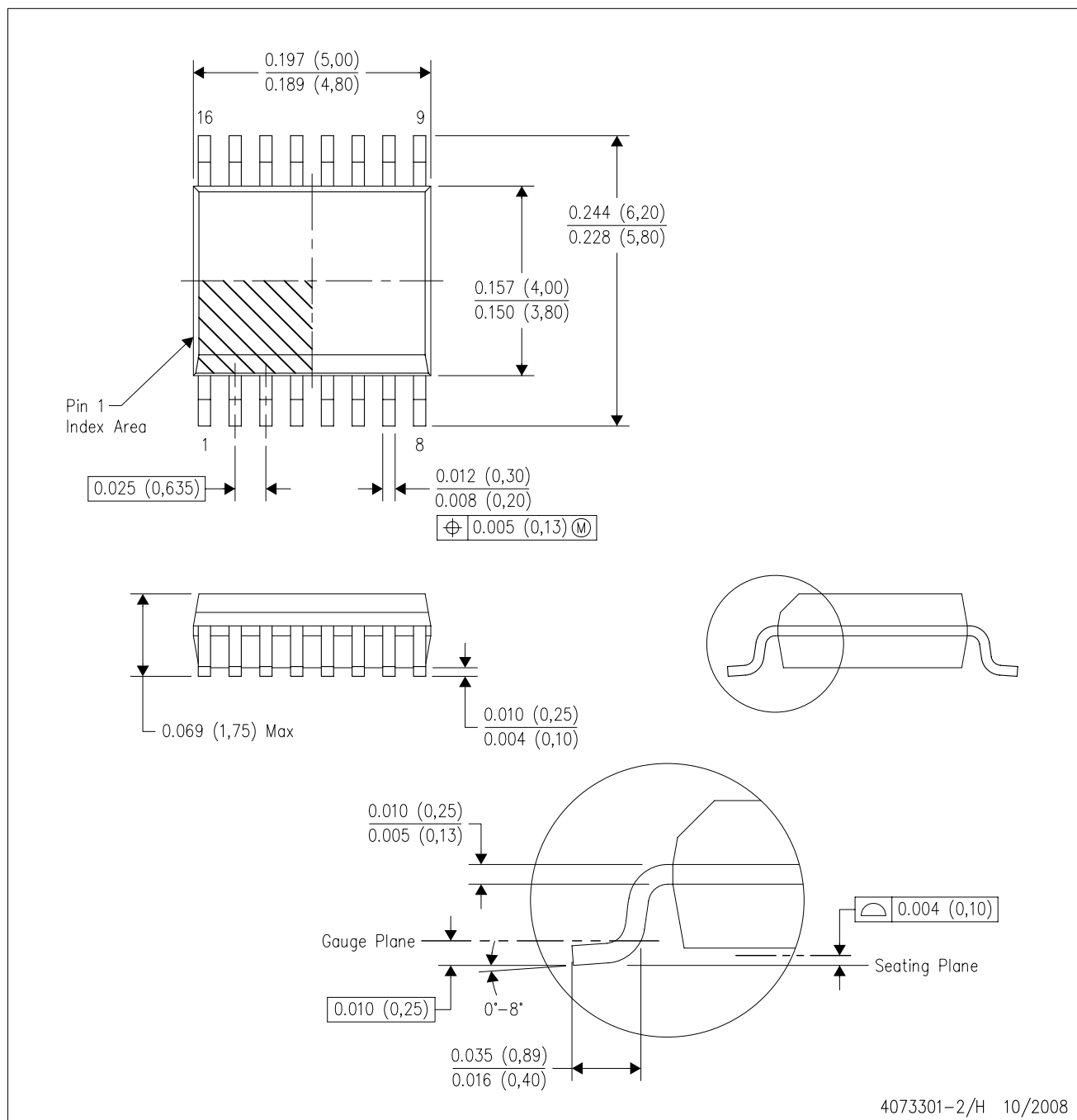
RSV (R−PUQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD

Example Board Layout

Example Stencil Design
0.125mm Stencil Thickness
(Note F&G)

Non Solder Mask Defined Pad

0,05
all around

Example
Solder Mask Opening
(Note D)

Example
Pad Geometry
(Note C)

0,10

4208244/C 02/13

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate designs.
        D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
        E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
        F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
        G. Side aperture dimensions over−print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions
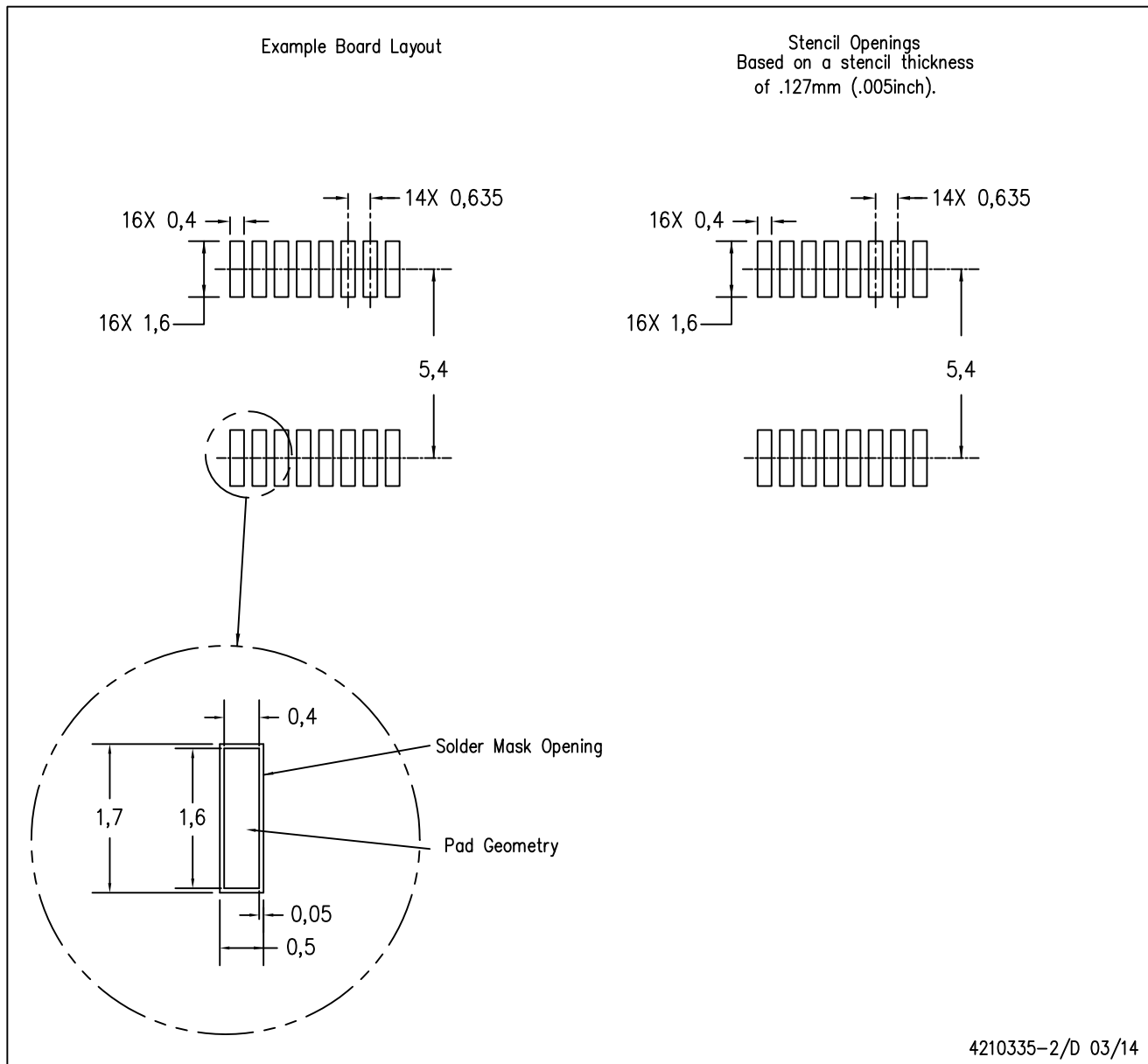   if stencil manufacturing process allows for sufficient release at smaller opening.

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DBQ (R−PDSO−G16)   PLASTIC SMALL−OUTLINE PACKAGE

0.197 (5,00)
0.189 (4,80)

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

Pin 1
Index Area

1   8

0.025 (0,635)

0.012 (0,30)
0.008 (0,20)

⌖ | 0.005 (0,13) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.035 (0,89)
0.016 (0,40)

4073301−2/H   10/2008

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
        D. Falls within JEDEC MO−137 variation AB.

DBQ (R–PDSO–G16)   PLASTIC SMALL OUTLINE PACKAGE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

14X 0,635

16X 0,4

16X 1,6

5,4

16X 0,4

16X 1,6

14X 0,635

5,4

0,4

Solder Mask Opening

1,7   1,6

Pad Geometry

0,05

0,5

4210335–2/D 03/14

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC–7351 is recommended for alternate designs.
         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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