TEXAS INSTRUMENTS

SN54HC125
SN74HC125

SCLS104E – AUGUST 1984 – REVISED DECEMBER 2015

SNx4HC125 Quadruple Bus Buffer Gates With 3-State Outputs

1 Features

- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State Outputs Interface Directly With System Bus or Can Drive Up to 15 LSTTL Loads
- Low Power Consumption, 80-µA Maximum I_{CC}
- Typical t_{pd} = 11 ns
- ±6-mA Output Drive at 5 V
- Low Input Current of 1 µA Maximum

2 Applications

- TV Set-Top Boxes and DVRs
- E-meters
- Smart Grids: Transmission Line Monitoring
- Printers and Computer Peripherals
- Building Security: Control Panels
- IP Phones
- Test and Measurement: Range Readers
- Smart Grids: Distribution Feeder Protection Relay

3 Description

The SNx4HC125 device is a quadruple set of bus buffer gates and features independent line drivers with 3-state outputs. The SNx4HC125 is designed for 2-V to 6-V V_{CC} operation. Each output is disabled when the associated output-enable ($\overline{OE}$) input is high.

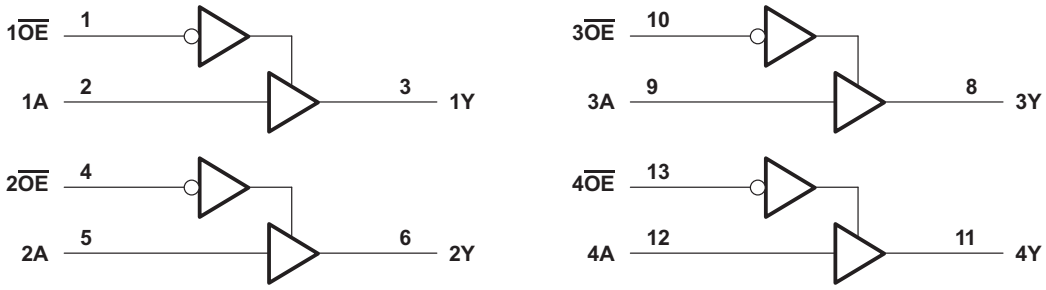
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74HC125N	PDIP (14)	18.30 mm × 6.35 mm
SN74HC125D	SOIC (14)	8.65 mm × 6.00 mm
SN74HC125W	SO (14)	10.20 mm × 5.30 mm
SN74HC125DB	SSOP (14)	6.20 mm × 5.30 mm
SN74HC125PW	TSSOP (14)	5.00 mm × 4.40 mm
SN54HC125J	CDIP (14)	19.90 mm × 6.90 mm
SN54HC125FK	LCCC (20)	8.90 mm × 8.44 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (August 2003) to Revision E	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1
• Removed *Ordering Information* table.	1

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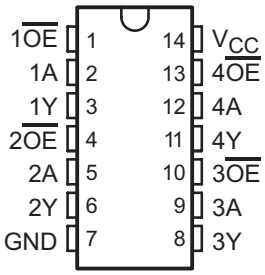
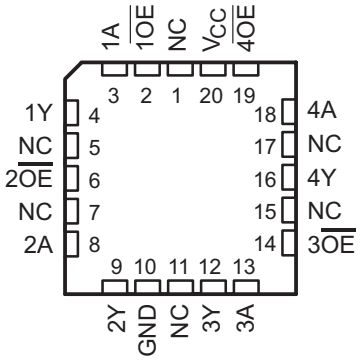
5 Pin Configuration and Functions

D, DB, N, NS, J, or PW Package
14-Pin SOIC, SSOP, PDIP, SO, CDIP, or TSSOP
Top View



FK Package
20-Pin LCCC
Top View



Pin Functions[1]

PIN			I/O	DESCRIPTION
NAME	SOIC, SSOP, PDIP, SO, CDIP, or TSSOP	LCCC		
1A	2	3	I	Input
$1\overline{OE}$	1	2	I	Output Enable (Active Low)
1Y	3	4	O	Output
2A	5	8	I	Input
$2\overline{OE}$	4	6	I	Output Enable (Active Low)
2Y	6	9	O	Output
3A	9	13	I	Input
$3\overline{OE}$	10	14	I	Output Enable (Active Low)
3Y	8	12	O	Output
4A	12	18	I	Input
$4\overline{OE}$	13	19	I	Output Enable (Active Low)
4Y	11	16	O	Output
GND	7	10	—	Ground
NC[2]	—	1, 5, 7, 11, 15, 17	—	Not connected
V_{CC}	14	20	—	Power

(1) See *Mechanical, Packaging, and Orderable Information* for dimensions
(2) NC – No internal connection

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current(2)	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
T_j	Junction temperature		–65	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See (1).

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 6 V	4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 6 V			1.8	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise and fall time	V_{CC} = 2 V			1000	ns
		V_{CC} = 4.5 V			500	
		V_{CC} = 6 V			400	
T_A	Operating free-air temperature	SN54HC125	–55		125	°C
		SN74HC125	–40		85	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC(1)		SN74LVC1G06					UNIT
		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SOP)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86	96	80	76	113	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics, T_A = 25°C

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 µA	2 V	1.9	1.998		V
			4.5 V	4.4	4.499		
			6 V	5.9	5.999		
		I_{OH} = –6 mA	4.5 V	3.98	4.3		
		I_{OH} = –7.8 mA	6 V	5.48	5.8		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	2 V		0.002	0.1	V
			4.5 V		0.001	0.1	
			6 V		0.001	0.1	
		I_{OL} = 6 mA	4.5 V		0.17	0.26	
		I_{OL} = 7.8 mA	6 V		0.15	0.26	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100	nA
I_{OZ}	V_O = V_{CC} or 0		6 V		±0.01	±0.5	µA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8	µA
C_i			2 V to 6 V		3	10	pF

6.6 Electrical Characteristics, SN54HC125

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	MAX	UNIT
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 µA	2 V	1.9		V
			4.5 V	4.4		
			6 V	5.9		
		I_{OH} = –6 mA	4.5 V	3.7		
		I_{OH} = –7.8 mA	6 V	5.2		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	2 V		0.1	V
			4.5 V		0.1	
			6 V		0.1	
		I_{OL} = 6 mA	4.5 V		0.4	
		I_{OL} = 7.8 mA	6 V		0.4	
I_I	V_I = V_{CC} or 0		6 V		±1000	nA
I_{OZ}	V_O = V_{CC} or 0		6 V		±10	µA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V		160	µA
C_i			2 V to 6 V		10	pF

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6.7 Electrical Characteristics, SN74HC125

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	MAX	UNIT
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 µA	2 V	1.9		V
			4.5 V	4.4		
			6 V	5.9		
		I_{OH} = –6 mA	4.5 V	3.84		
		I_{OH} = –7.8 mA	6 V	5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	2 V		0.1	V
			4.5 V		0.1	
			6 V		0.1	
		I_{OL} = 6 mA	4.5 V		0.33	
		I_{OL} = 7.8 mA	6 V		0.33	
I_I	$V_I = V_{CC}$ or 0		6 V		±1000	nA
I_{OZ}	$V_O = V_{CC}$ or 0		6 V		±5	µA
I_{CC}	$V_I = V_{CC}$ or 0,	I_O = 0	6 V		80	µA
C_i			2 V to 6 V		10	pF

6.8 Switching Characteristics, T_A = 25°C, C_L = 50 pF

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	A	Y	2 V		48	150	ns
			4.5 V		14	30	
			6 V		11	26	
t_{en}	$\overline{OE}$	Y	2 V		53	150	ns
			4.5 V		14	30	
			6 V		11	26	
t_{dis}	$\overline{OE}$	Y	2 V		30	150	ns
			4.5 V		15	30	
			6 V		14	26	
t_t		Any	2 V		28	75	ns
			4.5 V		8	15	
			6 V		6	13	

6.9 Switching Characteristics, SN54HC125, C_L = 50 pF

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
t_{pd}	A	Y	2 V		150	ns
			4.5 V		36	
			6 V		25	
t_{en}	$\overline{OE}$	Y	2 V		180	ns
			4.5 V		36	
			6 V		31	
t_{dis}	$\overline{OE}$	Y	2 V		180	ns
			4.5 V		36	
			6 V		31	

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Switching Characteristics, SN54HC125, C_L = 50 pF (continued)

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
t_t		Any	2 V		90	ns
			4.5 V		18	
			6 V		15	

6.10 Switching Characteristics, SN74HC125, C_L = 50 pF

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
t_{pd}	A	Y	2 V		150	ns
			4.5 V		30	
			6 V		26	
t_{en}	$\overline{OE}$	Y	2 V		150	ns
			4.5 V		30	
			6 V		26	
t_{dis}	$\overline{OE}$	Y	2 V		150	ns
			4.5 V		30	
			6 V		26	
t_t		Any	2 V		75	ns
			4.5 V		15	
			6 V		13	

6.11 Switching Characteristics, T_A = 25°C , C_L = 150 pF

over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	A	Y	2 V		67	150	ns
			4.5 V		19	30	
			6 V		15	25	
t_{en}	$\overline{OE}$	Y	2 V		100	135	ns
			4.5 V		20	27	
			6 V		17	23	
t_t		Any	2 V		45	210	ns
			4.5 V		17	42	
			6 V		13	36	

6.12 Switching Characteristics, SN54HC125, C_L = 150 pF

over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
t_{pd}	A	Y	2 V		225	ns
			4.5 V		45	
			6 V		39	
t_{en}	$\overline{OE}$	Y	2 V		200	ns
			4.5 V		40	
			6 V		34	

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Switching Characteristics, SN54HC125, C_L = 150 pF (continued)

over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
t_t		Any	2 V		315	ns
			4.5 V		63	
			6 V		53	

6.13 Switching Characteristics, SN74HC125, C_L = 150 pF

over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
t_{pd}	A	Y	2 V		190	ns
			4.5 V		38	
			6 V		32	
t_{en}	$\overline{OE}$	Y	2 V		170	ns
			4.5 V		34	
			6 V		29	
t_t		Any	2 V		265	ns
			4.5 V		53	
			6 V		45	

6.14 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	45	pF

6.15 Typical Characteristics

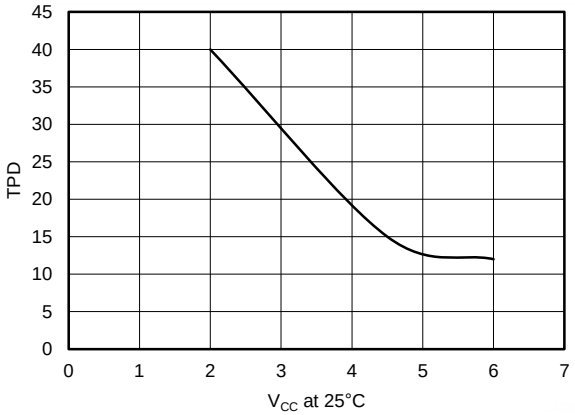

Figure 1. TPD vs V_{CC} at 25°C

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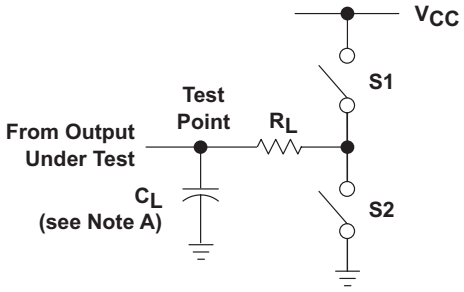
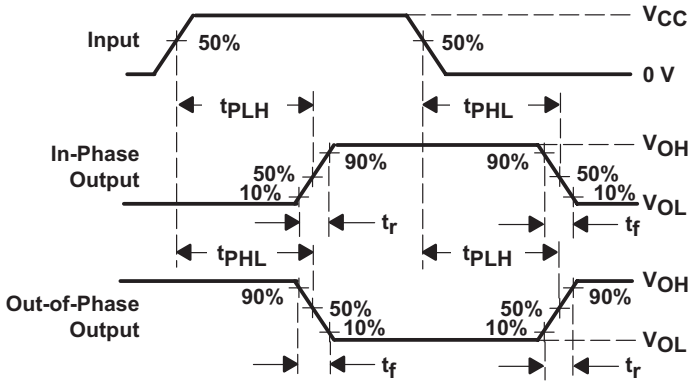
7 Parameter Measurement Information

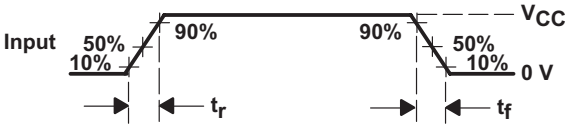


LOAD CIRCUIT

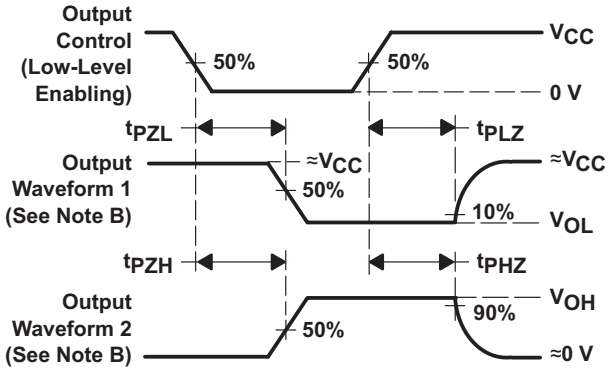
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		--	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

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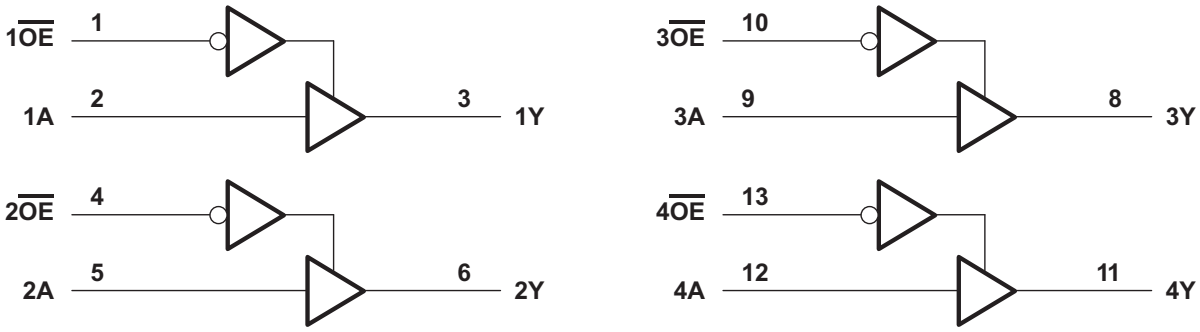
8 Detailed Description

8.1 Overview

The SNx4HC125 offers 4 independent gate buffers capable of sinking or sourcing 6 mA at 5-V V_{CC}. Each buffer also integrates a 3-state output, or high impedance output. To enable the device's 3-state output, set the corresponding $\overline{OE}$ input to a HIGH logic level.

Major benefits of using HC logic include both the technology's flexibility of input V_{CC} (2 V to 6 V) and high-speed capability (11 ns typical t_{pd}).

8.2 Functional Block Diagram



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

8.3 Feature Description

The 3-state outputs enable design choices such as connecting multiple outputs together, as long as the 3-state controls are used correctly. In a typical example, without 3-state outputs, if two outputs were connected to the same input on an adjacent system, and each output was trying to drive a different logic level (one HIGH, one LOW), the device could short-circuit and become damaged. With 3-state output functionality, the outputs can be configured so that when one output is driving an output signal, the others are set to high impedance and prevent any damage to the device.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SNx4HC125.

Table 1. Function Table

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SNx4HC125 can be used to buffer noisy or weak input signals in order to clean up these signals and drive a strong logic level to a processor or other sampling system.

9.2 Typical Application

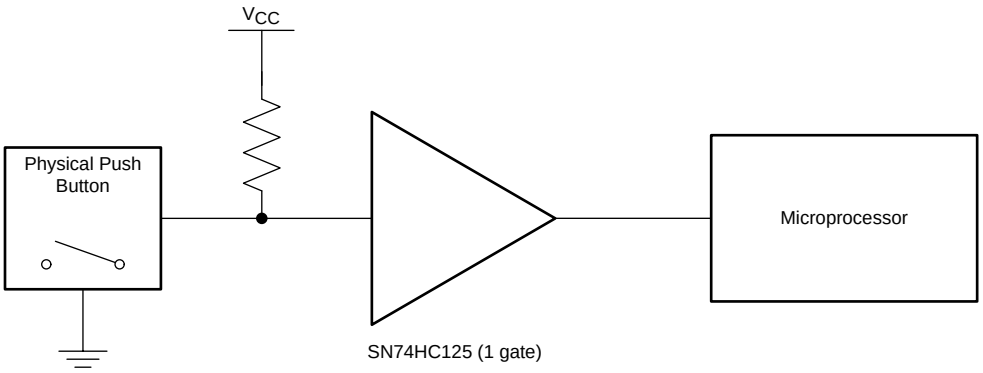

Figure 3. Typical Application Diagram

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - Rise time and fall time specs. See (Δt/ΔV) in the *Recommended Operating Conditions* table.
   - Specified high and low levels. See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as (V_I maximum) in the *Recommended Operating Conditions* table at any valid V_{CC}.
2. Recommend Output Conditions
   - Load currents should not exceed (I_O maximum) per output and should not exceed (continuous current through V_{CC} or GND) total current for the part. These limits are located in the *Absolute Maximum Ratings* table.
   - Outputs should not be pulled above V_{CC}.

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Typical Application (continued)

9.2.3 Application Curve

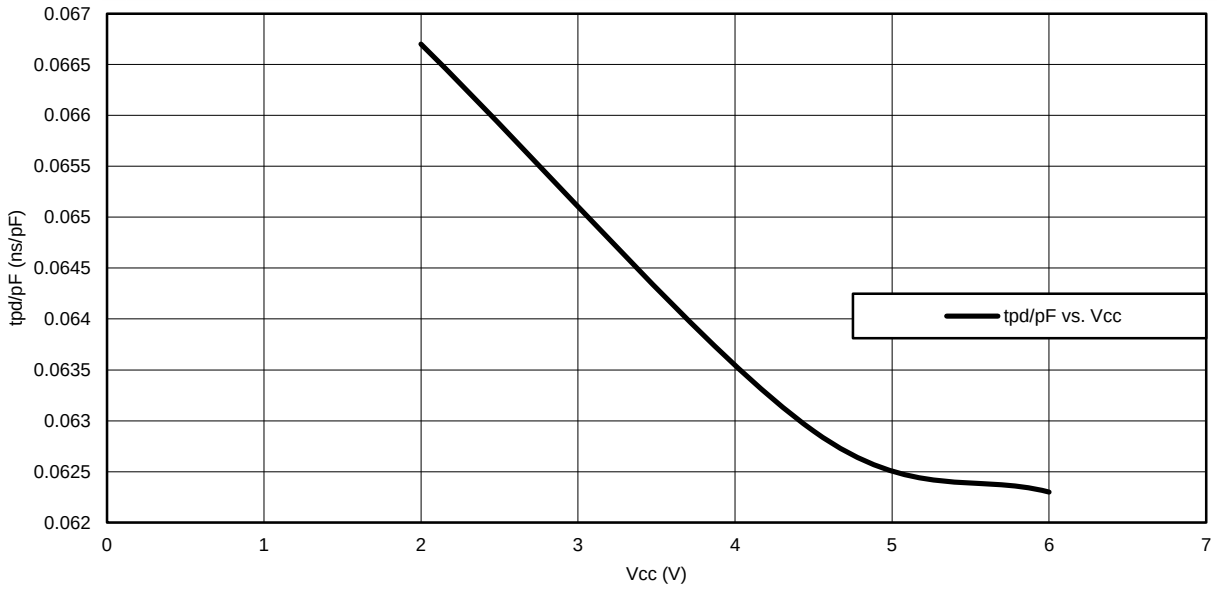

Figure 4. tpd/pF vs V_{CC} at 25°C

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF capacitor is recommended and if there are multiple V_{CC} pins then a 0.01-µF or 0.022-µF capacitor is recommended for each power pin. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs must not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient.

11.2 Layout Example

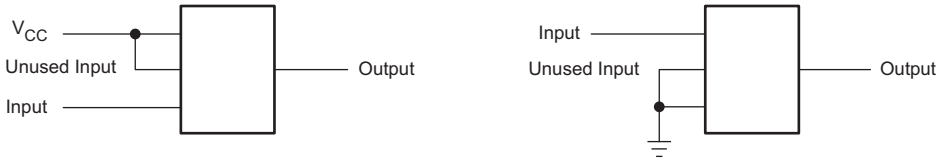

Figure 5. Layout Diagram

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *Implications of Slow or Floating CMOS Inputs*, SCBA004.
- *Introduction to Logic*, SLVA700

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54HC125	Click here	Click here	Click here	Click here	Click here
SN74HC125	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-87721012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-87721012A SNJ54HC125FK	Samples
5962-8772101CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8772101CA SNJ54HC125J	Samples
SN54HC125J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54HC125J	Samples
SN74HC125D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC125	Samples
SN74HC125DBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI	-40 to 85		
SN74HC125DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC125	Samples
SN74HC125DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC125	Samples
SN74HC125DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC125	Samples
SN74HC125DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	HC125	Samples
SN74HC125DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC125	Samples
SN74HC125DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC125	Samples
SN74HC125DT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC125	Samples
SN74HC125N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC125N	Samples
SN74HC125N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	-40 to 85		
SN74HC125NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC125N	Samples
SN74HC125NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC125	Samples
SN74HC125NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC125	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC125NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC125	Samples
SN74HC125PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	HC125	Samples
SN74HC125PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC125	Samples
SN74HC125PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC125	Samples
SN74HC125PWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC125	Samples
SN74HC125PWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC125	Samples
SNJ54HC125FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-87721012A SNJ54HC 125FK	Samples
SNJ54HC125J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8772101CA SNJ54HC125J	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54HC125, SN74HC125 :

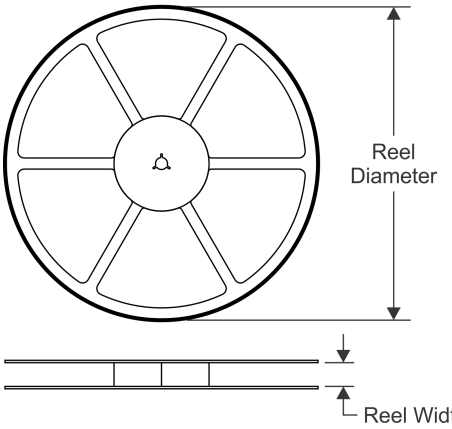
- Catalog: SN74HC125
- Automotive: SN74HC125-Q1, SN74HC125-Q1
- Military: SN54HC125

NOTE: Qualified Version Definitions:

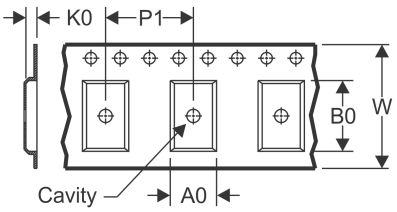
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

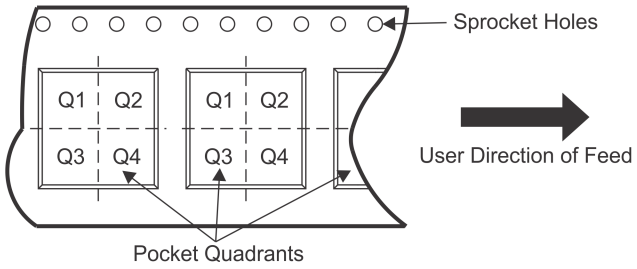


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

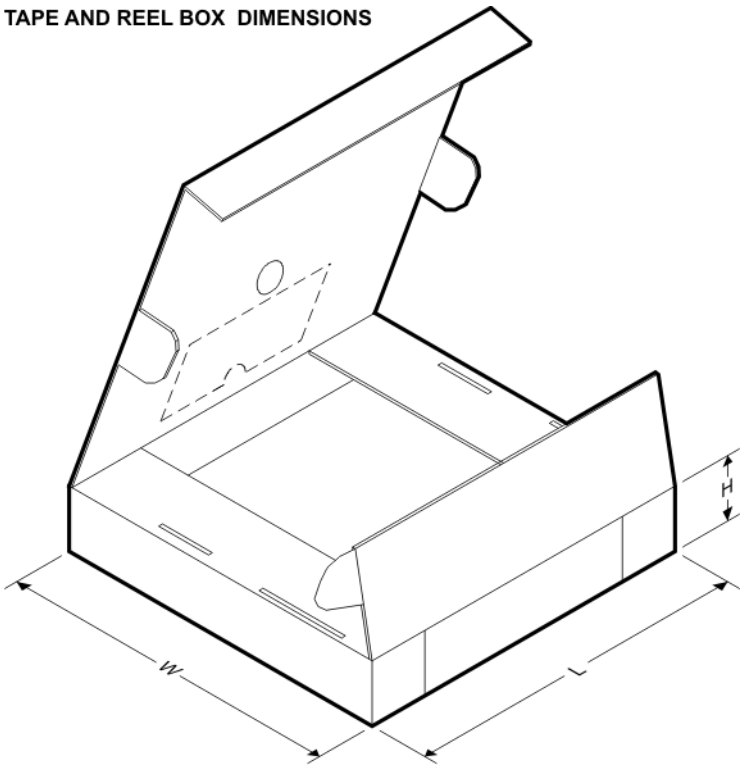
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC125DBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74HC125DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC125DR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.3	8.0	16.0	Q1
SN74HC125DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC125DT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC125PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC125PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC125PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC125PWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

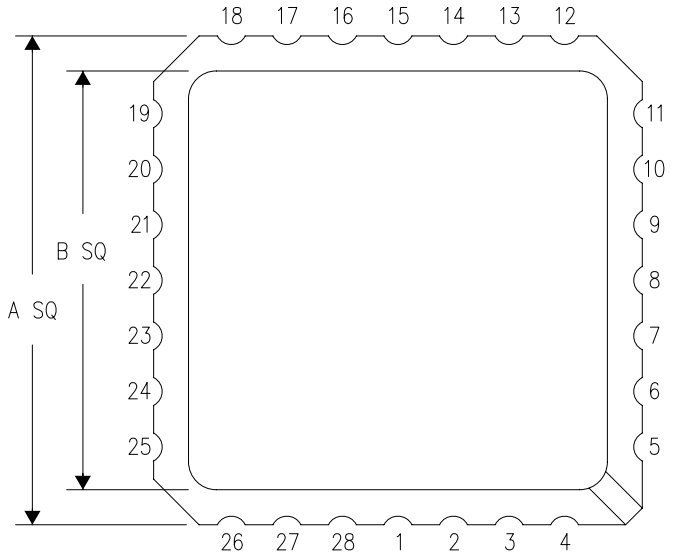


*All dimensions are nominal

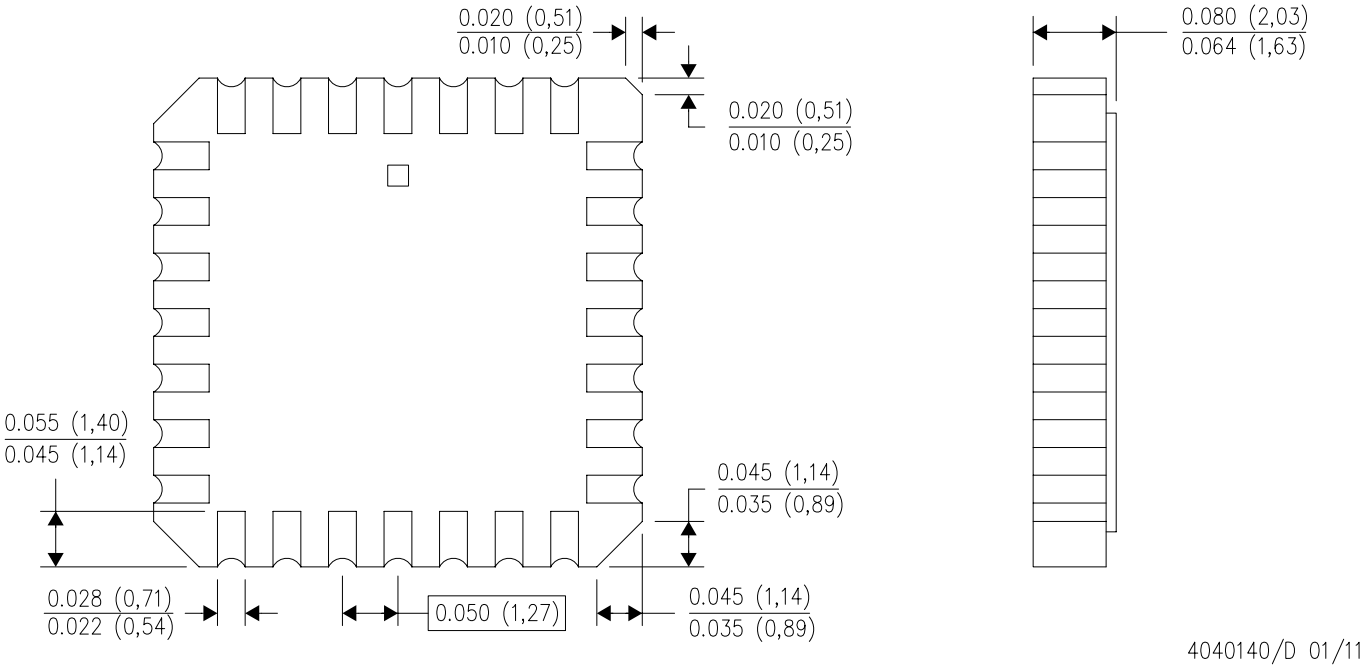
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC125DBR	SSOP	DB	14	2000	367.0	367.0	38.0
SN74HC125DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74HC125DR	SOIC	D	14	2500	364.0	364.0	27.0
SN74HC125DRG4	SOIC	D	14	2500	367.0	367.0	38.0
SN74HC125DT	SOIC	D	14	250	367.0	367.0	38.0
SN74HC125PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74HC125PWR	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74HC125PWRG4	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74HC125PWT	TSSOP	PW	14	250	367.0	367.0	35.0

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



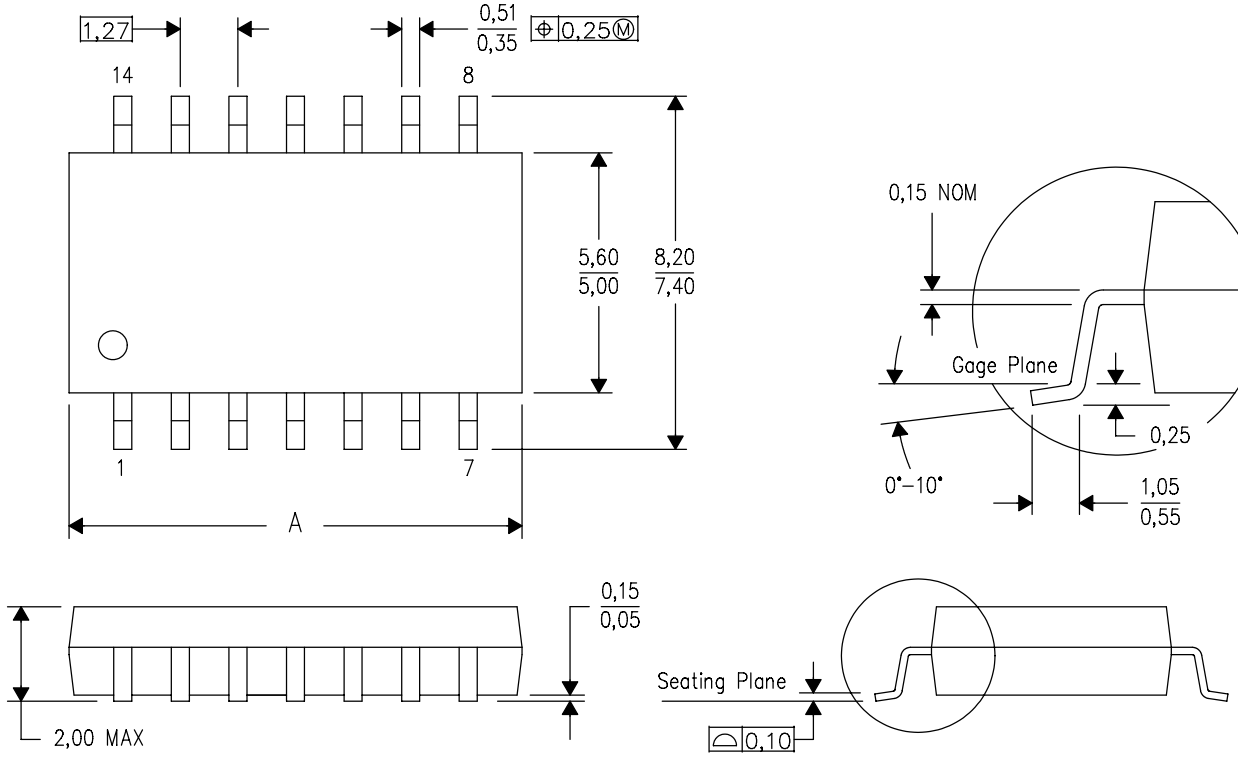
4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

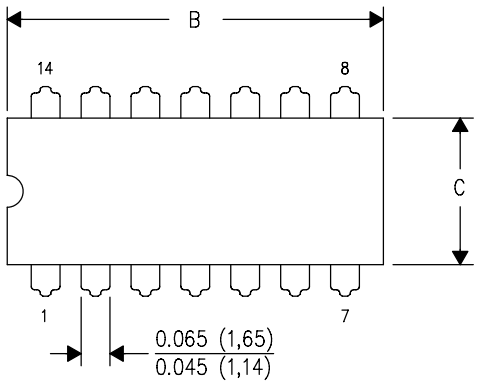
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

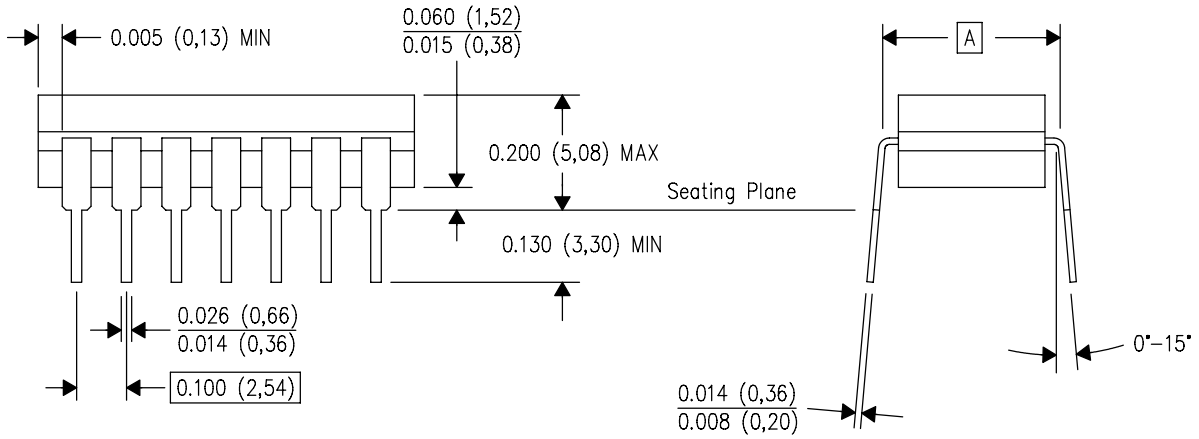
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



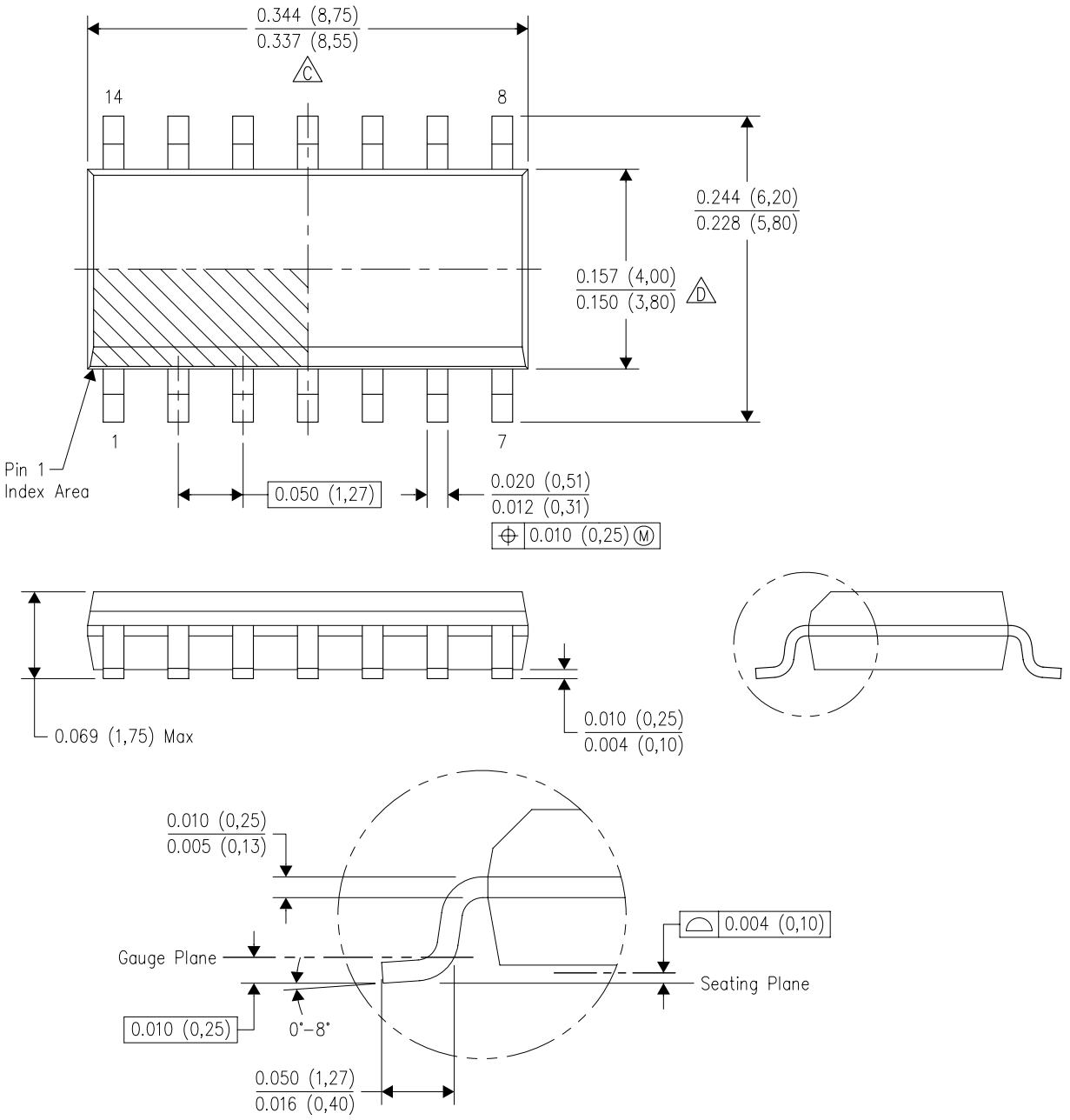
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

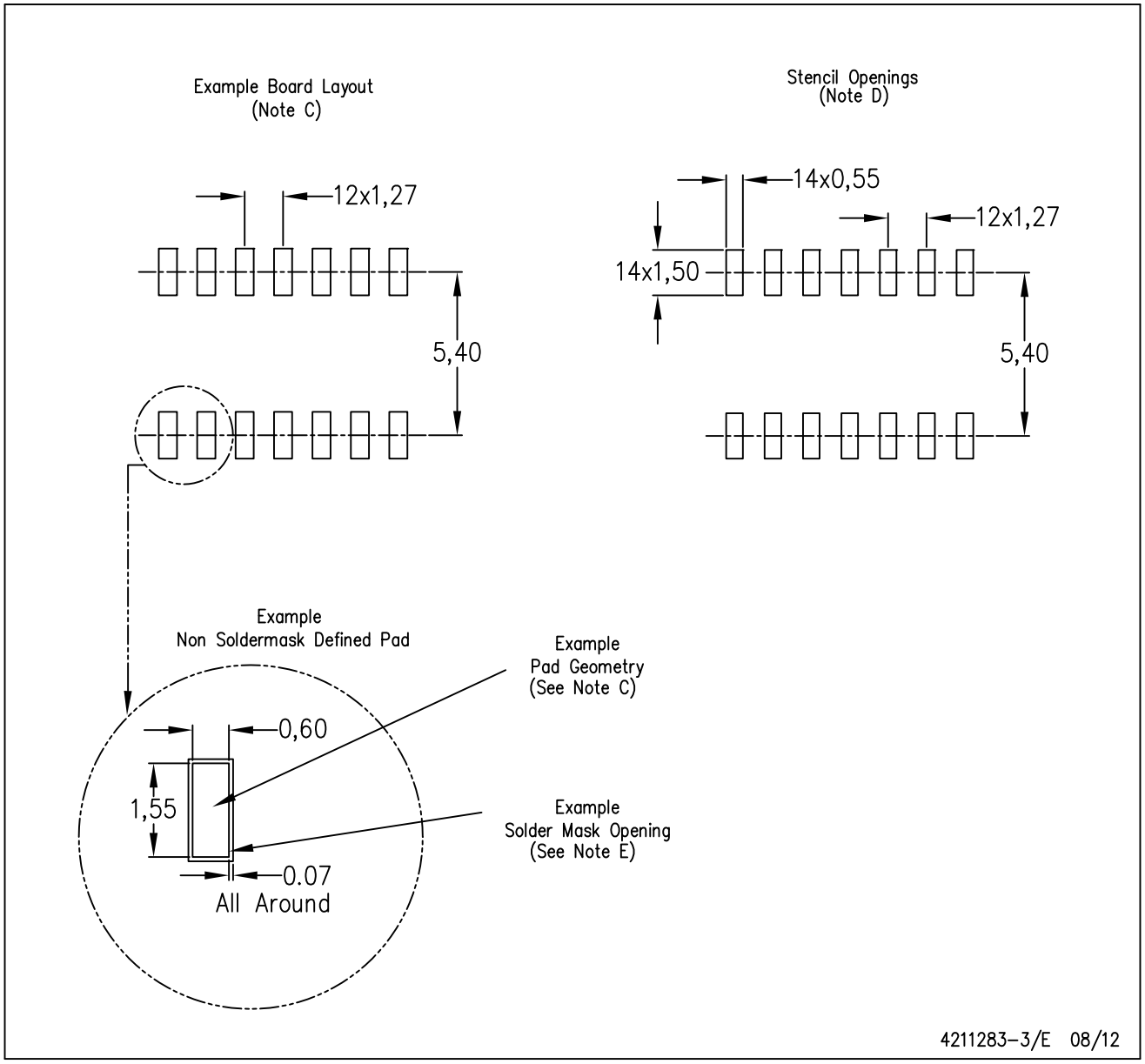
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

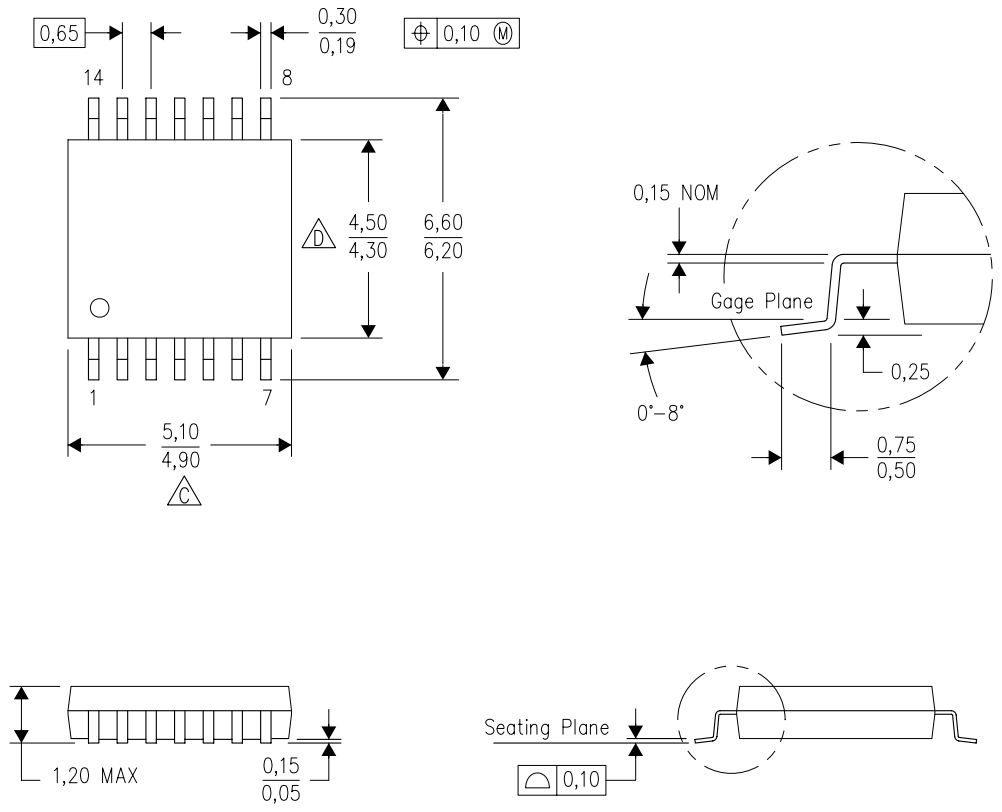
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

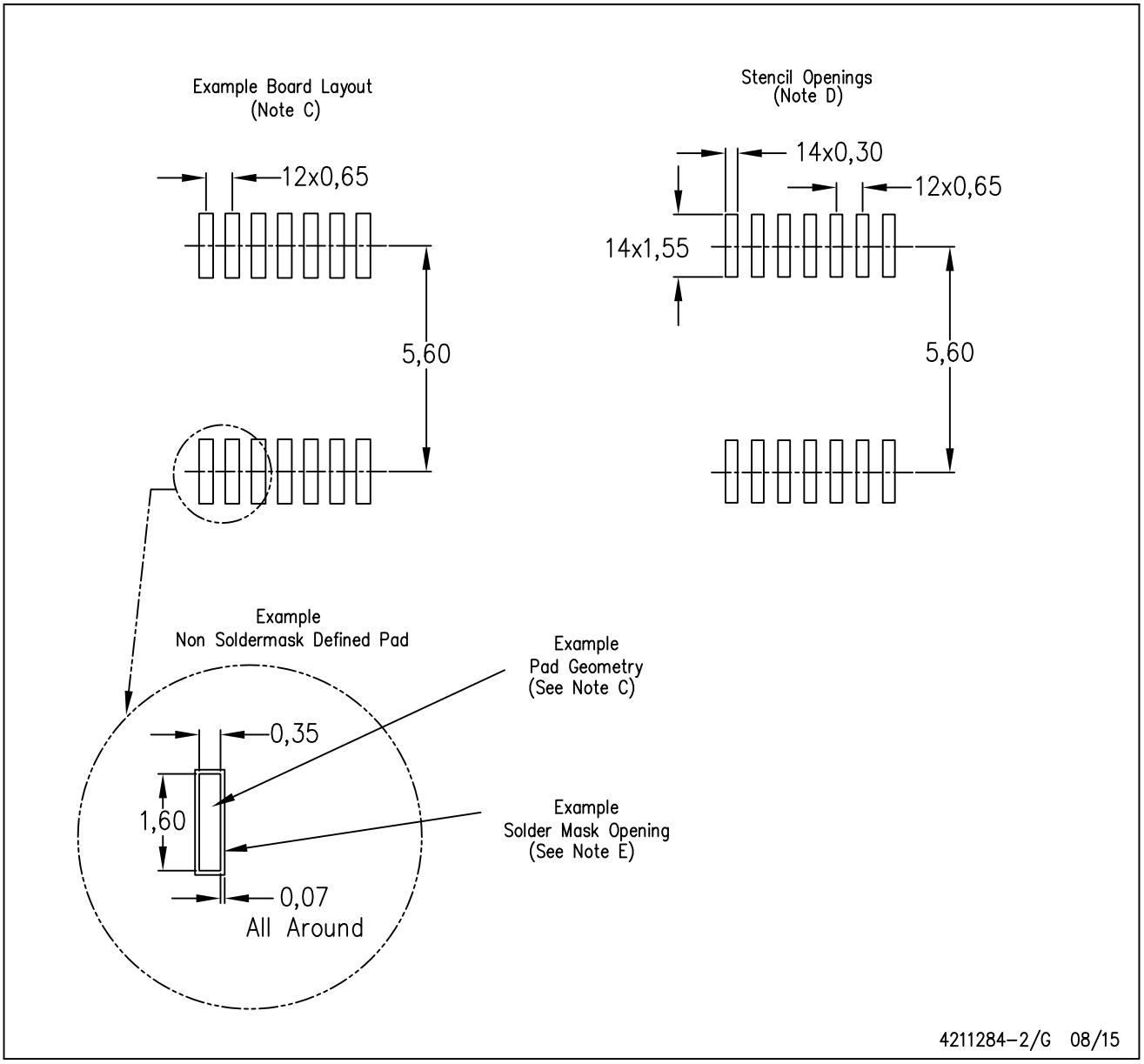
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

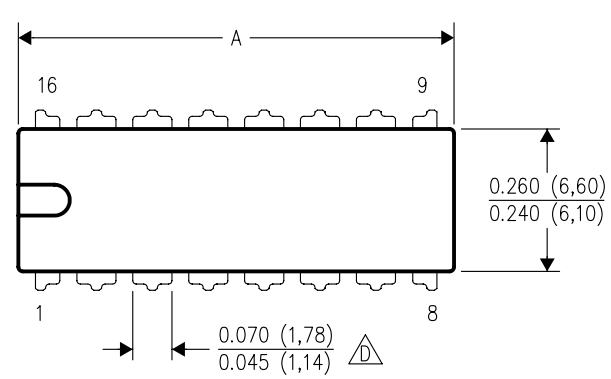


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

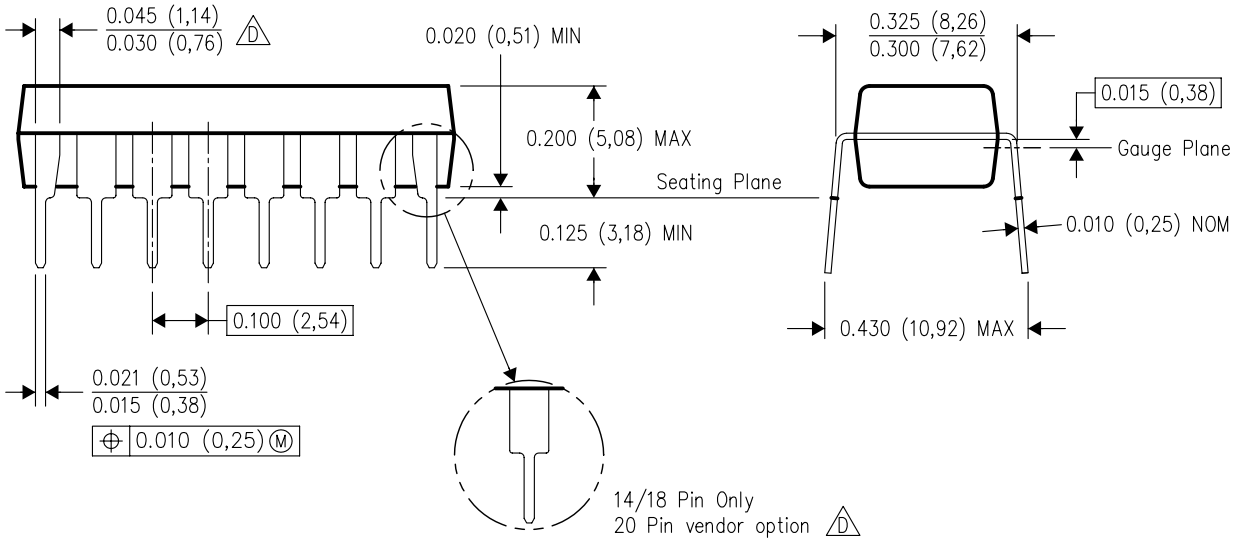
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



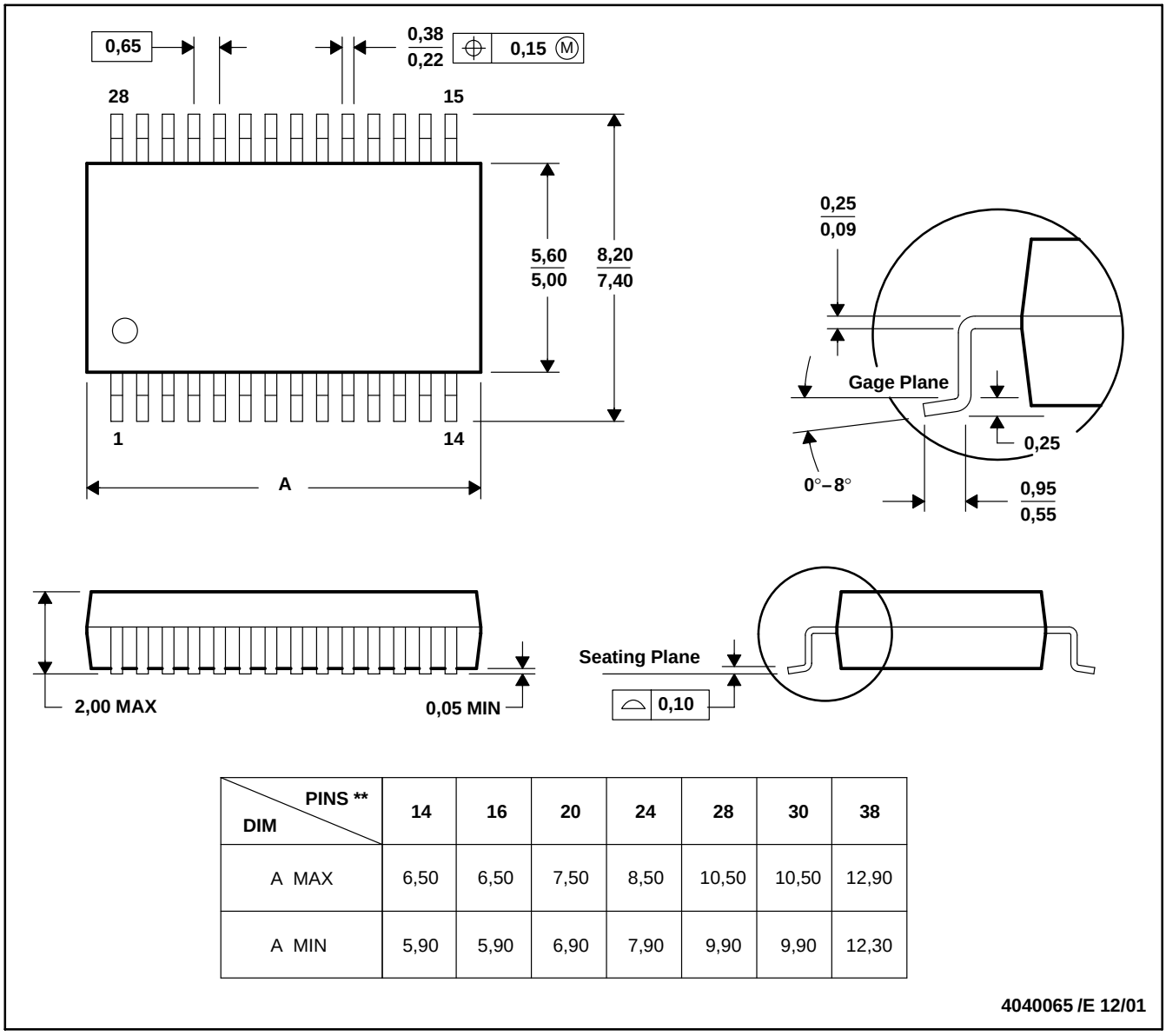
4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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