SN75LVDS83A Flatlink™ Transmitter

1 Features

- LVDS Display SerDes Interfaces Directly to LCD Display Panels with Integrated LVDS
- Package Options: 8.1 mm × 14 mm TSSOP
- 3.3-V Tolerant Data Inputs
- Transfer Rate up to 100 Mpps (Mega Pixel Per Second)
- Pixel Clock Frequency Range: 10 MHz to 100 MHz
- Suited for Display Resolutions Ranging From HVGA up to HD With Low EMI
- Operates From a Single 3.3-V Supply and 170 mW (Typical) at 75 MHz
- 28 Data Channels Plus Clock In Low-Voltage TTL to 4 Data Channels Plus Clock Out Low-Voltage Differential
- Consumes Less Than 1 mW When Disabled
- Selectable Rising or Falling Clock Edge Triggered Inputs
- ESD: 5000 V HBM
- Support Spread Spectrum Clocking (SSC)
- Compatible With all OMAP™ 2x, OMAP™ 3x, and DaVinci™ Application Processors

2 Applications

- Tablets
- Industrial PC, Laptop, and Other Factory Automation Displays
- Patient Monitor and Medical Equipment Displays
- Electronic Point-of-Sale (EPOS) Displays
- Printer Displays

3 Description

The SN75LVDS83A Flatlink™ transmitter device contains four 7-bit parallel-load serial-out shift registers, a 7× clock synthesizer, and five Low-Voltage Differential Signaling (LVDS) line drivers in a single integrated circuit. These functions allow 28 bits of single-ended LVTTL data to be synchronously transmitted over five balanced-pair conductors for receipt by a compatible receiver, such as the SN75LVDS82 and LCD panels with integrated LVDS receiver.

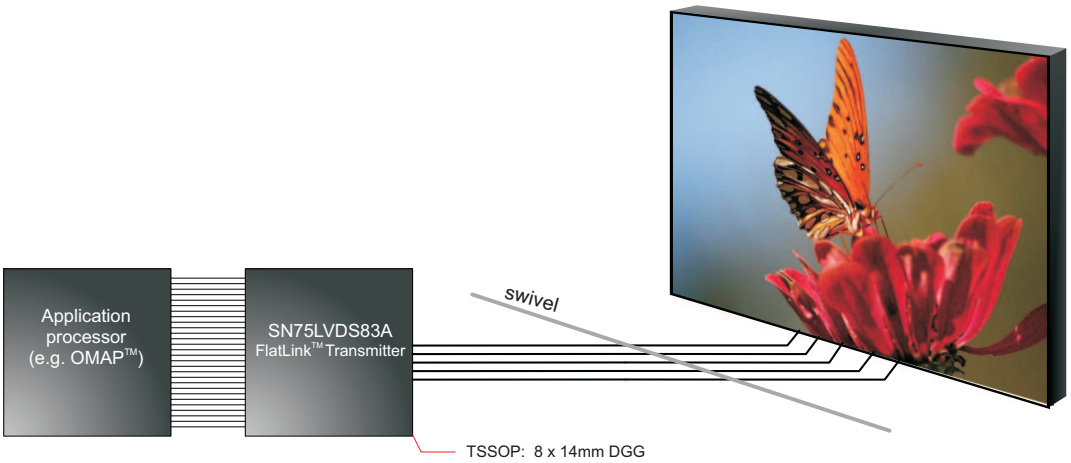
When transmitting, data bits D0 through D27 are each loaded into registers upon the edge of the input clock signal (CLKIN). The rising or falling edge of the clock can be selected via the clock select (CLKSEL) pin. The frequency of CLKIN is multiplied seven times, and then used to unload the data registers in 7-bit slices and serially. The four serial streams and a phase-locked clock (CLKOUT) are then output to LVDS output drivers. The frequency of CLKOUT is the same as the input clock, CLKIN.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN75LVDS83A	TSSOP (56)	14.00 mm × 6.10 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

LVDS Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (June 2011) to Revision E — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Deleted *Ordering Information* table; see POA at the end of the data sheet ... 1
- Added *Thermal Information* table ... 6

Changes from Revision C (August 2009) to Revision D — **Page**

- Changed *24-Bit Color Host to 24-bit LCD Panel Application Schematic* From: G7(LSB) To: G7(MSB) ... 18

Changes from Revision B (July 2009) to Revision C — **Page**

- Deleted sentence in the Pin Functions table for entry D0 - D27 - "supports 1.8V to 3.3V input voltage selectable by VDD supply." ... 4

Changes from Revision A (June 2009) to Revision B — **Page**

- Changed the data sheet From: Product Preview To: Production. ... 1

Changes from Original (June 2009) to Revision A — **Page**

- Changed Description text From: Alternative device option: The SN75LVDS83A is an alternative... To: Alternative device option: The SN75LVDS83B is an alternative... ... 3
- Changed *Typical PRBS Output Signal vs Over One Clock Period* graph ... 10

5 Description (continued)

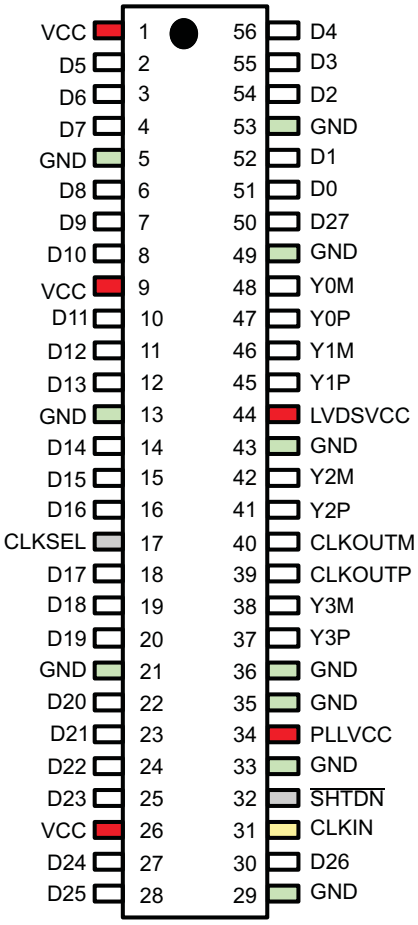
The SN75LVDS83A requires no external components and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user(s). The only user intervention is selecting a clock rising edge by inputting a high level to CLKSEL or a falling edge with a low-level input, and the possible use of the Shutdown/Clear ($\overline{SHTDN}$). $\overline{SHTDN}$ is an active-low input to inhibit the clock, and shut off the LVDS output drivers for lower power consumption. A low-level on this signal clears all internal registers to a low-level.

The SN75LVDS83A is characterized for operation over ambient air temperatures of –10°C to 70°C.

Alternative device option: The SN75LVDS83B is an alternative to the SN75LVDS83A for clock frequency range of 10 MHz to 135 MHz. The SN75LVDS83B is available in a smaller BGA package in addition to the TSSOP package.

6 Pin Configuration and Functions

DGG Package
56-Pin TSSOP
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
CLKIN	31	I	CMOS with pulldown; input pixel clock; rising or falling clock polarity is selectable by Control input CLKSEL.
CLKOUTM	40	O	Differential LVDS pixel clock output. Output is high-impedance when $\overline{\text{SHTDN}}$ is pulled low (de-asserted).
CLKOUTP	39	O	
CLKSEL	17	I	CMOS with pulldown; selects between rising edge input clock trigger (CLKSEL = V_{IH}) and falling edge input clock trigger (CLKSEL = V_{IL}).
D0	51	I	CMOS with pulldown; data inputs. To connect a graphic source successfully to a display, the bit assignment of D[27:0] is critical (and not necessarily intuitive). For input bit assignment, see Figure 14 to Figure 17 for details. Note: if application only requires 18-bit color, connect unused inputs D5, D10, D11, D16, D17, D23, and D27 to GND.
D1	52	I	
D2	54	I	
D3	55	I	
D4	56	I	
D5	2	I	
D6	3	I	
D7	4	I	
D8	6	I	
D9	7	I	
D10	8	I	
D11	10	I	
D12	11	I	
D13	12	I	
D14	14	I	
D15	15	I	
D16	16	I	
D17	18	I	
D18	19	I	
D19	20	I	
D20	22	I	
D21	23	I	
D22	24	I	
D23	25	I	
D24	27	I	
D25	28	I	
D26	30	I	
D27	50	I	
GND	5, 23, 21, 29, 43, 49, 53	P	Supply ground for VCC, LVDSVCC, and PLLVCC(2)
LVDSVCC	44	P	3.3-V LVDS output analog supply(2)
PLLVCC	34	P	3.3-V PLL analog supply(2)
$\overline{\text{SHTDN}}$	32	I	CMOS with pulldown; device shut down; pull low (deassert) to shut down the device (low power, resets all registers) and high (assert) for normal operation.
VCC	1, 9, 26	P	3.3-V digital supply voltage(2)
Y0M	48	O	Differential LVDS data outputs. Output is high-impedance when $\overline{\text{SHTDN}}$ is pulled low (deasserted).
Y0P	47	O	Differential LVDS data outputs. Output is high-impedance when $\overline{\text{SHTDN}}$ is pulled low (deasserted).

(1) I = Input, O = Output, P = Power
(2) For a multi-layer PCB, TI recommends keeping one common GND layer underneath the device and connecting all ground terminals directly to this plane.

Pin Functions (continued)

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
Y1M	46	O	Differential LVDS data outputs. Output is high-impedance when $\overline{\text{SHTDN}}$ is pulled low (deasserted).
Y1P	45	O	Differential LVDS data outputs. Output is high-impedance when $\overline{\text{SHTDN}}$ is pulled low (deasserted).
Y2M	42	O	Differential LVDS data outputs. Output is high-impedance when $\overline{\text{SHTDN}}$ is pulled low (deasserted).
Y2P	41	O	Differential LVDS data outputs. Output is high-impedance when $\overline{\text{SHTDN}}$ is pulled low (deasserted).
Y3M	38	O	Differential LVDS Data outputs. Output is high-impedance when $\overline{\text{SHTDN}}$ is pulled low (deasserted). Note: If the application only requires 18-bit color, this output can be left open.
Y3P	37	O	Differential LVDS Data outputs. Output is high-impedance when $\overline{\text{SHTDN}}$ is pulled low (deasserted). Note: If the application only requires 18-bit color, this output can be left open.

7 Specifications

7.1 Absolute Maximum Ratings(1)

	MIN	MAX	UNIT
Supply voltage, VCC, LVDSVCC, PLLVCC(2)	–0.5	4	V
Voltage at any output terminal	–0.5	VCC + 0.5	V
Voltage at any input terminal	–0.5	VCC + 0.5	V
Continuous power dissipation	See *Dissipation Ratings*		
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the GND terminals.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)(1)	±5000	V
		Charged-device model (CDM)(2)	±500	
		Machine model (MM)(3)	±150	

(1) In accordance with JEDEC Standard 22, Test Method A114-A.
(2) In accordance with JEDEC Standard 22, Test Method C101.
(3) In accordance with JEDEC Standard 22, Test Method A115-A.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VCC	Supply voltage	3	3.3	3.6	V
LVDSVCC	LVDS output supply voltage	3	3.3	3.6	V
PLLVCC	PLL analog supply voltage	3	3.3	3.6	V
	Power supply noise on any VCC terminal			0.1	V
V_{IH}	High-level input voltage	VCC/2 + 0.5			V
V_{IL}	Low-level input voltage			VCC/2 – 0.5	V
Z_L	Differential load impedance	90		132	Ω
T_A	Operating free-air temperature	–10		70	°C

7.4 Thermal Information

THERMAL METRIC(1)		SN75LVDS83A DGG (TSSOP) 56 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	62.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	30.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_T	Input voltage threshold	R_L = 100 Ω, see Figure 6		VCC/2		V
$\|V_{OD}\|$	Differential steady-state output voltage magnitude	R_L = 100 Ω, see Figure 6	250		450	mV
$\Delta\|V_{OD}\|$	Change in the steady-state differential output voltage magnitude between opposite binary states	R_L = 100 Ω, see Figure 6		1	35	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	$t_{R/F}$ (Dx, CLKin) = 1 ns, see Figure 6	1.125		1.375	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	$t_{R/F}$ (Dx, CLKin) = 1 ns, see Figure 6			100	mV
I_{IH}	High-level input current	V_{IH} = VCC			25	µA
I_{IL}	Low-level input current	V_{IL} = 0 V			±10	µA
I_{OS}	Short-circuit output current	V_{OY} = 0 V			±24	mA
		V_{OD} = 0 V			±12	mA
I_{OZ}	High-impedance state output current	V_O = 0 V to VCC			±20	µA
R_{pdn}	Input pulldown integrated resistor on all inputs	Dx, CLKSEL, $\overline{SHTDN}$, CLKIN		100		kΩ
I_Q	Quiescent current	$\overline{SHTDN}$ = V_{IL}, disabled, all inputs at GND		2	100	µA
I_{CC}	Supply current (average)	$\overline{SHTDN}$ = V_{IH}, R_L = 100 Ω (5 places), grayscale pattern (Figure 7) VCC = 3.3 V, f_{CLK} = 75 MHz		52.3	62.2	mA
		$\overline{SHTDN}$ = V_{IH}, R_L = 100 Ω (5 places), 50% transition density pattern (Figure 7), VCC = 3.3 V, f_{CLK} = 75 MHz		53.9	67.1	mA
		$\overline{SHTDN}$ = V_{IH}, R_L = 100 Ω (5 places), worst-case pattern (Figure 8), VCC = 3.6 V, f_{CLK} = 75 MHz		65	79.3	mA
		$\overline{SHTDN}$ = V_{IH}, R_L = 100 Ω (5 places), worst-case pattern (Figure 8), f_{CLK} = 100 MHz			96.8	mA
C_I	Input capacitance			2		pF

(1) All typical values are at VCC = 3.3 V, T_A = 25°C.

7.6 Dissipation Ratings

PACKAGE	CIRCUIT BOARD MODEL(1)	T_{JA} ≤ 25°C	DERATING FACTOR(2) ABOVE T_{JA} = 25°C	T_{JA} = 70°C POWER RATING
DGG	Low-K	1111 mW	12.3 mW/°C	555 mW
	High-K	1730 mW	19 mW/°C	865 mW

(1) In accordance with the High-K and Low-K thermal metric definitions of EIA/JESD51-2.
(2) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

7.7 Timing Requirements

			MIN	MAX	UNIT
t_c	Input clock period		10	100	ns
	Input clock modulation (SSC)	with modulation frequency 30 kHz		8%	
		with modulation frequency 50 kHz		6%	
t_w	High-level input clock pulse width duration		0.4 × t_c	0.6 × t_c	ns
t_t	Input signal transition time			3	ns
	Data set up time, D0 through D27 before CLKIN (see Figure 5)		2		ns
	Data hold time, D0 through D27 after CLKIN		0.8		ns

7.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_0	Delay time, CLKOUT↑ after Yn valid (serial bit position 0, equal D1, D9, D20, D5)	t_C = 10 ns, |Input clock jitter| < 25 ps (see Figure 9)(2)	–0.1	0	0.1	ns
t_1	Delay time, CLKOUT↑ after Yn valid (serial bit position 1, equal D0, D8, D19, D27)	t_C = 10 ns, |Input clock jitter| < 25 ps (see Figure 9)(2)	$^1/_7$ t_c – 0.1		$^1/_7$ t_c + 0.1	ns
t_2	Delay time, CLKOUT↑ after Yn valid (serial bit position 2, equal D7, D18, D26. D23)	t_C = 10 ns, |Input clock jitter| < 25 ps (see Figure 9)(2)	$^2/_7$ t_c – 0.1		$^2/_7$ t_c + 0.1	ns
t_3	Delay time, CLKOUT↑ after Yn valid (serial bit position 3; equal D6, D15, D25, D17)	t_C = 10 ns, |Input clock jitter| < 25 ps (see Figure 9)(2)	$^3/_7$ t_c – 0.1		$^3/_7$ t_c + 0.1	ns
t_4	Delay time, CLKOUT↑ after Yn valid (serial bit position 4, equal D4, D14, D24, D16)	t_C = 10 ns, |Input clock jitter| < 25 ps (see Figure 9)(2)	$^4/_7$ t_c – 0.1		$^4/_7$ t_c + 0.1	ns
t_5	Delay time, CLKOUT↑ after Yn valid (serial bit position 5, equal D3, D13, D22, D11)	t_C = 10 ns, |Input clock jitter| < 25 ps (see Figure 9)(2)	$^5/_7$ t_c – 0.1		$^5/_7$ t_c + 0.1	ns
t_6	Delay time, CLKOUT↑ after Yn valid (serial bit position 6, equal D2, D12, D21, D10)	t_C = 10 ns, |Input clock jitter| < 25 ps (see Figure 9)(2)	$^6/_7$ t_c – 0.1		$^6/_7$ t_c + 0.1	ns
$t_{sk(o)}$	Output skew, t_n - $^n/_7$ t_C	Target potential adjustment after characteristic	–0.1 (–0.15)		0.1 (0.15)	ns
$t_{c(o)}$	Output clock period			t_c		ns
$\Delta t_{c(o)}$	Output clock cycle-to-cycle jitter(3)	t_C = 10 ns, clean reference clock (see Figure 10)		±40		ps
		t_C = 10 ns with 0.05 UI added noise modulated at 3 MHz (see Figure 10)		±44		
		t_C = 10 ns with 0.1 UI added noise modulated at 3 MHz (see Figure 10)		±42		
t_w	High-level output clock pulse duration			$^4/_7$ t_c		ns
$t_{r/f}$	Differential output voltage transition time (t_r or t_f)	fCLK (see Figure 6)		225	500	ps
t_{en}	Enable time, $\overline{SHTDN}$↑ to phase lock (Yn valid)	f_{CLK} = 100 MHz (see Figure 11)		6		ms
t_{dis}	Disable time, $\overline{SHTDN}$↓ to off-state (CLKOUT high-impedance)	f_{CLK} = 100 MHz (see Figure 12)		7		ns

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) |Input clock jitter| is the magnitude of the change in the input clock period.
(3) The output clock cycle-to-cycle jitter is the largest recorded change in the output clock period from one cycle to the next cycle observed over 15,000 cycles. Tektronix TDSJIT3 Jitter Analysis software was used to derive the maximum and minimum jitter value.

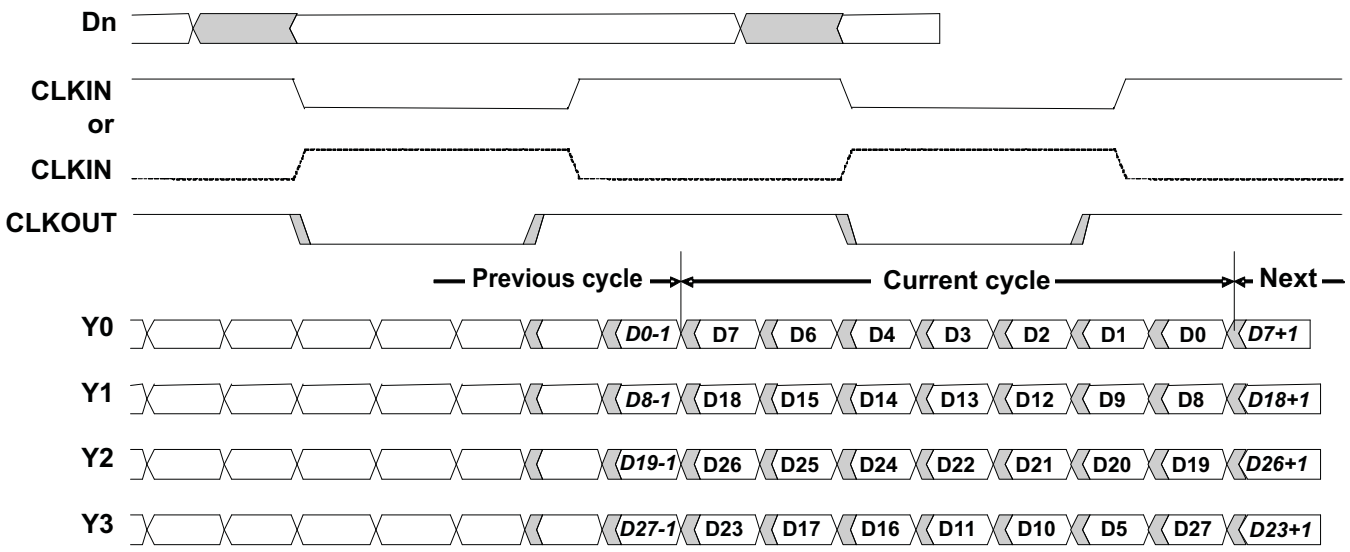


Figure 1. Typical SN75LVDS83A Load and Shift Sequences

7.9 Typical Characteristics

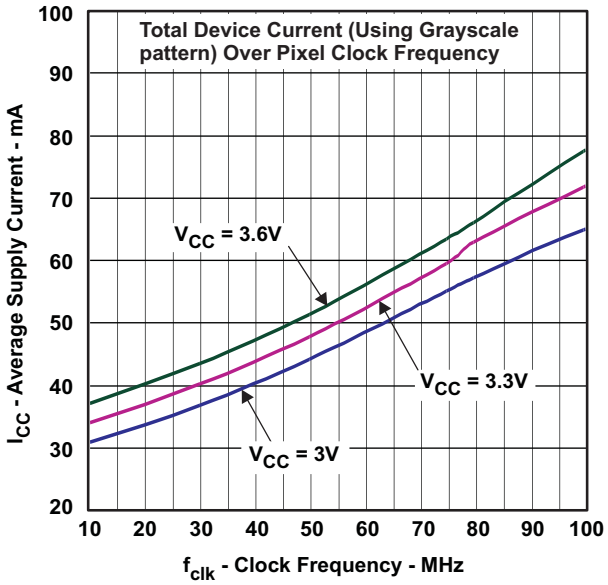


Figure 2. Average Grayscale ICC vs Clock Frequency

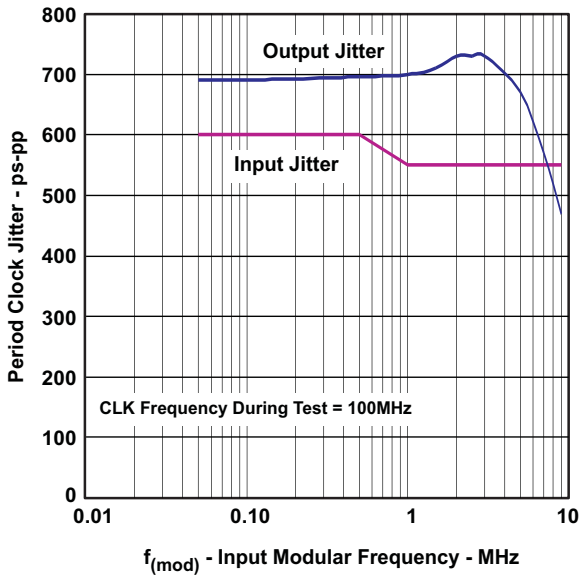


Figure 3. Output Clock Jitter vs Input Clock Jitter

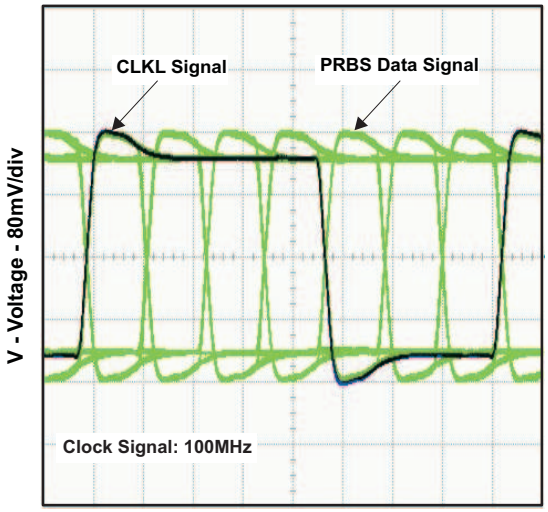
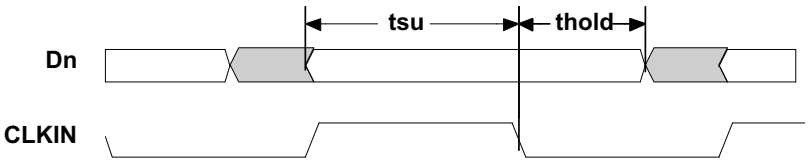


Figure 4. Typical PRBS Output Signal vs Over One Clock Period

8 Parameter Measurement Information



All input timing is defined at IOVDD / 2 on an input signal with a 10% to 90% rise or fall time of less than 3 ns. CLKSEL = 0 V.

Figure 5. Set Up and Hold Time Definition

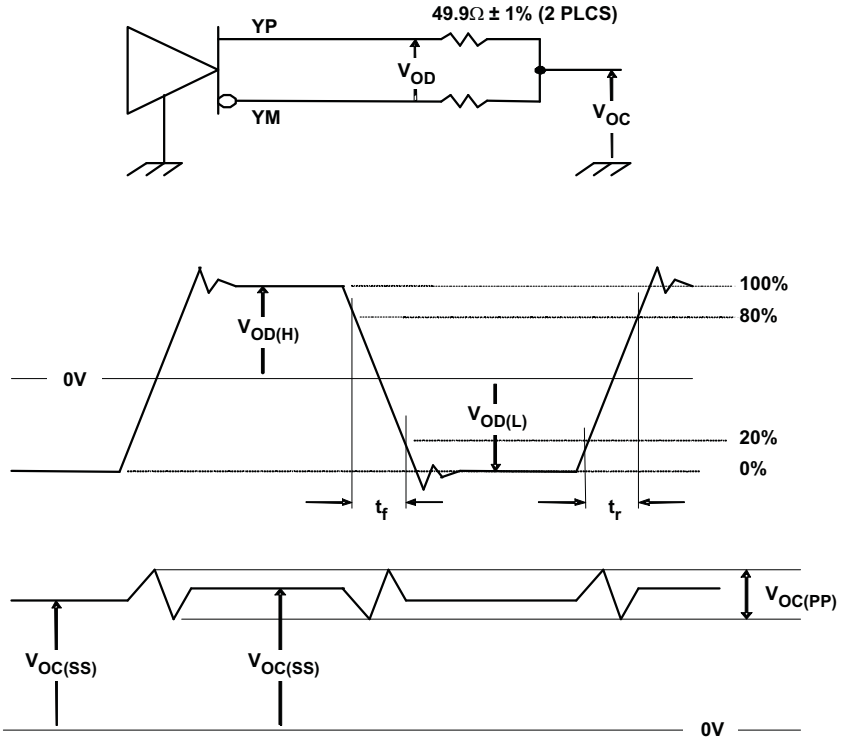
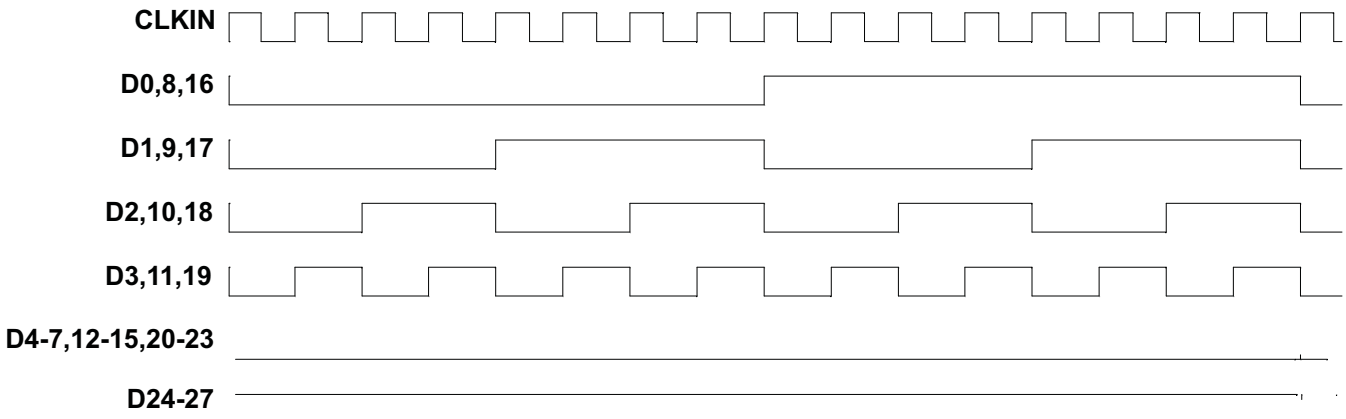


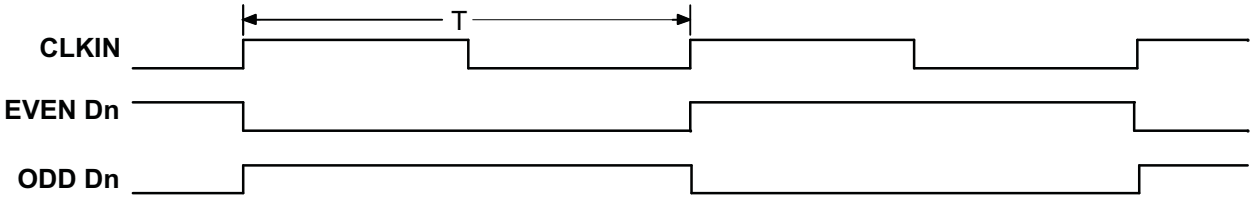
Figure 6. Test Load and Voltage Definitions for LVDS Outputs



The 16 grayscale test pattern test device power consumption for a typical display pattern.

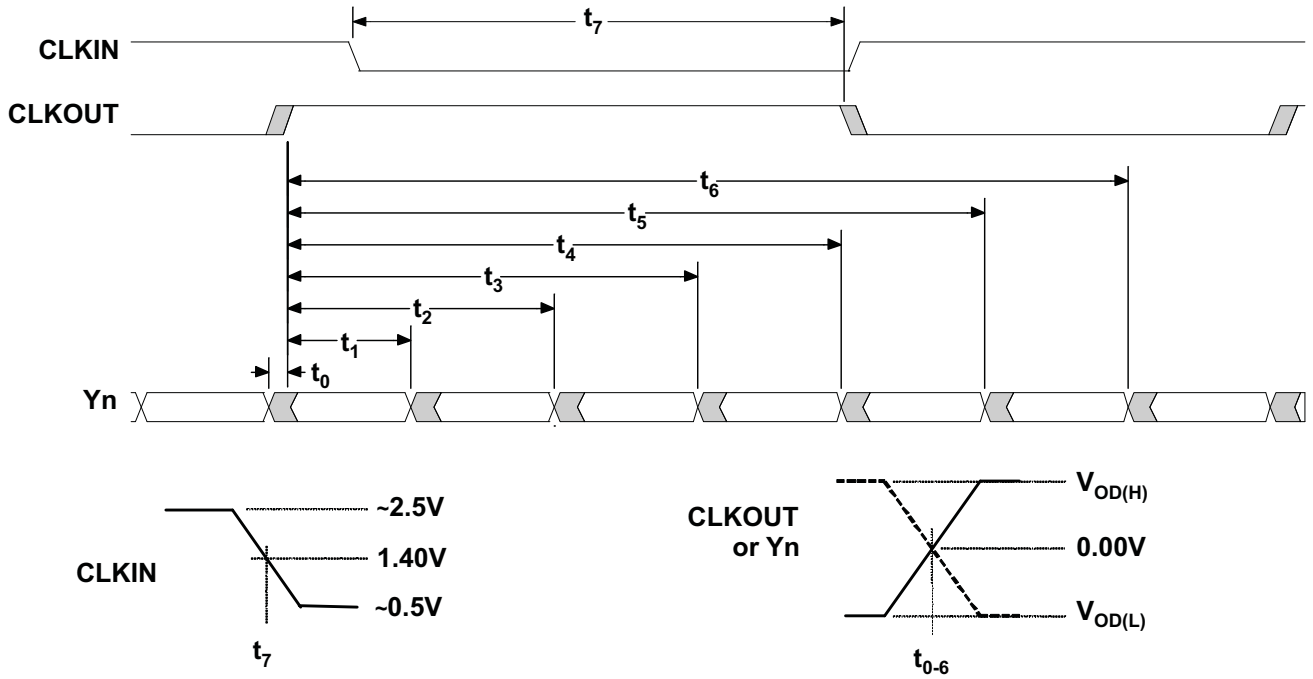
Figure 7. 16 Grayscale Test Pattern

Parameter Measurement Information (continued)



The worst-case test pattern produces nearly the maximum switching frequency for all of the LVDS outputs.

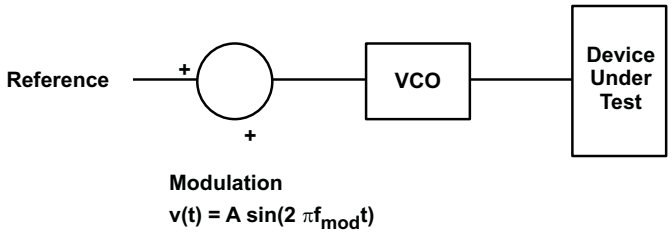
Figure 8. Worst-Case Power Test Pattern



CLKOUT is shown with CLKSEL at high-level.
CLKIN polarity depends on CLKSEL input level.

Figure 9. SN75LVDS83A Timing Definitions

Parameter Measurement Information (continued)



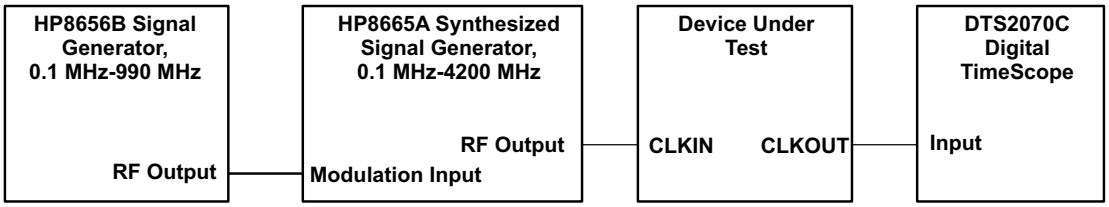


Figure 10. Output Clock Jitter Test Set Up

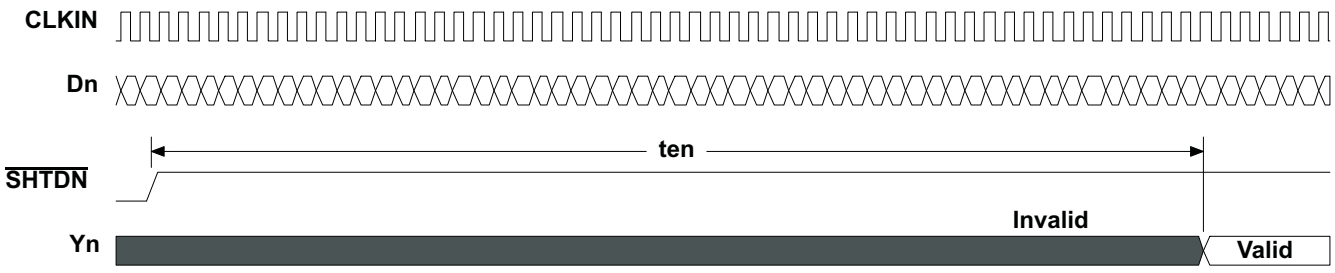


Figure 11. Enable Time Waveforms

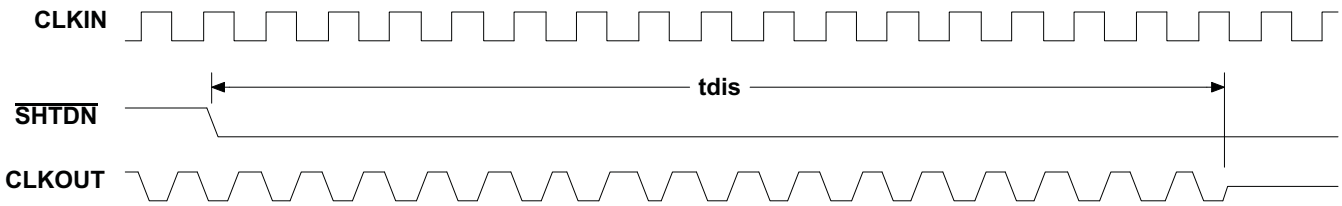


Figure 12. Disable Time Waveforms

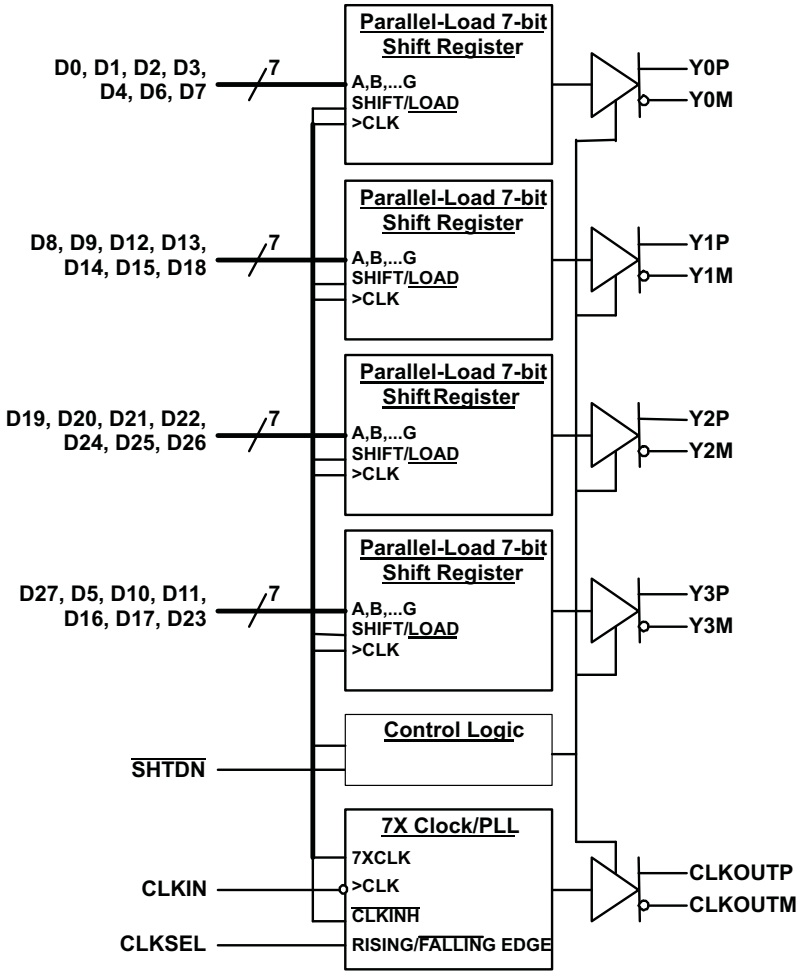
9 Detailed Description

9.1 Overview

The Flatlink™ is a LVDS SerDes data transmission system. The SN75LVDS83A device takes in three (or four) data words each containing seven single-ended data bits and converts this to an LVDS serial output. Each serial output runs at seven times that of the parallel data rate. The deserializer (receiver) device operates in the reverse manner. The three (or four) LVDS serial inputs are transformed back to the original seven-bit parallel single-ended data. Flatlink™ devices are available in 21:3 or 28:4 SerDes ratios.

The 21-bit devices are designed for 6-bit RGB video for a total of 18 bits in addition to three extra bits for horizontal synchronization, vertical synchronization, and data enable. The 28-bit devices are intended for 8-bit RGB video applications. Again, the extra four bits are for horizontal synchronization, vertical synchronization, data enable, and the remaining is the reserved bit. These 28-bit devices can also be used in 6-bit and 4-bit RGB applications as shown in the subsequent system diagrams.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 TTL Input Data

The data inputs to the transmitter come from the graphics processor and consist of up to 24 bits of video information, a horizontal synchronization bit, a vertical synchronization bit, an enable bit, and a spare bit.

The data can be loaded into the registers upon either the rising or falling edge of the input clock selectable by the CLKSEL pin. Data inputs are 1.8 V to 3.3 V tolerant for the SN75LVDS83A and can connect directly to low-power, low-voltage application and graphic processors. The bit mapping is listed in Table 1.

Table 1. Pixel Bit Ordering

	RED	GREEN	BLUE
LSB	R0	G0	B0
	R1	G1	B1
	R2	G2	B2
4-bit MSB	R3	G3	B3
	R4	G4	B4
6-bit MSB	R5	G5	B5
	R6	G6	B6
8-bit MSB	R7	G7	B7

9.3.2 LVDS Output Data

The pixel data assignment is listed in Table 2 for 24-bit, 18-bit, and 12-bit color hosts.

Table 2. Pixel Data Assignment

SERIAL CHANNEL	DATA BITS	8-BIT			6-BIT	4-BIT	
		FORMAT-1(1)	FORMAT-2(2)	FORMAT-3(3)		NON-LINEAR STEP SIZE(4)	LINEAR STEP SIZE(5)
Y0	D0	R0	R2	R2	R0	R2	VCC
	D1	R1	R3	R3	R1	R3	GND
	D2	R2	R4	R4	R2	R0	R0
	D3	R3	R5	R5	R3	R1	R1
	D4	R4	R6	R6	R4	R2	R2
	D6	R5	R7	R7	R5	R3	R3
	D7	G0	G2	G2	G0	G2	VCC
Y1	D8	G1	G3	G3	G1	G3	GND
	D9	G2	G4	G4	G2	G0	G0
	D12	G3	G5	G5	G3	G1	G1
	D13	G4	G6	G6	G4	G2	G2
	D14	G5	G7	G7	G5	G3	G3
	D15	B0	B2	B2	B0	B2	VCC
	D18	B1	B3	B3	B1	B3	GND

(1) 2 MSBs of each color transmitted over 4th serial data channel (Y3). Dominant data format for LCD panel.
(2) 2 LSBs of each color transmitted over 4th serial data channel. System designer needs to verify the data format by checking with the LCD display data sheet.
(3) 24-bit color host to 18-bit color LCD panel display application.
(4) Increased dynamic range of the entire color space at the expense of non-linear step sizes between each step.
(5) Linear step size with less dynamic range.

Table 2. Pixel Data Assignment (continued)

SERIAL CHANNEL	DATA BITS	8-BIT			6-BIT	4-BIT	
		FORMAT-1(1)	FORMAT-2(2)	FORMAT-3(3)		NON-LINEAR STEP SIZE(4)	LINEAR STEP SIZE(5)
Y2	D19	B2	B4	B4	B2	B0	B0
	D20	B3	B5	B5	B3	B1	B1
	D21	B4	B6	B6	B4	B2	B2
	D22	B5	B7	B7	B5	B3	B3
	D24	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
	D25	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
	D26	ENABLE	ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
Y3	D27	R6	R0	GND	GND	GND	GND
	D5	R7	R1	GND	GND	GND	GND
	D10	G6	G0	GND	GND	GND	GND
	D11	G7	G1	GND	GND	GND	GND
	D16	B6	B0	GND	GND	GND	GND
	D17	B7	B1	GND	GND	GND	GND
	D23	RSVD	RSVD	GND	GND	GND	GND
CLKOUT	CLKIN	CLK	CLK	CLK	CLK	CLK	CLK

9.4 Device Functional Modes

9.4.1 Input Clock Edge

The transmission of data bits D0 through D27 occurs as each are loaded into registers upon the edge of the CLKIN signal, where the rising or falling edge of the clock may be selected through CLKSEL. The selection of a clock rising edge occurs by inputting a high level to CLKSEL, which is achieved by populating pullup resistor to pull CLKSEL is high. Inputting a low level to select a clock falling edge is achieved by directly connecting CLKSEL to GND.

9.4.2 Low Power Mode

The SN75LVDS83A can be put in low-power consumption mode by active-low input SHTDN#.

Connecting terminal SHTDN to GND inhibits the clock and shut off the LVDS output drivers for lower power consumption. A low level on this signal clears all internal registers to a low level.

Populate a pullup to VCC on SHTDN# to enable the device for normal operation.

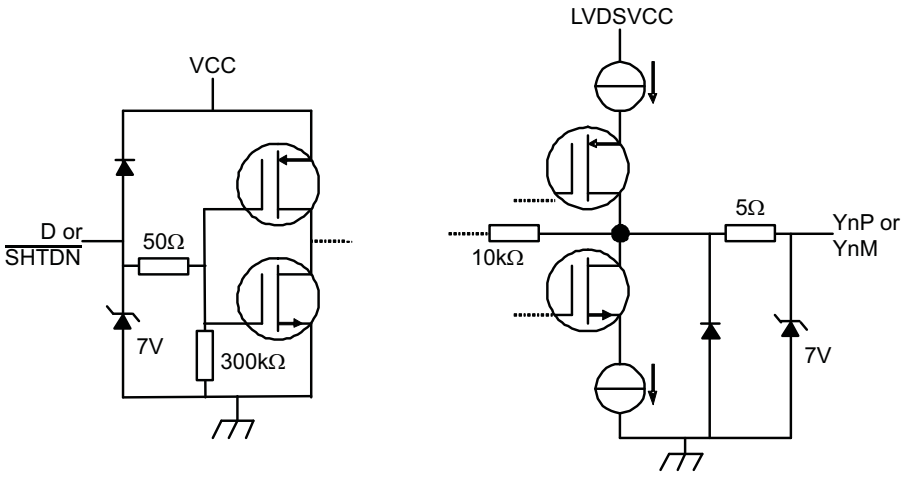


Figure 13. Equivalent Input and Output Schematic Diagrams

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

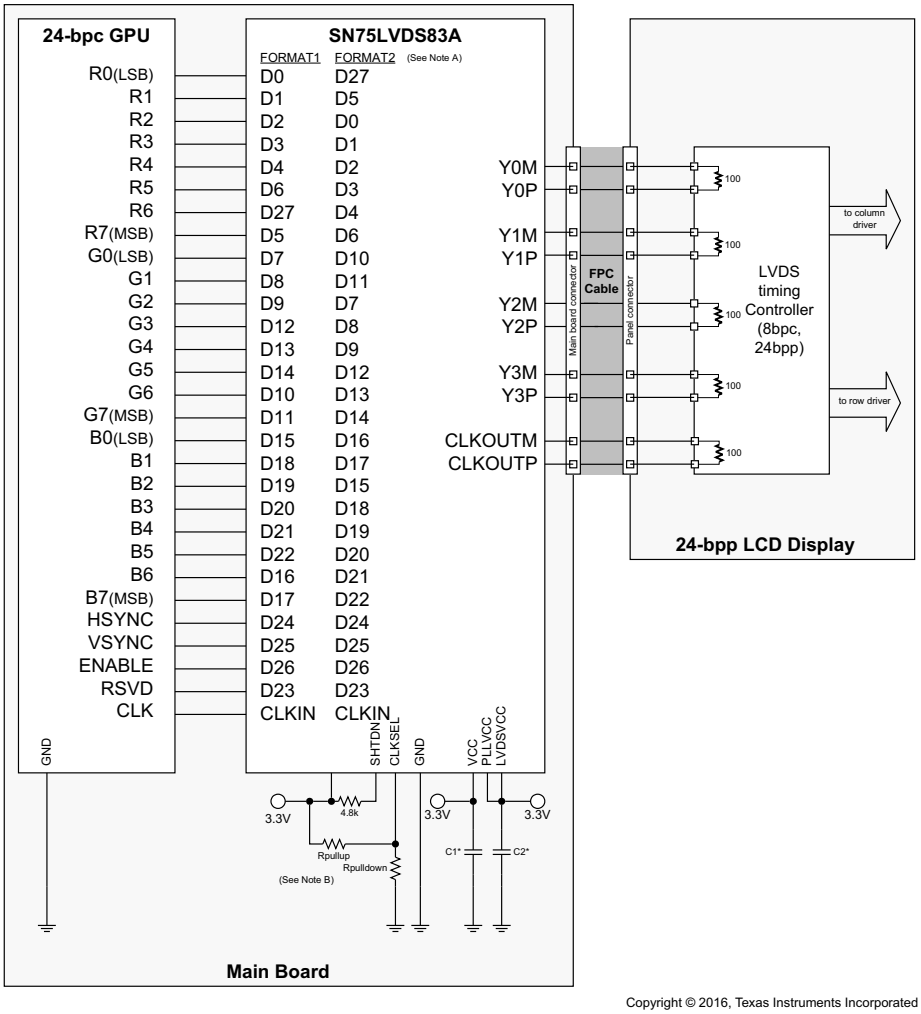
10.1 Application Information

This section provides information on device connectivity to various GPU and LCD display panels, and offers a PCB routing example.

10.1.1 Signal Connectivity

While there is no formal industry standardized specification for the input interface of LVDS LCD panels, the industry has aligned over the years on a certain data format (bit order). Figure 14 through Figure 17 show how each signal must be connected from the graphic source through the SN75LVDS83A input, output, and LVDS LCD panel input. Detailed notes are provided with each figure.

Application Information (continued)



A. **FORMAT:** The majority of 24-bit LCD display panels require the two most significant bits (2 MSB) of each color to be transferred over the 4th serial data output Y3. A few 24-bit LCD display panels require the two LSBs of each color to be transmitted over the Y3 output. The system designer needs to verify which format is expected by checking the LCD display data sheet. **Format 1:** Use with displays expecting the 2 MSB to be transmitted over the 4th data channel Y3. This is the dominate data format for LCD panels. **Format 2:** Use with displays expecting the 2 LSB to be transmitted over the 4th data channel.

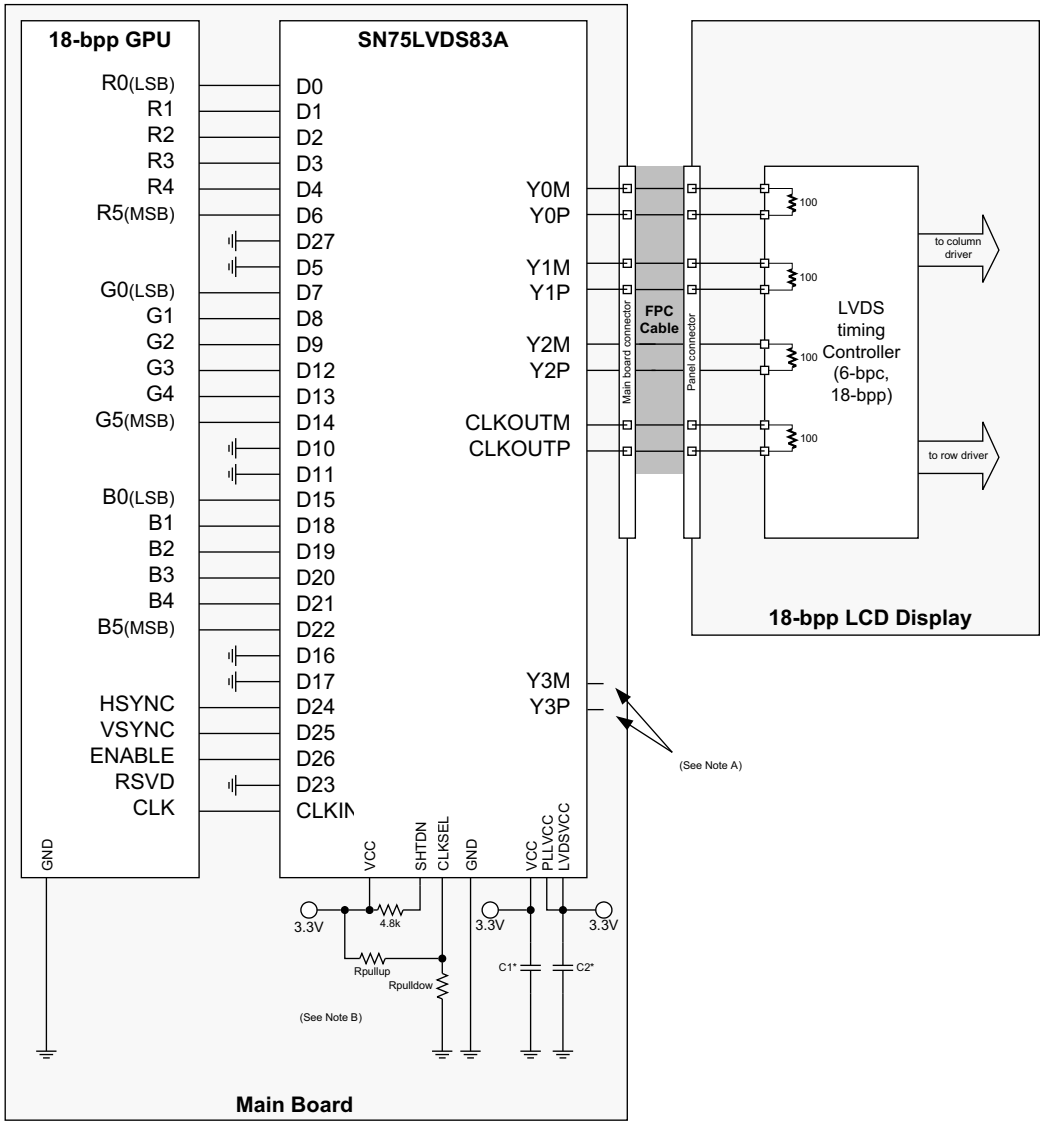
B. **Rpullup:** Install only to use rising edge triggered clocking. **Rpulldown:** Install only to use falling edge triggered clocking. **C1:** Decoupling capacitor for the VDDIO supply; install at least 1, 0.01-µF capacitor. **C2:** Decoupling capacitor for the VDD supply; install at least 1, 0.1-µF capacitor and 1, 0.01-µF capacitor. **C3:** Decoupling capacitor for the VDDPLL and VDDLVDS supply; install at least 1, 0.1-µF capacitor and 1, 0.01-µF capacitor.

C. If RSVD is not driven to a valid logic level, then an external connection to GND is recommended.

D. RSVD must be driven to a valid logic level. All unused SN75LVDS83A inputs must be tied to a valid logic level.

Figure 14. 24-Bit Color Host to 24-Bit LCD Panel Application

Application Information (continued)

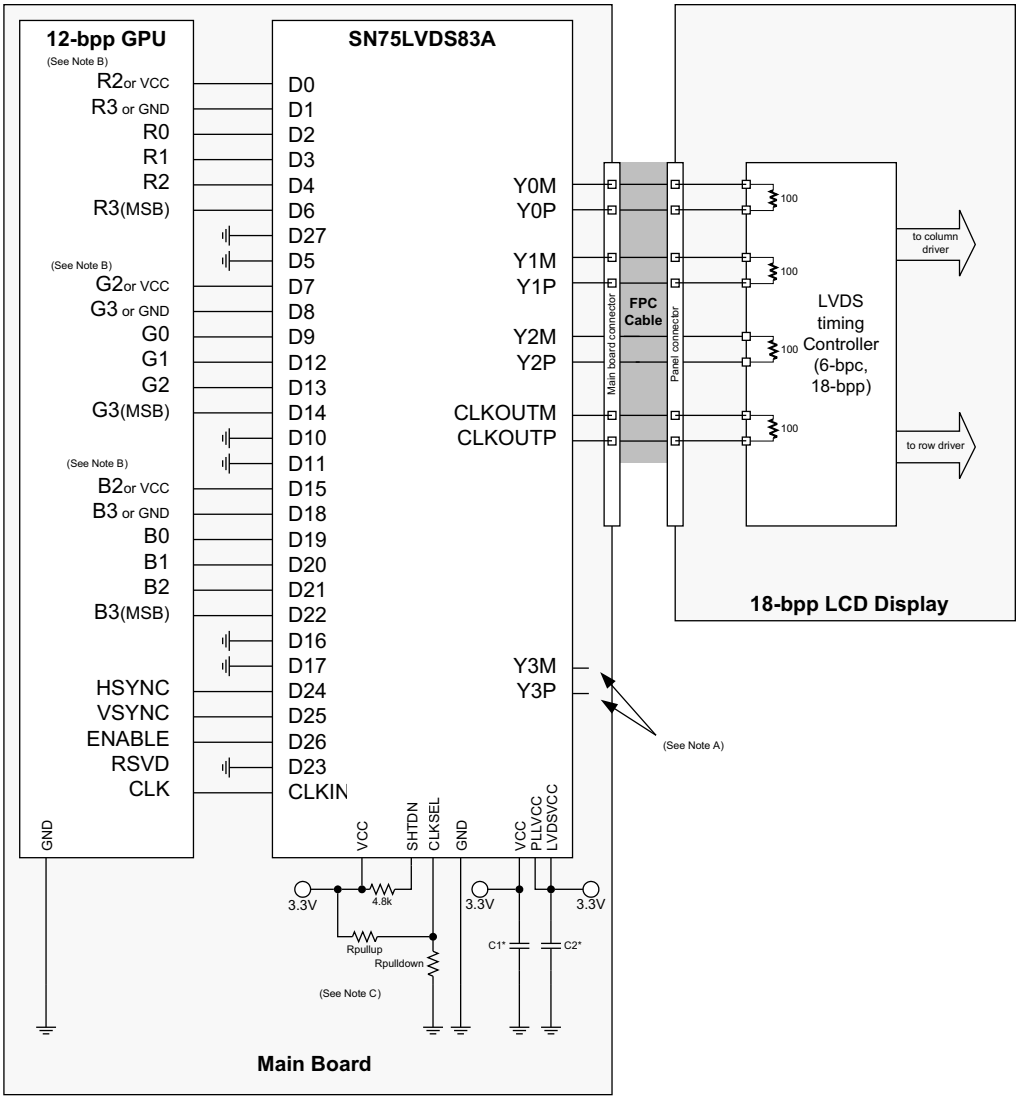


A. Leave output Y3 NC.

B. **Rpullup:** Install only to use rising edge triggered clocking. **Rpulldown:** Install only to use falling edge triggered clocking. **C1:** Decoupling capacitor for the VDDIO supply; install at least 1, 0.01-µF capacitor. **C2:** Decoupling capacitor for the VDD supply; install at least 1, 0.1-µF capacitor and 1, 0.01-µF capacitor. **C3:** Decoupling capacitor for the VDDPLL and VDDLVDS supply; install at least 1, 0.1-µF capacitor and 1, 0.01-µF capacitor.

Figure 15. 18-Bit Color Host to 18-Bit Color LCD Panel Display Application

Application Information (continued)



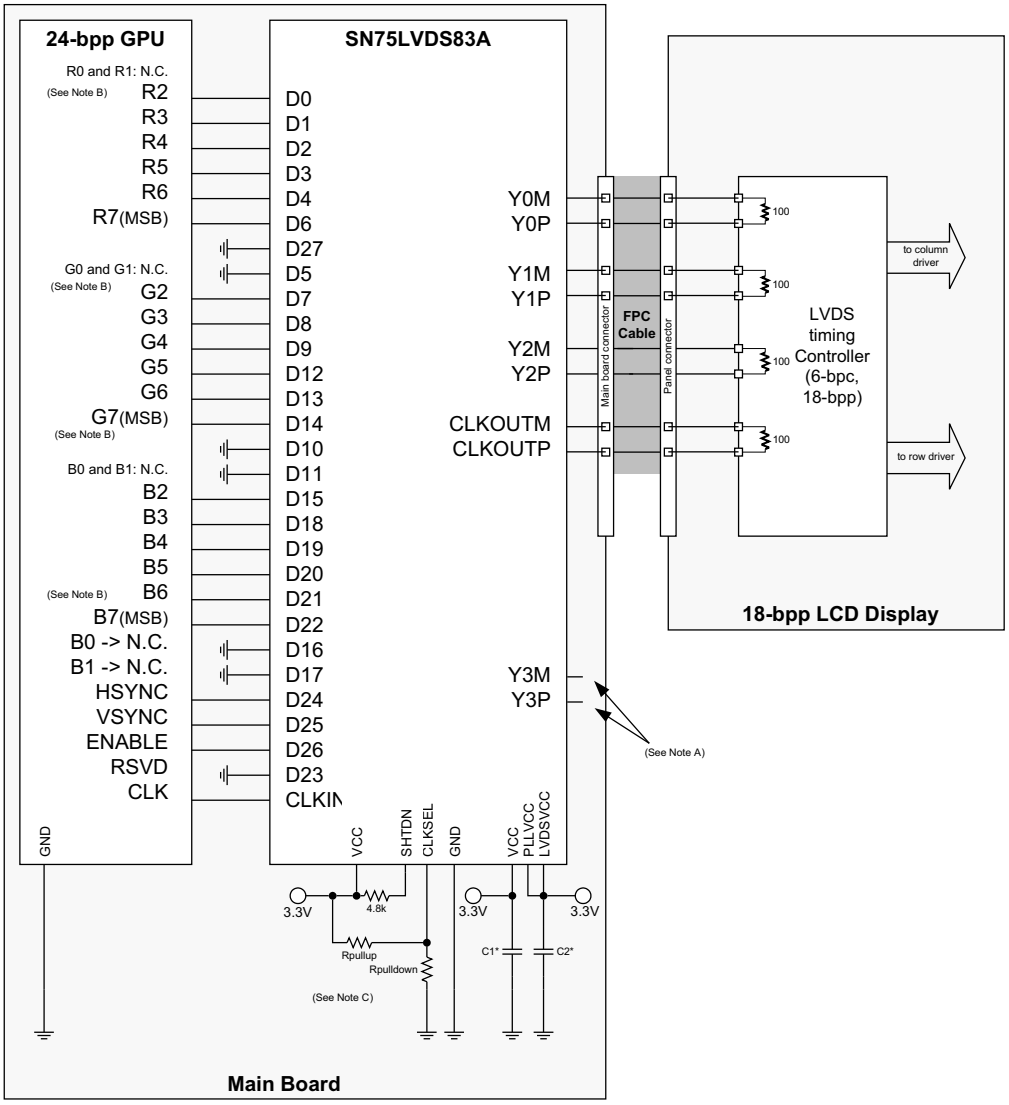
A. Leave output Y3 NC.

B. **R3, G3, B3:** This MSB of each color also connects to the 5th bit of each color for increased dynamic range of the entire color space at the expense of non-linear step sizes between each step. For linear steps with less dynamic range, connect D1, D8, and D18 to GND. **R2, G2, B2:** These outputs also connect to the LSB of each color for increased. Dynamic range of the entire color space at the expense of non-linear step sizes between each step. For linear steps with less dynamic range, connect D0, D7, and D15 to VCC.

C. **Rpullup:** Install only to use rising edge triggered clocking. **Rpulldown:** Install only to use falling edge triggered clocking. **C1:** Decoupling capacitor for the VDDIO supply; install at least 1, 0.01-µF capacitor. **C2:** Decoupling capacitor for the VDD supply; install at least 1, 0.1-µF capacitor and 1, 0.01-µF capacitor. **C3:** Decoupling capacitor for the VDDPLL and VDDLVDS supply; install at least 1, 0.1-µF capacitor and 1, 0.01-µF capacitor.

Figure 16. 12-Bit Color Host to 18-Bit Color LCD Panel Display Application

Application Information (continued)



A. Leave output Y3 NC.

B. R0, R1, G0, G1, B0, and B1: For improved image quality, the GPU must dither the 24-bit output pixel down to18-bit per pixel.

C. **Rpullup:** Install only to use rising edge triggered clocking. **Rpulldown:** Install only to use falling edge triggered clocking. **C1:** Decoupling capacitor for the VDDIO supply; install at least 1, 0.01-µF capacitor. **C2:** Decoupling capacitor for the VDD supply; install at least 1, 0.1-µF capacitor and 1, 0.01-µF capacitor. **C3:** Decoupling capacitor for the VDDPLL and VDDLVDS supply; install at least 1, 0.1-µF capacitor and 1, 0.01-µF capacitor.

Figure 17. 24-Bit Color Host to 18-Bit Color LCD Panel Display Application

Application Information (continued)

10.1.2 PCB Routing

Figure 18 and Figure 19 show a possible breakout of the data input and output signals from the BGA package.

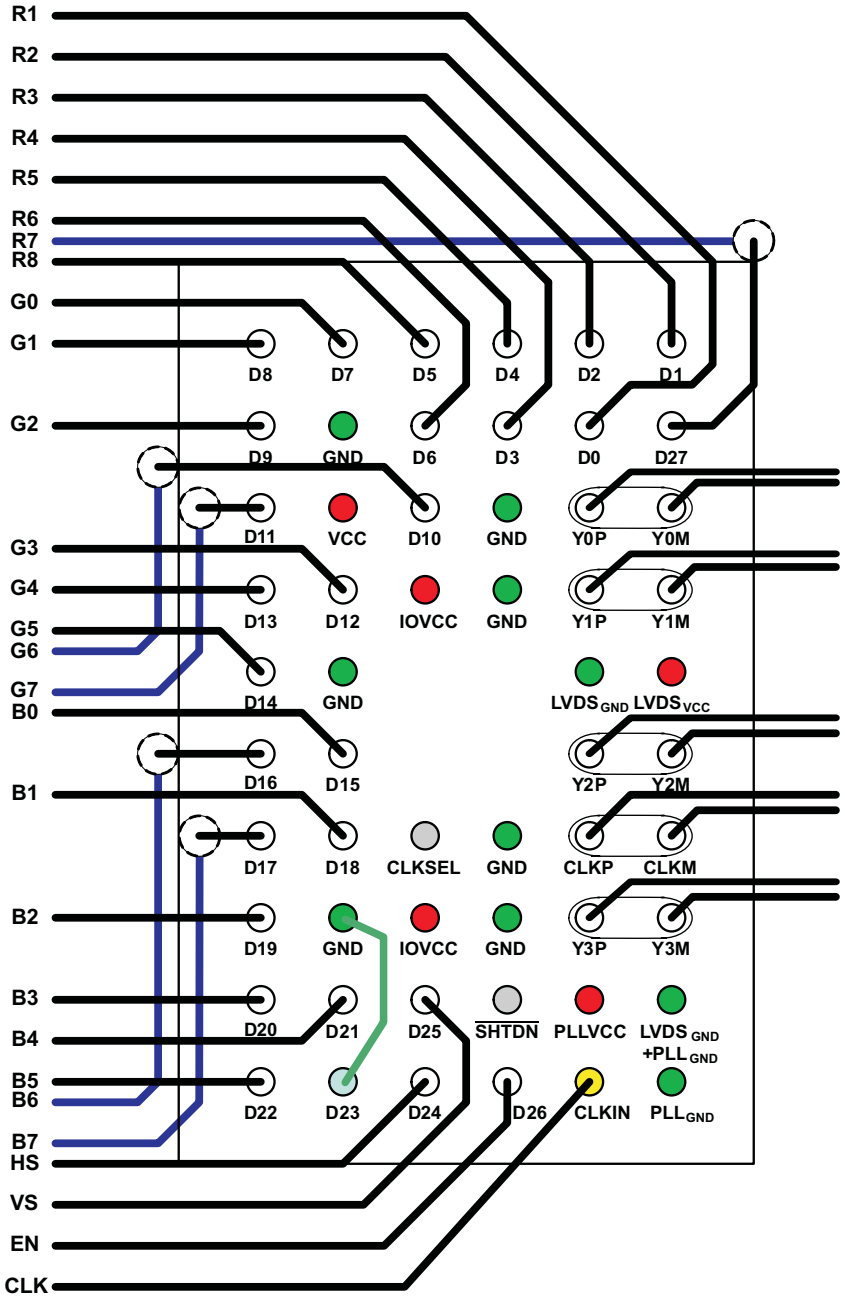


Figure 18. 24-Bit Color Routing (See Figure 14 for Schematic)

Application Information (continued)

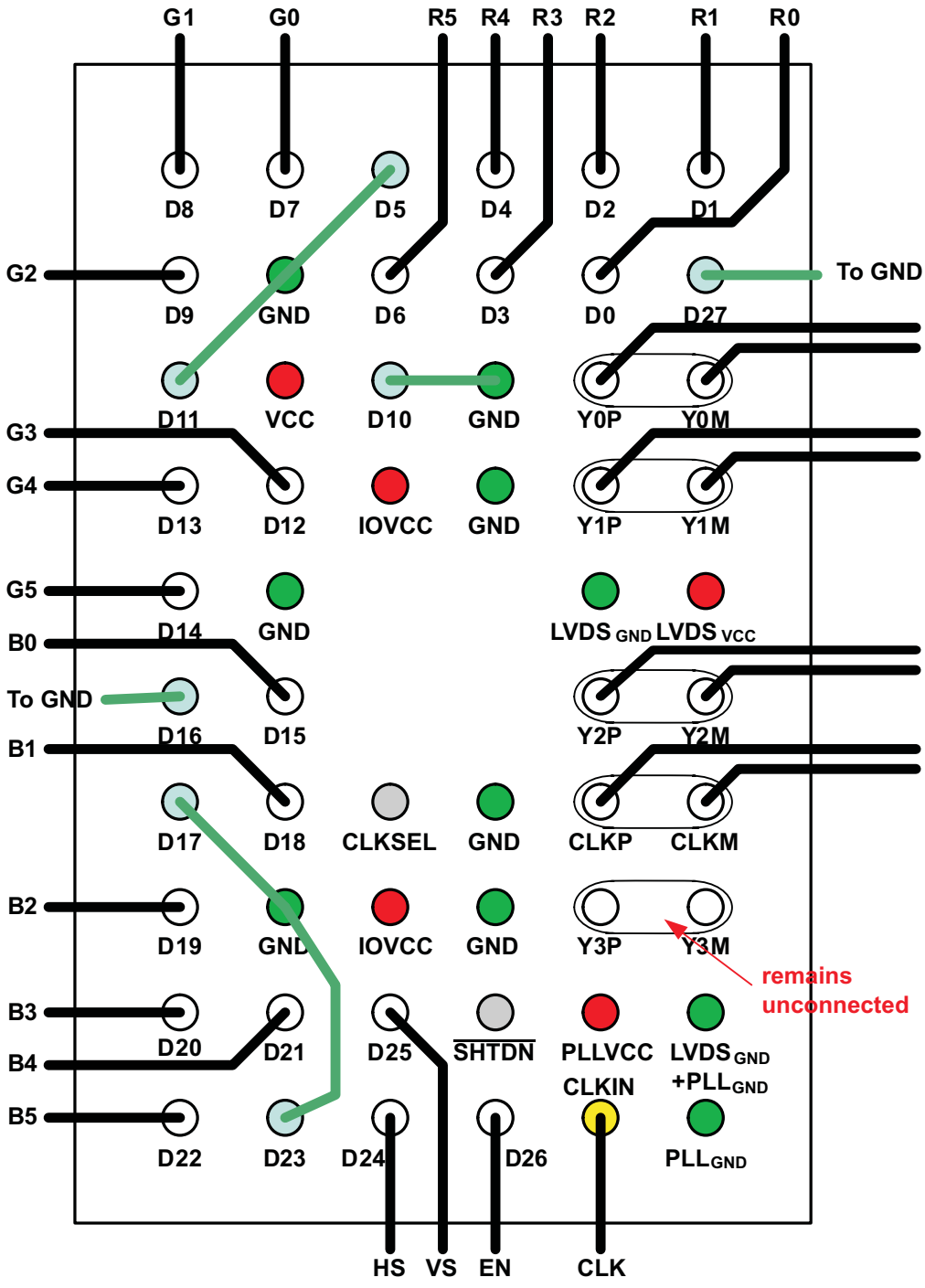


Figure 19. 18-Bit Color Routing (See Figure 15, Figure 16, and Figure 17 for Schematic)

10.2 Typical Application

Figure 20 represents the schematic drawing of the SN75LVDS83A evaluation module.

Typical Application (continued)

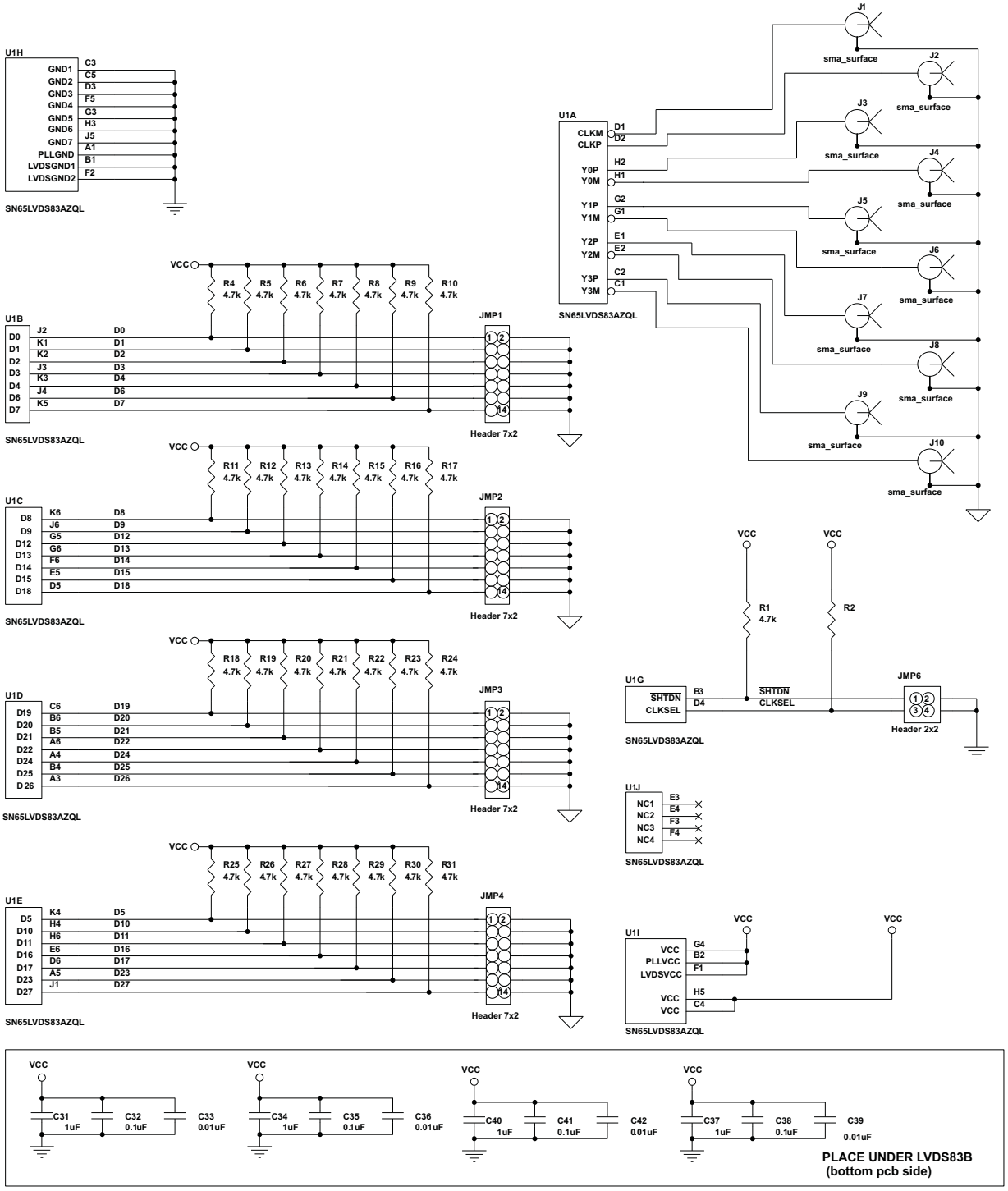


Figure 20. Schematic Example (SN75LVDS83A Evaluation Board)

Typical Application (continued)

10.2.1 Design Requirements

Table 3 lists the parameters for this schematic example.

Table 3. Design Parameters

PARAMETER	VALUE
VCC	3.3 V
CLKIN	Falling edge
SHTDN	High
Format	18-bit GPU to 24-bit LCD

10.2.2 Detailed Design Procedure

10.2.2.1 Power Up Sequence

The SN75LVDS83A does not require a specific power up sequence. It is permitted to power up IOVCC while VCC, VCCPLL, and VCCLVDS remain powered down and connected to GND. The input level of the SHTDN during this time does not matter as only the input stage is powered up while all other device blocks are still powered down.

It is also permitted to power up all 3.3-V power domains while IOVCC is still powered down to GND. The device does now suffer damage. However, in this case, all the I/Os are detected as logic HIGH, regardless of their true input voltage level. Therefore, connecting SHTDN to GND is still interpreted as a logic HIGH, and the LVDS output stage are turned on. The power consumption in this condition is significantly higher than standby mode, but still lower than normal mode.

The user experience is impacted by the way a system powers up and powers down an LCD screen. The following sequence is recommended:

Power up sequence (SN75LVDS83A SHTDN input initially low):

1. Ramp-up LCD power (0.5 ms to 10 ms for example) but keep backlight turned off
2. Wait an additional 0 to 200 ms to ensure display noise won't occur
3. Enable video source output and start sending black video data
4. Toggle LVDS83A shutdown to SHTDN = VIH
5. Send >1 ms of black video data (this allows the LVDS83A to be phase locked and the display to show black data first)
6. Start sending true image data
7. Enable backlight

Power down sequence (SN75LVDS83A SHTDN input initially high):

1. Disable LCD backlight and wait for the minimum time specified in the LCD data sheet for the backlight to go low
2. Video source output data switch from active video data to black image data (all visible pixel turn black); drive this for >2 frame times
3. Set SN75LVDS83A input SHTDN = GND and wait for 250 ns
4. Disable the video output of the video source
5. Remove power from the LCD panel for lowest system power

10.2.3 Application Curve

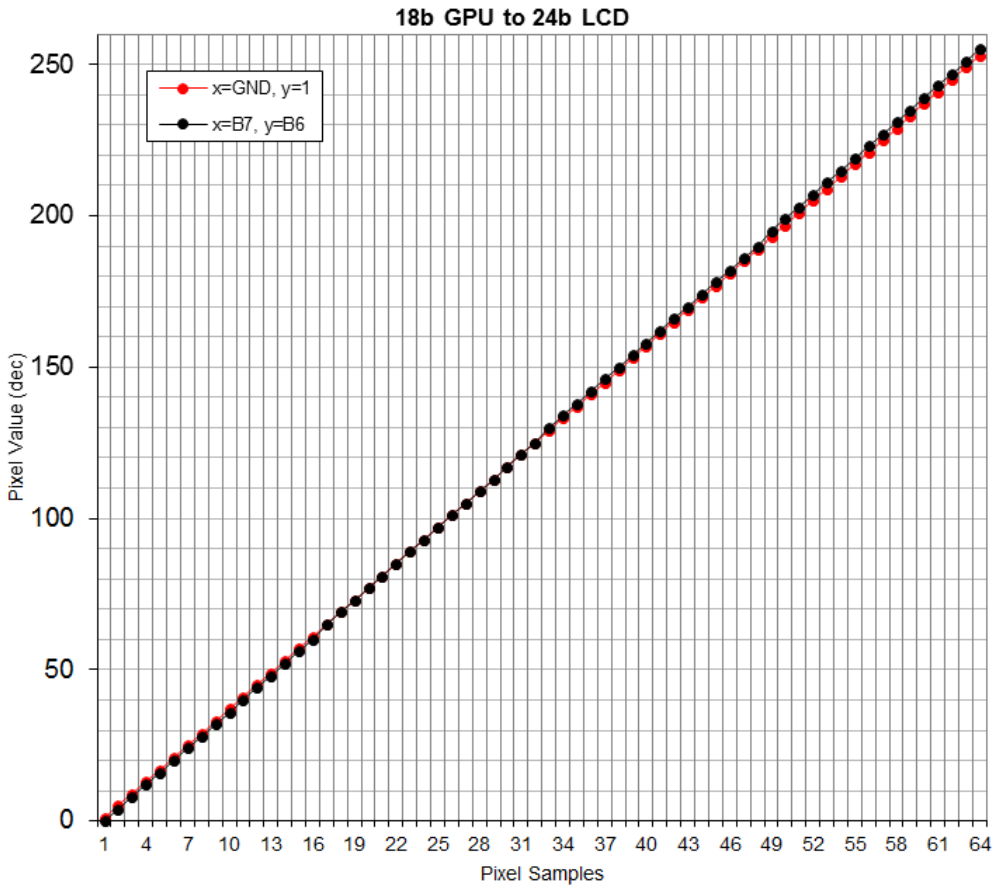


Figure 21. 18b GPU to 24b LCD

11 Power Supply Recommendations

Power supply PLL, IO, and LVDS terminals must be uncoupled from each.

12 Layout

12.1 Layout Guidelines

12.1.1 Board Stackup

There is no fundamental information about how many layers should be used and how the board stackup should look. Again, the easiest way the get good results is to use the design from the EVMs of Texas Instruments. The magazine Elektronik Praxis [11] has published an article with an analysis of different board stackups. These are listed in Table 4.

Table 4. Board Stackup on a Four-Layer PCB

	MODEL 1	MODEL 2	MODEL 3	MODEL 4
Layer 1	SIG	SIG	SIG	GND
Layer 2	SIG	GND	GND	SIG
Layer 3	VCC	VCC	SIG	VCC
Layer 4	GND	SIG	VCC	SIG
Decoupling	Good	Good	Bad	Bad
EMC	Bad	Bad	Bad	Bad
Signal integrity	Bad	Bad	Good	Bad
Self disturbance	Satisfaction	Satisfaction	Satisfaction	High

Generally, the use of microstrip traces needs at least two layers, whereas one of them must be a GND plane. Better is the use of a four-layer PCB, with a GND and a VCC plane and two signal layers. If the circuit is complex and signals must be routed as stripline, because of propagation delay and/or characteristic impedance, a six-layer stackup should be used.

12.1.2 Power and Ground Planes

A complete ground plane in high-speed design is essential. Additionally, a complete power plane is recommended as well. In a complex system, several regulated voltages can be present. The best solution is for every voltage to have its own layer and its own ground plane. This would result in a huge number of layers just for ground and supply voltages.

In a mixed-signal design (for example, using data converters) the manufacturer often recommends splitting the analog ground and the digital ground to avoid noise coupling between the digital part and the sensitive analog part. Take care when using split ground planes, because the following occurs:

- Split ground planes act as slot antennas and radiate
- A routed trace over a gap creates large loop areas, because the return current cannot flow beside the signal. The signal can induce noise into the nonrelated reference plane (see Figure 22).
- With a proper signal routing, crosstalk also can arise in the return current path due to discontinuities in the ground plane. Always take care of the return current (see Figure 23).

Do not route a signal referenced to digital ground over analog ground and vice versa (see Figure 22). The return current cannot take the direct way along the signal trace and so a loop area occurs. Furthermore, the signal induces noise, due to crosstalk (dotted red line) into the analog ground plane.

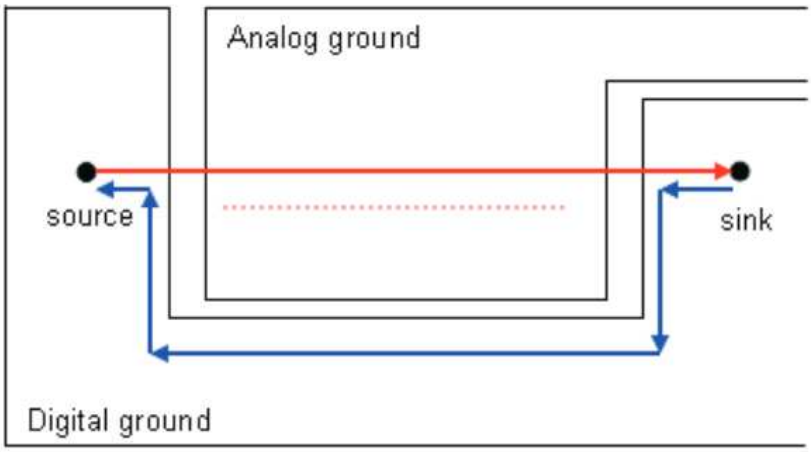


Figure 22. Loop Area and Crosstalk Due to Poor Signal Routing and Ground Splitting

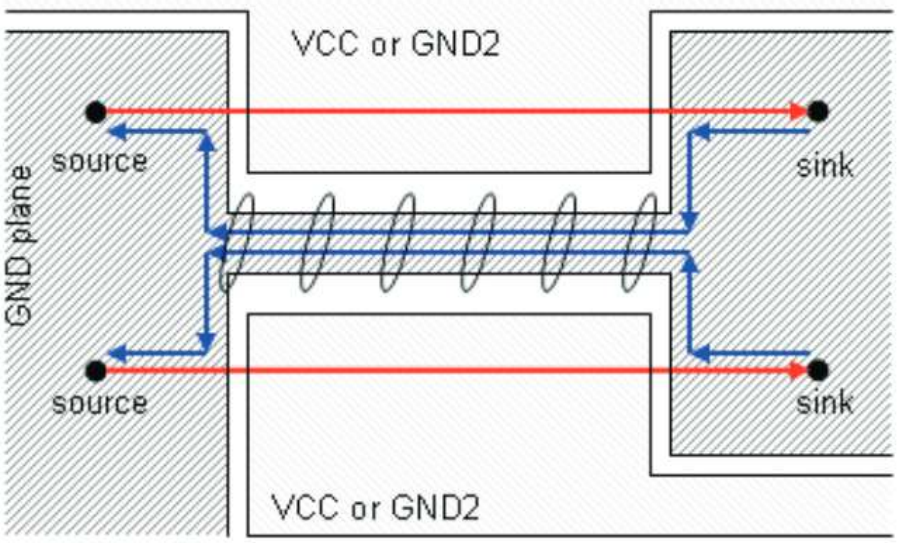


Figure 23. Crosstalk Induced by the Return Current Path

12.1.3 Traces, Vias, and Other PCB Components

A right angle in a trace can cause more radiation. The capacitance increases in the region of the corner, and the characteristic impedance changes. This impedance change causes reflections.

Avoid right-angle bends in a trace and try to route them at least with two 45° corners. To minimize any impedance change, the best routing would be a round bend (see Figure 24).

Separate high-speed signals (for example, clock signals) from low-speed signals and digital from analog signals; again, placement is important.

To minimize crosstalk not only between two signals on one layer but also between adjacent layers, route them with 90° to each other.

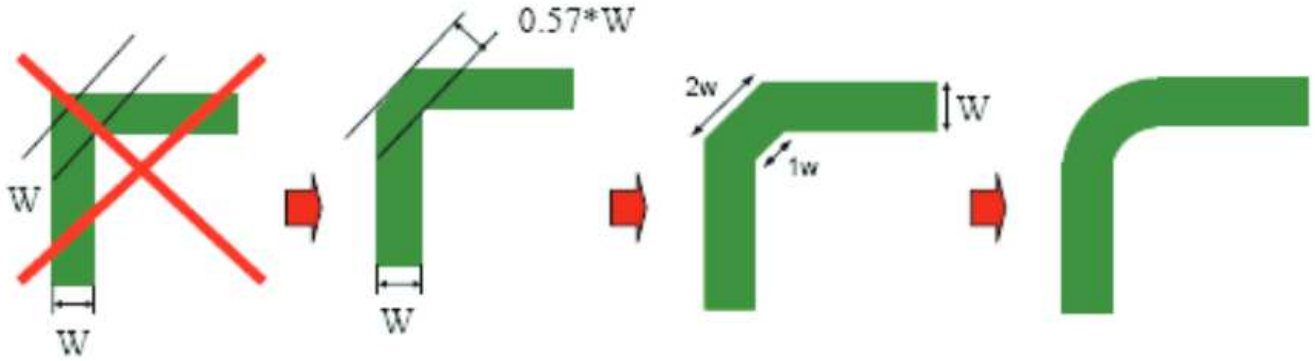


Figure 24. Right Angle Bend Examples

12.2 Layout Example

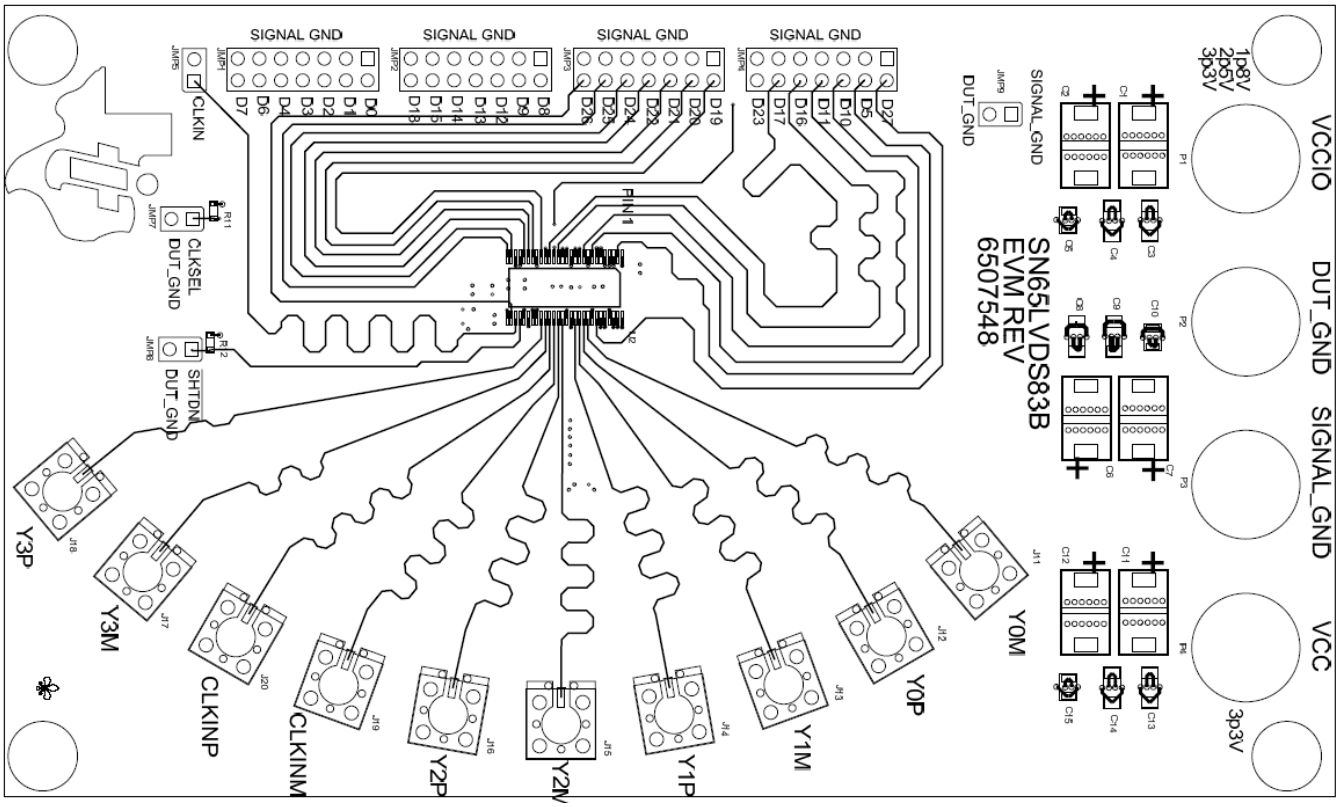


Figure 25. SN75LVDS83B EVM Top Layer – TSSOP Package

Layout Example (continued)

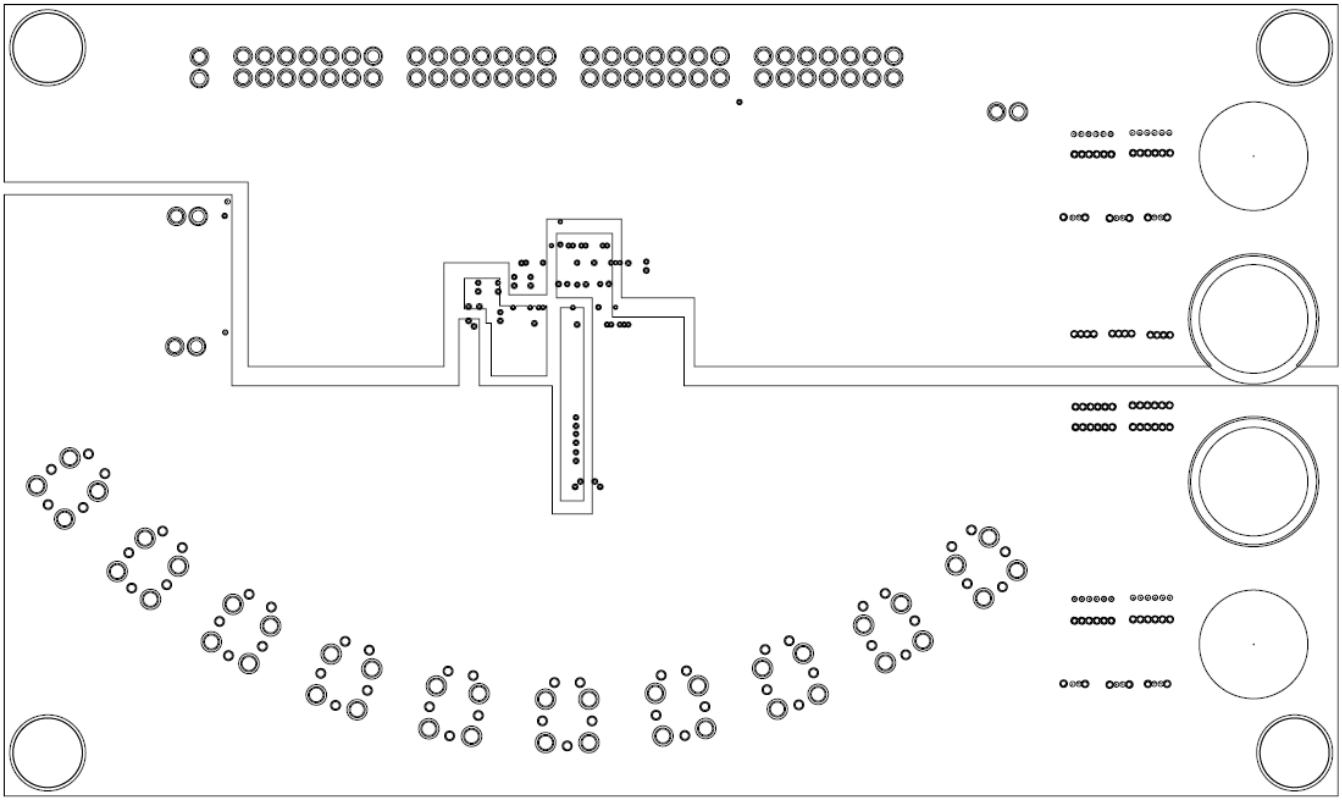


Figure 26. SN75LVDS83B EVM VCC Layer – TSSOP Package

13 Device and Documentation Support

13.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

OMAP, DaVinci, Flatlink, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75LVDS83ADGG	ACTIVE	TSSOP	DGG	56	35	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-10 to 70	LVDS83A	Samples
SN75LVDS83ADGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-10 to 70	LVDS83A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

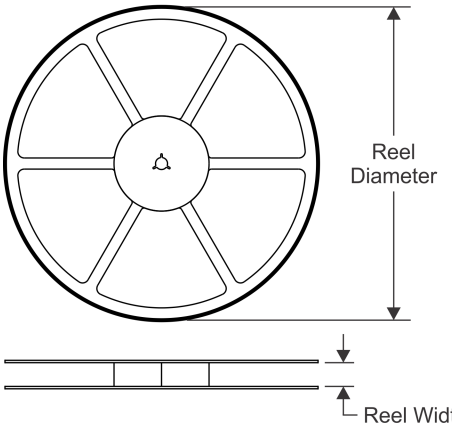
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

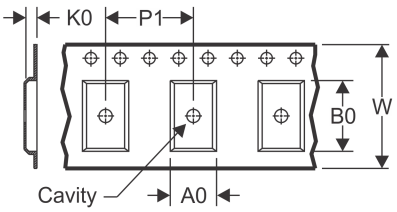
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

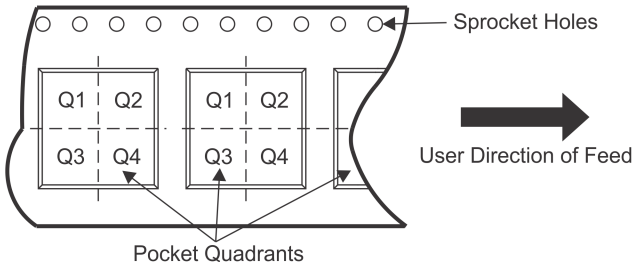


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

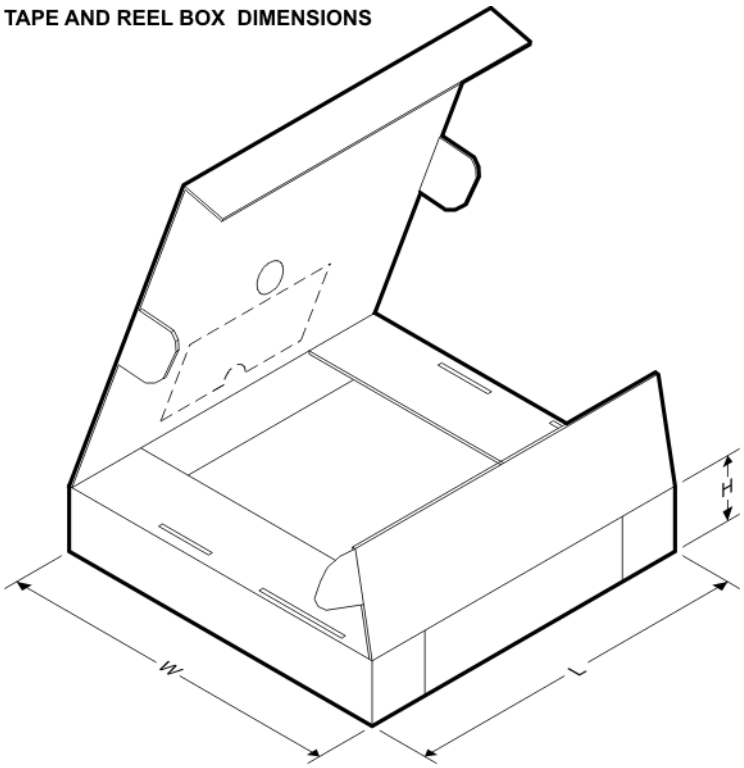
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LVDS83ADGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

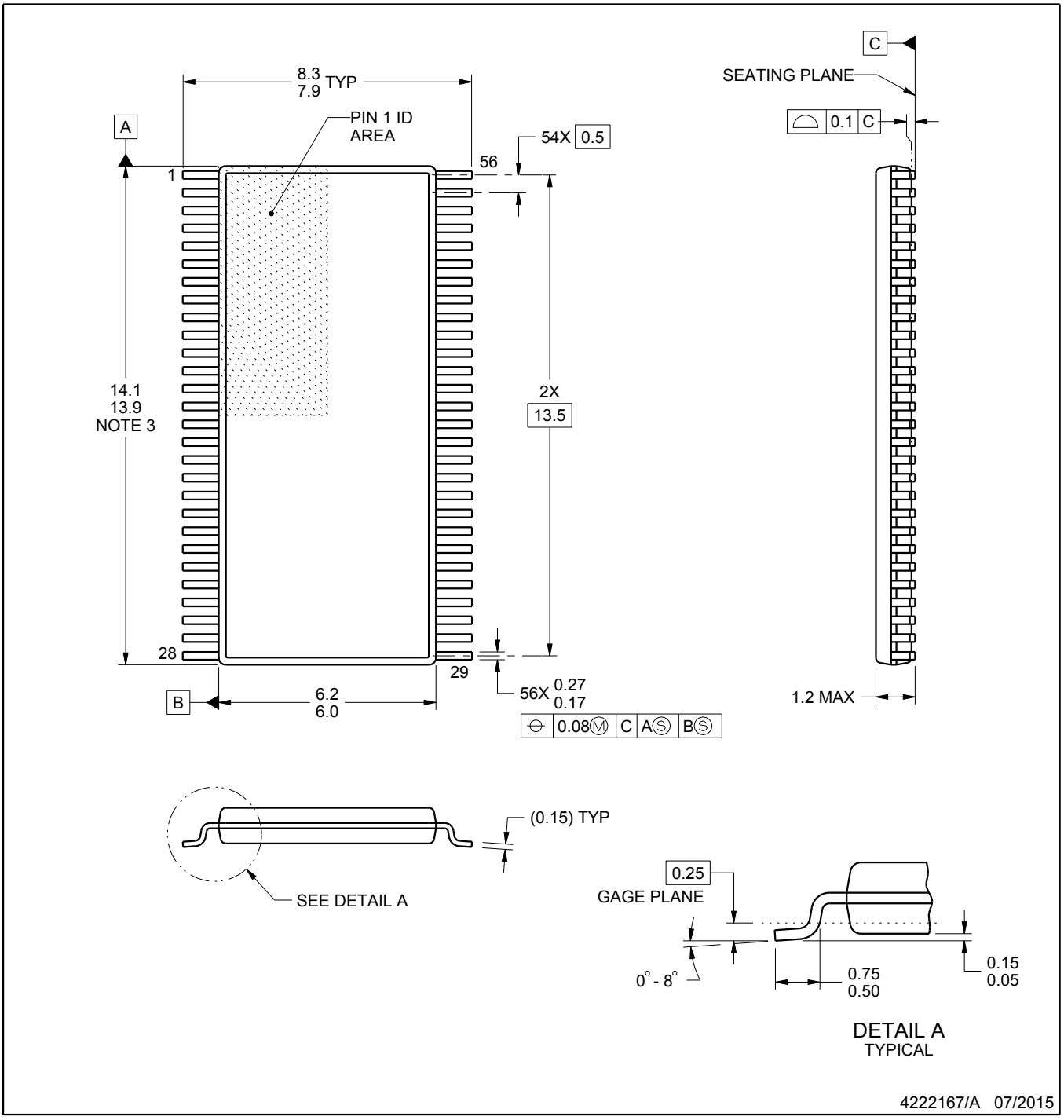
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LVDS83ADGGR	TSSOP	DGG	56	2000	367.0	367.0	45.0

PACKAGE OUTLINE

DGG0056A

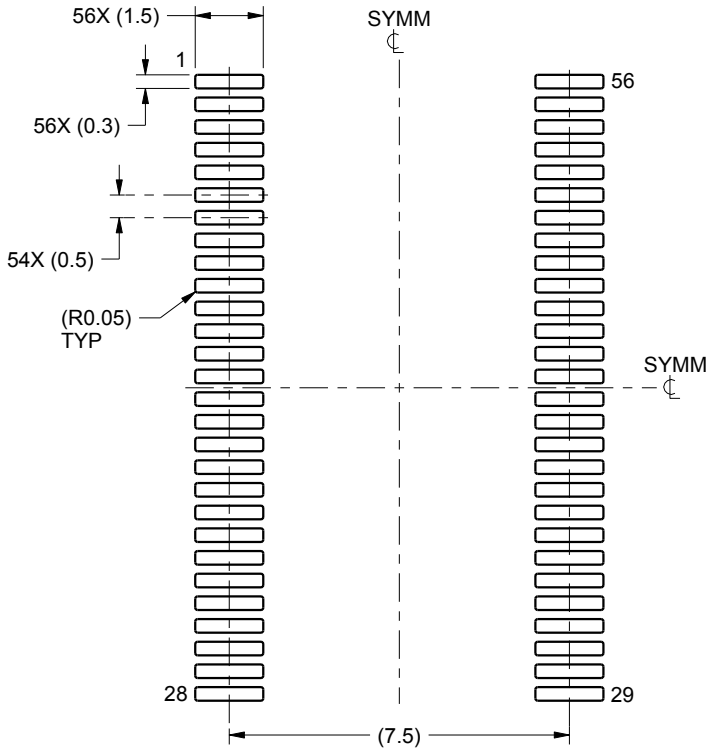
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

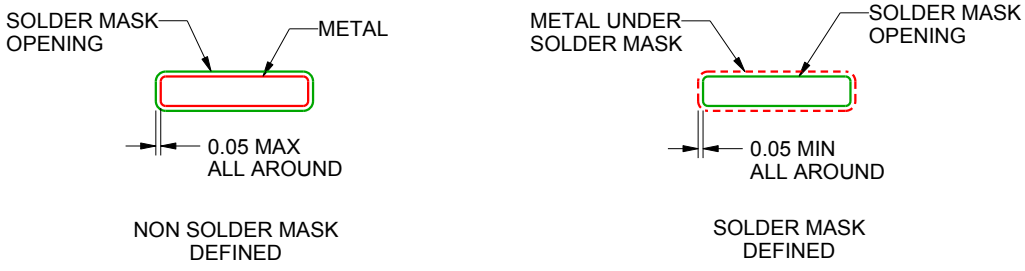


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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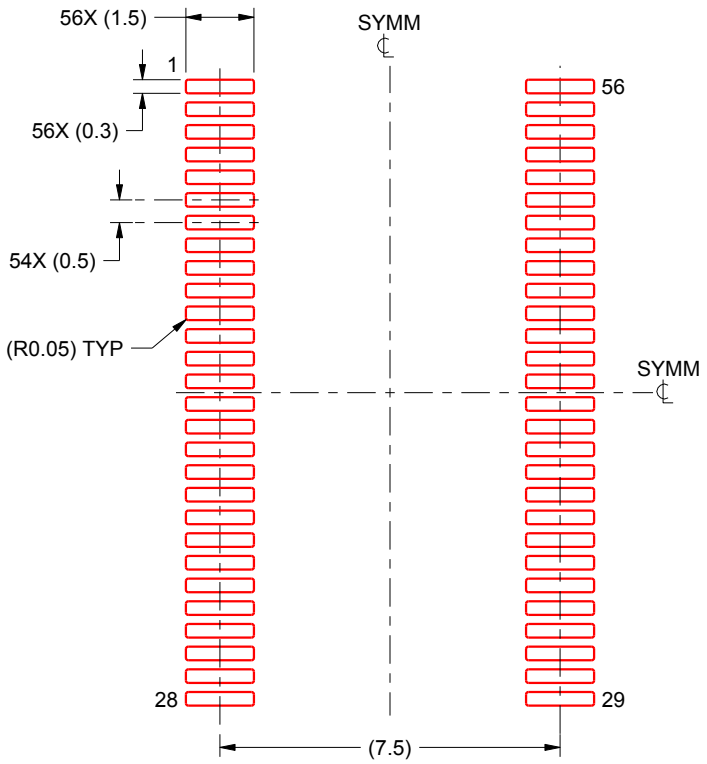
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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