TPS25810 USB Type-C DFP Controller and Power Switch with Load Detection

1 Features

- USB Type-C Rev. 1.1 Compliant DFP Controller
- Connector Attach/Detach Detection
- STD/1.5-A/3-A Capability Advertisement on CC
- Super Speed Polarity Determination
- V_{BUS} Application and Discharge
- V_{CONN} Application to Electronically Marked Cable
- Audio and Debug Accessory Identification
- 0.7-µA (typ) I_{DDQ} When Port Unattached
- Three Input Supply Options
  - IN1: USB Charging Supply
  - IN2: V_{CONN} Supply
  - AUX: Device Power Supply
- Power Wake Supports Low Power in System Hibernate (S4) and OFF (S5) Power States
- 34-mΩ (typ) High-Side MOSFET
- 1.7/3.4-A I_{Limit} (±7.1%) - Programmable
- Port Power Management Enables Power Resource Optimization Across Multi-Ports
- Package: 20-Pin WQFN (3 x 4) (1)
- UL Listed – File No. E169910

2 Applications

- USB Type C Host Port in Notebook for Sleep Charging
- LCD Monitor/Docking Station and Charging Cradles
- Type C USB Wall Chargers

(1) CC pins are IEC-61000-4-2 rated

3 Description

The TPS25810 is a USB Type-C Downstream Facing Port (DFP) controller with an integrated 3-A rated USB power switch. The TPS25810 monitors the Type-C Configuration Channel (CC) lines to determine when an USB device is attached. If an Upstream Facing Port (UFP) device is attached, the TPS25810 applies power to V_{BUS} and communicates the selectable V_{BUS} current sourcing capability to the UFP via the passthrough CC line. If the UFP is attached using an electronically marked cable, the TPS25810 also applies V_{CONN} power to the cable CC pin. The TPS25810 also identifies when Type-C audio or debug accessories are attached.

The TPS25810 draws less than 0.7 uA (typ) when no device is attached. Additional system power saving is achievable in S4/S5 system power states by using the $\overline{UFP}$ output to disable the high power 5-V supply when no UFP is attached. In this mode the device is capable of running from an auxiliary supply (AUX) which can be a lower voltage supply (3.3 V), typically powering the system uC in low power states (S4/S5).

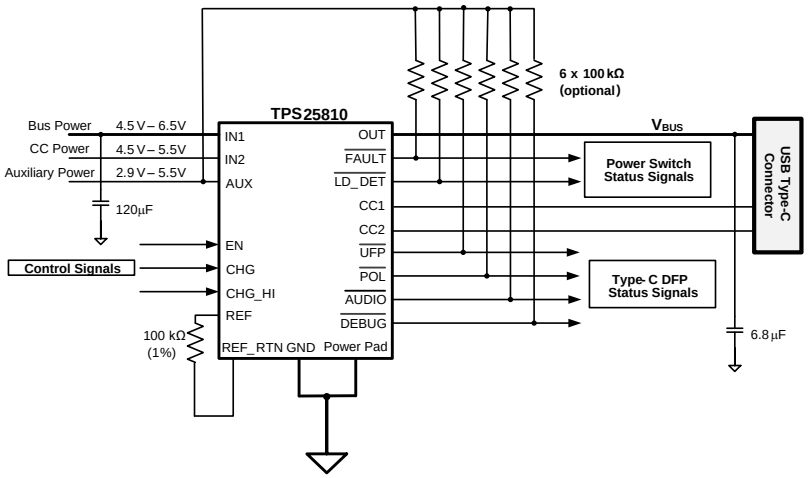
The TPS25810 34-mΩ power switch has two selectable fixed current limits that align with the Type-C current levels. The $\overline{FAULT}$ output signals when the switch is in an over current or over temperature condition. The $\overline{LD\_DET}$ output controls power management to multiple high current Type-C ports in an environment where all ports cannot simultaneously provide high current (3 A).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS25810	WQFN (20)	3.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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- Changed 10µF to 6.8µF in Simplified Schematic ... 1
- Added text to REF description ... 3
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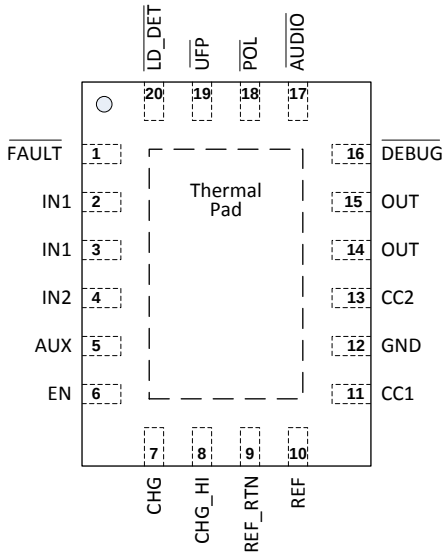
- Changed from Product Preview to Production Data ... 1

5 Pin Configuration and Functions

RVC Package
20-Pin WQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
$\overline{\text{FAULT}}$	1	O	Fault event indicator. Open-drain logic output that asserts low to indicate current limit or thermal shutdown event due to over temperature.
IN1	2, 3	I	V_{BUS} input supply. Internal power switch connects IN1 to OUT.
IN2	4	I	V_{CONN} input supply. Internal power switch connects IN2 to CC1 or CC2. Short to IN1 if only one supply is used.
AUX	5	I	Auxiliary input supply. Connect to always alive system rail to use the Power Wake feature. Short to IN1 and IN2 if only one supply is used.
EN	6	I	Enable logic input to turn the device on and off.
CHG	7	I	Charge logic input to select between standard USB (500 mA for a Type C receptacle supporting only USB 2.0 and 900 mA for Type C receptacle supporting USB 3.1) or Type-C current sourcing ability.
CHG_HI	8	I	High-charge logic input to select between 1.5-A and 3-A Type-C current sourcing capability. Valid when CHG is set to Type-C current.
REF_RTN	9	I	Precision signal reference return. Connect to REF pin via 100-kΩ, 1% resistor.
REF	10	I	Analog input used to generate internal current reference. Connect a 1% or better, 100 ppm, 100-kΩ resistor between this pin and REF_RTN.
CC1	11	I/O	Analog input/output that connects to the Type-C receptacle CC1 pin
GND	12	–	Power ground
CC2	13	I/O	Analog input/output that connects to the Type-C receptacle CC2 pin.
OUT	14,15	O	Power switch output.
$\overline{\text{DEBUG}}$	16	O	Open-drain logic output that asserts when a Type-C Debug accessory is identified on the CC lines.
$\overline{\text{AUDIO}}$	17	O	Open-drain logic output that asserts when a Type-C Audio accessory is identified on the CC lines.
$\overline{\text{POL}}$	18	O	Polarity open-drain logic output that signals which Type-C CC pin is connected to the CC line. This gives the information needed to mux the super speed lines. Asserted when the CC2 pin is connected to the CC line in cable.
$\overline{\text{UFP}}$	19	O	Open-drain logic output that asserts when a Type-C UFP is identified on the CC lines.
$\overline{\text{LD\_DET}}$	20	O	Load-detect open-drain logic output that signals when a device set to source Type-C 3 A current is sourcing over 1.95 A nominal.
Thermal Pad	–	–	Thermal pad on bottom of package.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range, voltages are respect to GND (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage, V	IN1, IN2, AUX, EN, CHG, CHG_HI, REF, OUT, $\overline{\text{LD\_DET}}$, $\overline{\text{FAULT}}$, CC1, CC2, $\overline{\text{UFP}}$, $\overline{\text{POL}}$, $\overline{\text{AUDIO}}$, $\overline{\text{DEBUG}}$	–0.3	7	V
	REF_RTN		Internally connected to GND	V
Pin positive source current, I_{SRC}	OUT, REF, CC1, CC2		Internally limited	A
Pin positive sink current, I_{SNK}	OUT (while applying VBUS)		5	A
	CC1, CC2 (while applying V_{CONN})		1	A
	$\overline{\text{LD\_DET}}$, $\overline{\text{FAULT}}$, $\overline{\text{UFP}}$, $\overline{\text{POL}}$, $\overline{\text{AUDIO}}$, $\overline{\text{DEBUG}}$		Internally limited	mA
Operating junction temperature, T_J		–40	180	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ (1)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (2)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (3)	±500	
		IEC (4) IEC61000-4-2 contact discharge, CC1 and CC2	±8000	
		IEC (4) IEC61000-4-2 air discharge, CC1 and CC2	±15000	

(1) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by assembly line electrostatic discharges into the device.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(4) Surges per IEC61000-402, 1999 applied between CC1/CC2 and output ground of the TPS25810EVM-745.

6.3 Recommended Operating Conditions

Voltages are with respect to GND (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_I	Supply voltage	IN1	4.5		6.5	V
		IN2	4.5		5.5	
		AUX	2.9		5.5	
V_I	Input voltage	EN, CHG, CHG_HI	0		5.5	V
V_{IH}	High-level input voltage	EN, CHG, CHG_HI	1.17			V
V_{IL}	Low-level voltage	EN, CHG, CHG_HI			0.63	V
V_{PU}	Pull-up voltage	Used on $\overline{\text{LD\_DET}}$, $\overline{\text{FAULT}}$, $\overline{\text{UFP}}$, $\overline{\text{POL}}$, $\overline{\text{AUDIO}}$, $\overline{\text{DEBUG}}$	0		5.5	V
I_{SRC}	Positive source current	OUT			3	A
		CC1 or CC2 when supplying VCONN			250	mA
I_{SNK}	Positive sink current (10 ms moving average)	$\overline{\text{LD\_DET}}$, $\overline{\text{FAULT}}$, $\overline{\text{UFP}}$, $\overline{\text{POL}}$, $\overline{\text{AUDIO}}$, $\overline{\text{DEBUG}}$			10	mA
I_{SNK_PULSE}	Positive repetitive pulse sink current	$\overline{\text{LD\_DET}}$, $\overline{\text{FAULT}}$, $\overline{\text{UFP}}$, $\overline{\text{POL}}$, $\overline{\text{AUDIO}}$, $\overline{\text{DEBUG}}$			Internally Limited	mA
R_{REF}	Reference Resistor		98	100	102	kΩ
T_J	Operating junction temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS25810 RVC (WQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

–40°C ≤ T_J ≤ 125°C, 4.5 V ≤ V_{IN1} ≤ 6.5 V, 4.5 V ≤ V_{IN2} ≤ 5.5 V, 2.9 V ≤ V_{AUX} ≤ 5.5 V; V_{EN} = V_{CHG} = V_{CHG_HI} = V_{AUX}, R_{REF} = 100 kΩ. Typical values are at 25°C. All voltages are with respect to GND. I_{OUT} and I_{OS} defined positive out of the indicated pin (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUT - POWER SWITCH						
$R_{DS(on)}$	On resistance[1]	T_J = 25°C, I_{OUT} = 3 A		34	37	mΩ
		–40°C ≤ T_J ≤ 85°C, I_{OUT} = 3 A		34	46	
		–40°C ≤ T_J ≤ 125°C, I_{OUT} = 3 A		34	55	
I_{REV}	OUT to IN reverse leakage current	V_{OUT} = 6.5 V, V_{IN1} = V_{EN} = 0 V, –40°C ≤ T_J ≤ 85°C, I_{REV} is current out of IN1 pin		0	3	µA
OUT - CURRENT LIMIT						
I_{OS}	Short circuit current limit [1]	V_{CHG} = 0 V or V_{CHG} = V_{AUX} and V_{CHG_HI} = 0 V	1.58	1.7	1.82	A
		V_{CHG} = V_{AUX} and V_{CHG_HI} = V_{AUX}	3.16	3.4	3.64	
		R_{REF} = 10 Ω			7	
OUT - DISCHARGE						
	Discharge resistance	V_{OUT} = 4 V, UFP signature removed from CC lines, time < t_{w_DCHG}	400	500	600	Ω
	Bleed discharge resistance	V_{OUT} = 4 V, No UFP signature on CC lines, time > t_{w_DCHG}	100	150	250	kΩ
REF						
V_O	Output voltage		0.78	0.8	0.82	V
I_{OS}	Short circuit current	R_{REF} = 10 Ω	9.5		15.3	µA
$\overline{\text{FAULT}}$						
V_{OL}	Output low voltage	$I_{\overline{FAULT}}$ = 1 mA			350	mV
I_{OFF}	Off-state leakage	$V_{\overline{FAULT}}$ = 5.5 V			1	µA
$\overline{\text{LD\_DET}}$						
V_{OL}	Output low voltage	$I_{\overline{LD\_DET}}$ = 1 mA			350	mV
I_{OFF}	Off-state leakage	$V_{\overline{LD\_DET}}$ = 5.5 V			1	µA
I_{TH}	OUT sourcing, rising threshold current for load detect		1.8	1.95	2.1	A
	Hysteresis[2]			125		mA

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
(2) These parameters are provided for reference only and do not constitute part of TI's published specifications for purposes of TI's product warranty.

Electrical Characteristics (continued)

–40°C ≤ T_J ≤ 125°C, 4.5 V ≤ V_{IN1} ≤ 6.5 V, 4.5 V ≤ V_{IN2} ≤ 5.5 V, 2.9 V ≤ V_{AUX} ≤ 5.5 V; V_{EN} = V_{CHG} = V_{CHG_HI} = V_{AUX}, R_{REF} = 100 kΩ. Typical values are at 25°C. All voltages are with respect to GND. I_{OUT} and I_{OS} defined positive out of the indicated pin (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CC1/CC2 - V_{CONN} POWER SWITCH						
$R_{DS(on)}$	On resistance	T_J = 25°C, I_{OUT} = 250 mA		365	420	mΩ
		-40°C ≤ T_J ≤ 85°C, I_{OUT} = 250 mA		365	530	
		-40°C ≤ T_J ≤ 125°C, I_{OUT} = 250 mA		365	600	
CC1/CC2 - V_{CONN} POWER SWITCH - CURRENT LIMIT						
I_{OS}	Short circuit current limit (1)		300	355	410	mA
		R_{REF} = 10 Ω			800	
CC1/CC2 – CONNECT MANAGEMENT – DANGLING ELECTRONICALLY MARKED CABLE MODE						
I_{SRC}	Sourcing current on the pass-through CC Line	0 V ≤ V_{CCx} ≤ 1.5 V	64	80	96	µA
	Sourcing current on the Ra CC line	0 V ≤ V_{CCx} ≤ 1.5 V	64	80	96	µA
CC1/CC2 – CONNECT MANAGEMENT – ACCESSORY MODE						
I_{SRC}	CCx Sourcing current (CC2- Audio, CC1-Debug)	0 V ≤ V_{CCx} ≤ 1.5 V	64	80	96	µA
	CCx Sourcing current (CC1- Audio, CC2-Debug) (2)	0 V ≤ V_{CCx} ≤ 1.5 V		0		µA
CC1/CC2 – CONNECT MANAGEMENT – UFP MODE						
I_{SRC}	Sourcing current with either IN1 or IN2 in UVLO	0 V ≤ V_{CCx} ≤ 1.5 V V_{IN1} < $V_{TH\_UVLO\_IN1}$ or V_{IN2} < $V_{TH\_UVLO\_IN2}$	64	80	96	µA
I_{SRC}	Sourcing current	V_{CHG} = 0 V and V_{CHG_HI} = 0 V 0 V ≤ V_{CCx} ≤ 1.5 V	75	80	85	µA
		V_{CHG} = V_{AUX} and V_{CHG_HI} = 0 V 0 V ≤ V_{CCx} ≤ 1.5 V	170	180	190	
		V_{CHG} = V_{AUX} and V_{CHG_HI} = V_{AUX} 0 V ≤ V_{CCx} ≤ 2.45 V	312	330	348	
$\overline{UFP}$, $\overline{POL}$, $\overline{AUDIO}$, $\overline{DEBUG}$						
V_{OL}	Output low voltage	I_{SNK_PIN} = 1 mA			250	mV
I_{OFF}	Off-state leakage	V_{PIN} = 5.5 V			1	µA
EN, CHG, CHG_HI - LOGIC INPUTS						
V_{TH}	Rising threshold voltage			0.925	1.15	V
V_{TH}	Falling threshold voltage		0.65	0.875		V
	Hysteresis (2)			50		mV
I_{IN}	Input current	V_{EN} = 0 V or 6.5 V	–0.5		0.5	µA
OVER TEMPERATURE SHUT DOWN						
T_{TH_OTSD2}	Rising threshold temperature for device shutdown		155			°C
	Hysteresis (2)			20		°C
T_{TH_OTSD1}	Rising threshold temperature for OUT/ V_{CONN} switch shutdown in current limit		135			°C
	Hysteresis (2)			20		°C
IN1						
$V_{TH\_UVLO\_IN1}$	Rising threshold voltage for UVLO		3.9	4.1	4.3	V
	Hysteresis (2)			100		mV

Electrical Characteristics (continued)

–40°C ≤ T_J ≤ 125°C, 4.5 V ≤ V_{IN1} ≤ 6.5 V, 4.5 V ≤ V_{IN2} ≤ 5.5 V, 2.9 V ≤ V_{AUX} ≤ 5.5 V; V_{EN} = V_{CHG} = V_{CHG_HI} = V_{AUX}, R_{REF} = 100 kΩ. Typical values are at 25°C. All voltages are with respect to GND. I_{OUT} and I_{OS} defined positive out of the indicated pin (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_I	Disabled supply current	V_{EN} = 0 V, -40°C ≤ T_J ≤ 85°C			1	µA
	Enabled supply current with CC lines open	-40°C ≤ T_J ≤ 85°C			1	µA
	Enabled supply current with accessory or dangling electronically marked cable signature on CC lines				2	µA
	Enabled supply current with UFP attached	V_{CHG} = 0 V, or V_{CHG} = V_{AUX} and V_{CHG_HI} = 0 V		75	100	µA
				85	110	
IN2						
$V_{TH\_UVLO\_IN2}$	Rising threshold voltage for UVLO		3.9	4.1	4.3	V
	Hysteresis(2)			100		mV
I_I	Disabled supply current	V_{EN} = 0 V, -40°C ≤ T_J ≤ 85°C			1	µA
	Enabled supply current with CC lines open	-40°C ≤ T_J ≤ 85°C			1	µA
I_I	Enabled supply current with accessory or dangling electronically marked cable signature on CC lines				2	µA
I_I	Enabled supply current with UFP signature on CC lines (Includes IN current that provides the CC output current to the UFP Rd resistor)	V_{CHG} = 0 V, 0 V ≤ V_{CCx} ≤ 1.5 V		98	110	µA
		V_{CHG} = V_{IN} and V_{CHG_HI} = 0 V, 0 V ≤ V_{CCx} ≤ 1.5 V		198	215	
		0 V ≤ V_{CCx} ≤ 2.45 V		348	373	
AUX						
$V_{TH\_UVLO\_AUX}$	Rising threshold voltage for UVLO		2.65	2.75	2.85	V
	Hysteresis(2)			100		mV
I_I	Disabled supply current	V_{EN} = 0 V, -40°C ≤ T_J ≤ 85°C			1	µA
I_I	Enabled internal supply current with CC lines open	-40°C ≤ T_J ≤ 85°C		0.7	3	µA
I_I	Enabled supply current with accessory or dangling active cable signature on CC lines			140	185	µA
I_I	Enabled supply current with UFP termination on CC lines and with either IN1 or IN2 in UVLO	V_{IN1} < $V_{TH\_UVLO\_IN1}$ or V_{IN2} < $V_{TH\_UVLO\_IN2}$		145	190	µA
I_I	Enabled supply current with UFP termination on CC lines			55	82	µA

6.6 Switching Characteristics

–40°C ≤ T_J ≤ 125°C, 4.5 V ≤ V_{IN1} ≤ 6.5 V, 4.5 V ≤ V_{IN2} ≤ 5.5 V, 2.9 V ≤ V_{AUX} ≤ 5.5 V; V_{EN} = V_{CHG} = V_{CHG_HI} = V_{AUX}, R_{REF} = 100 kΩ. Typical values are at 25°C. All voltages are with respect to GND. I_{OUT} and I_{OS} defined positive out of the indicated pin (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUT - POWER SWITCH						
t_r	Output voltage rise time	V_{IN1} = 5 V, C_L = 1 µF, R_L = 100 Ω (measured from 10% to 90% of final value)	1.2	1.8	2.5	ms
t_f	Output voltage fall time		0.35	0.55	0.75	ms
t_{on}	Output voltage turn-on time	V_{IN1} = 5 V, C_L = 1 µF, R_L = 100 Ω	2.5	3.5	5	ms
t_{off}	Output voltage turn-off time		2	3	4.5	ms

Switching Characteristics (continued)

–40°C ≤ T_J ≤ 125°C, 4.5 V ≤ V_{IN1} ≤ 6.5 V, 4.5 V ≤ V_{IN2} ≤ 5.5 V, 2.9 V ≤ V_{AUX} ≤ 5.5 V; V_{EN} = V_{CHG} = V_{CHG_HI} = V_{AUX}, R_{REF} = 100 kΩ. Typical values are at 25°C. All voltages are with respect to GND. I_{OUT} and I_{OS} defined positive out of the indicated pin (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUT - CURRENT LIMIT						
t_{ios}	Current limit response time to short circuit	V_{IN1} - V_{OUT} = 1 V, R_L = 10 mΩ, see Figure 1		1.5	4	µs
$\overline{\text{FAULT}}$						
t_{DEGA}	Asserting deglitch due to over current		5.5	8.2	10.7	ms
t_{DEGA}	Asserting deglitch due to over temperature in current limit(1)			0		ms
t_{DEGD}	De-asserting deglitch		5.5	8.2	10.7	ms
$\overline{\text{LD\_DET}}$						
t_{DEGA}	Asserting deglitch		45	65	85	ms
t_{DEGD}	De-asserting deglitch		1.45	2.15	2.9	s
OUT - DISCHARGE						
	R_{DCHG} discharge time	V_{OUT} = 1 V, time I_{SNK_OUT} > 1 mA after UFP signature removed from CC lines	39	65	96	ms
CC1/CC2 - V_{CONN} POWER SWITCH						
t_r	Output voltage rise time	V_{IN2} = 5 V, C_L = 1 µF, R_L = 100 Ω (measured from 10% to 90% of final value)	0.15	0.25	0.35	ms
t_f	Output voltage fall time		0.18	0.22	0.26	ms
t_{on}	Output voltage turn-on time	V_{IN2} = 5 V, C_L = 1 µF, R_L = 100 Ω	1	1.5	2	ms
t_{off}	Output voltage turn-off time		0.3	0.4	0.55	ms
CC1/CC2 - V_{CONN} POWER SWITCH - CURRENT LIMIT						
t_{res}	Current limit response time to short circuit	V_{IN2} – V_{CONN} = 1 V, R = 10 mΩ, see Figure 1		1	3	µs
$\overline{\text{UFP}}$, $\overline{\text{POL}}$, $\overline{\text{AUDIO}}$, $\overline{\text{DEBUG}}$						
t_{DEGR}	Asserting deglitch		100	150	200	ms
t_{DEGF}	De-asserting deglitch		7.9	12.5	17.7	ms

(1) These parameters are provided for reference only and do not constitute part of TI's published specifications for purposes of TI's product warranty.

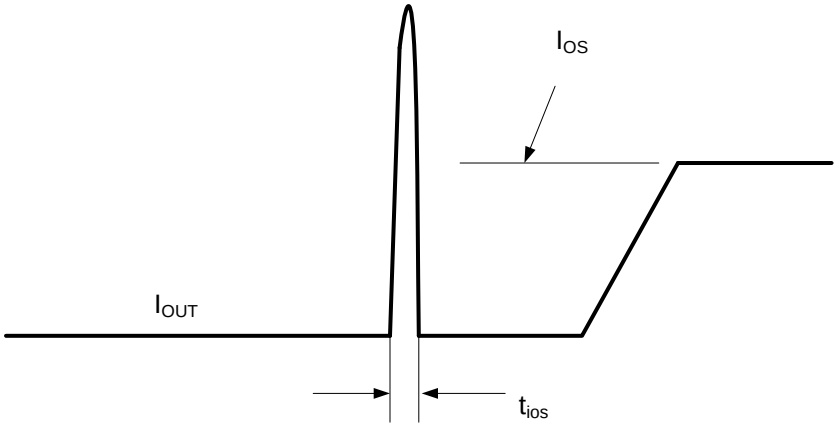


Figure 1. Output Short Circuit Parameter Diagram

6.7 Typical Characteristics

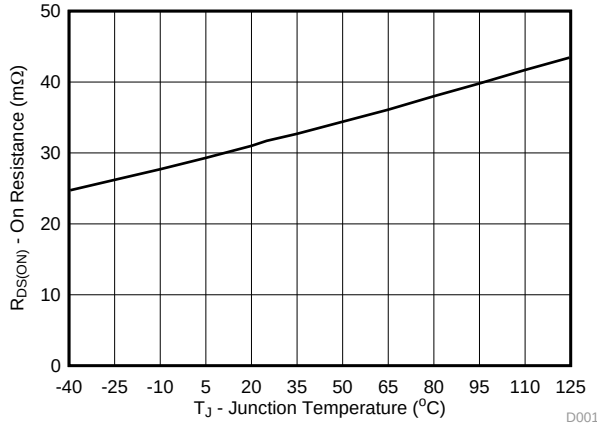


Figure 2. VBUS Current Limiting Switch On Resistance vs Temperature

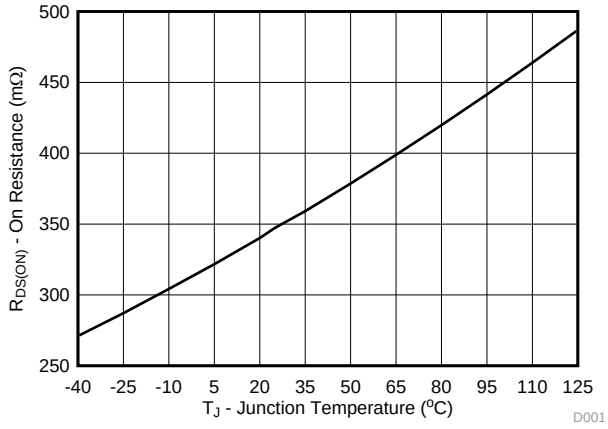
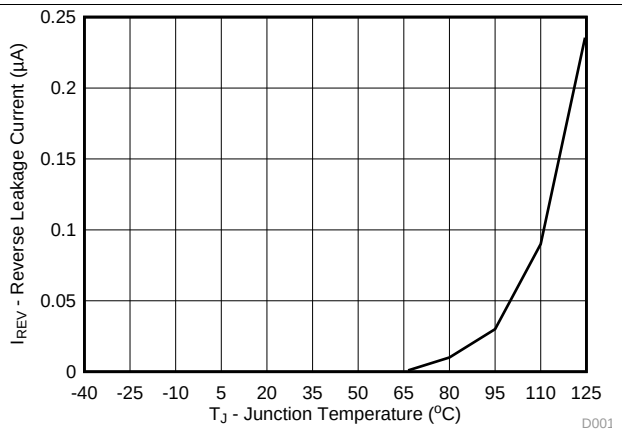


Figure 3. VCONN Current Limiting Switch On Resistance vs Temperature



Device = Disabled; (VOUT-VIN) =6.5V

Figure 4. OUT Reverse Leakage Current vs Temperature

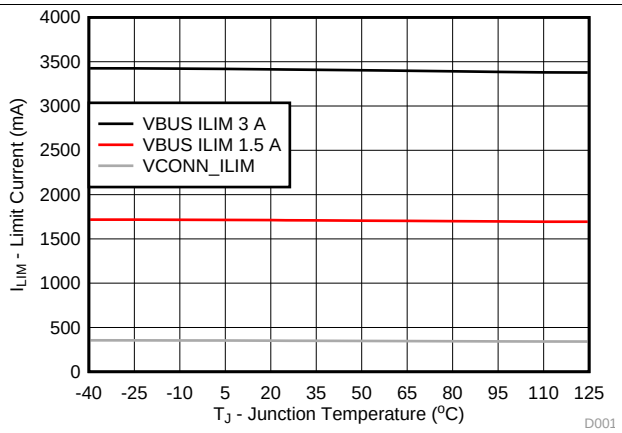


Figure 5. ILIM for VBUS and VCON vs Temperature

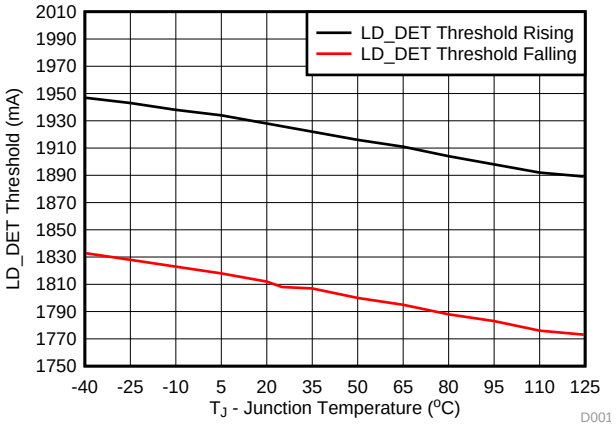


Figure 6. LD_DET Threshold vs Temperature

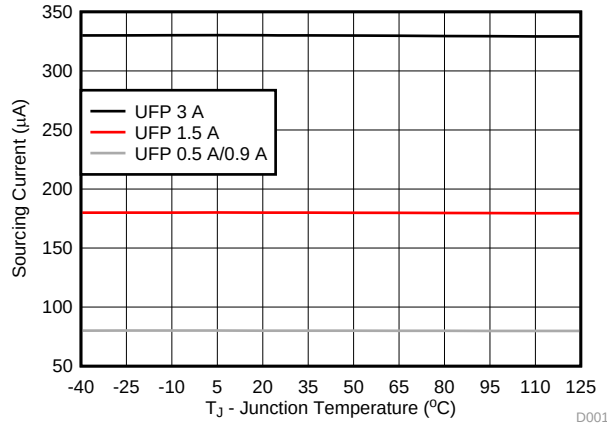


Figure 7. CC Sourcing Current to UFP vs Temperature

Typical Characteristics (continued)

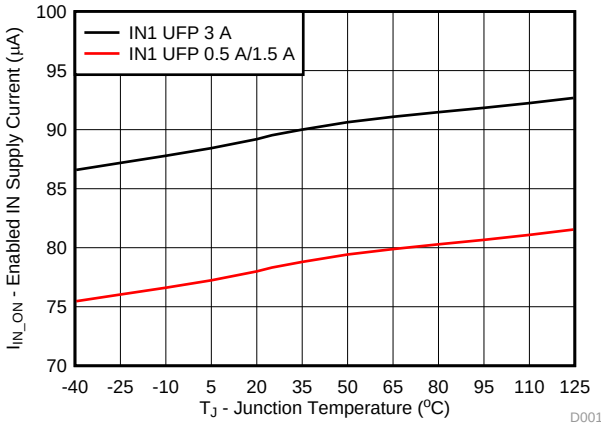


Figure 8. IN1 Current with UFP vs Temperature

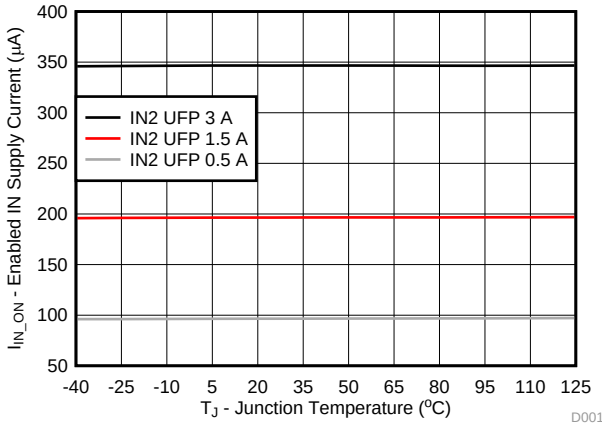
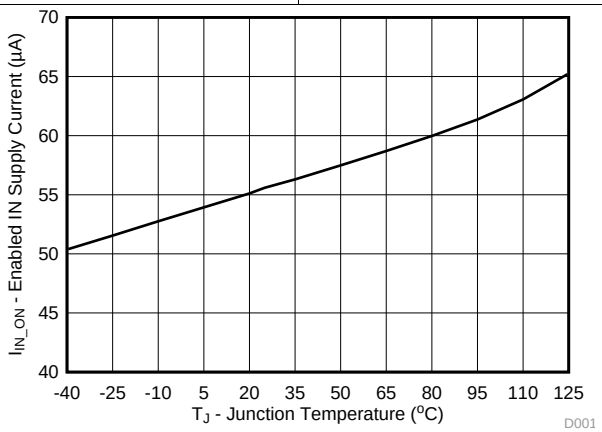


Figure 9. IN2 Current with UFP vs Temperature



V_{AUX} = 5 V

Figure 10. AUX Current with UFP vs Temperature

7 Detailed Description

7.1 Overview

The TPS25810 is a highly integrated USB Type-C Downstream Facing Port (DFP) controller with built-in power switch developed for the new USB Type-C connector and cable. The part provides all functionality needed to support a USB Type C DFP in a system where USB power delivery (PD) source capabilities (for example, VBUS > 5 V) are not implemented. The device is designed to be compliant to Type-C spec revision 1.1.

7.1.1 USB Type C Basic

For a detailed description of the Type-C spec refer to the USB-IF website to download the latest released version. Some of the basic concepts of the Type-C spec that pertains to understanding the operation of the TPS25810 (a DFP device) are described as follows.

USB Type-C removes the need for different plug and receptacle types for host and device functionality. The Type-C receptacle replaces both Type-A and Type-B receptacle since the Type-C cable is plug-able in either direction between host and device. A host-to-device logical relationship is maintained via the configuration channel (CC). Optionally hosts and devices can be either providers or consumers of power when USB PD communication is used to swap roles.

All USB Type-C ports operate in one of below three data modes:

- Host mode: the port can only be host (provider of power)
- Device mode: the port can only be device (consumer of power)
- Dual-Role mode: the port can be either host or device

Port types:

- DFP (Downstream Facing Port): Host
- UFP (Upstream Facing Port): Device
- DRP (Dual-Role Port): Host or Device

Valid DFP-to-UFP connections:

- Table 1 describes valid DFP-to-UFP connections
- Host to Host or Device to Device have no functions

Table 1. DFP-to-UFP Connections

	HOST-MODE PORT	DEVICE-MODE PORT	DUAL-ROLE PORT
Host-Mode Port	No Function	Works	Works
Device-Mode Port	Works	No Function	Works
Dual-Role Port	Works	Works	Works(1)

(1) This may be automatic or manually driven.

7.1.2 Configuration Channel

The function of the configuration channel is to detect connections and configure the interface across the USB Type-C cables and connectors.

Functionally the Configuration Channel (CC) is used to serve the following purposes:

- Detect connect to the USB ports
- Resolve cable orientation and twist connections to establish USB data bus routing
- Establish DFP and UFP roles between two connected ports
- Discover and configure power: USB Type-C current modes or USB Power Delivery
- Discovery and configure optional Alternate and Accessory modes
- Enhances flexibility and ease of use

Typical flow of DFP to UFP configuration is shown in Figure 11:

Figure 11. Flow of DFP to UFP Configuration

7.1.3 Detecting a Connection

DFPs and DRPs fulfill the role of detecting a valid connection over USB Type-C. Figure 12 shows a DFP to UFP connection made with Type C cable. As shown in Figure 12, the detection concept is based on being able to detect terminations in the product which has been attached. A pull-up and pull-down termination model is used. A pull-up termination can be replaced by a current source.

- In the DFP-UFP connection the DFP monitors both CC pins for a voltage lower than the unterminated voltage.
- An UFP advertises Rd on both its CC pins (CC1 and CC2).
- A powered cable advertises Ra on only one of CC pins of the plug. Ra is used to inform the source to apply VCONN.
- An analog audio device advertises Ra on both CC pins of the plug, which identifies it as an analog audio device. VCONN is not applied on either CC pin in this case.

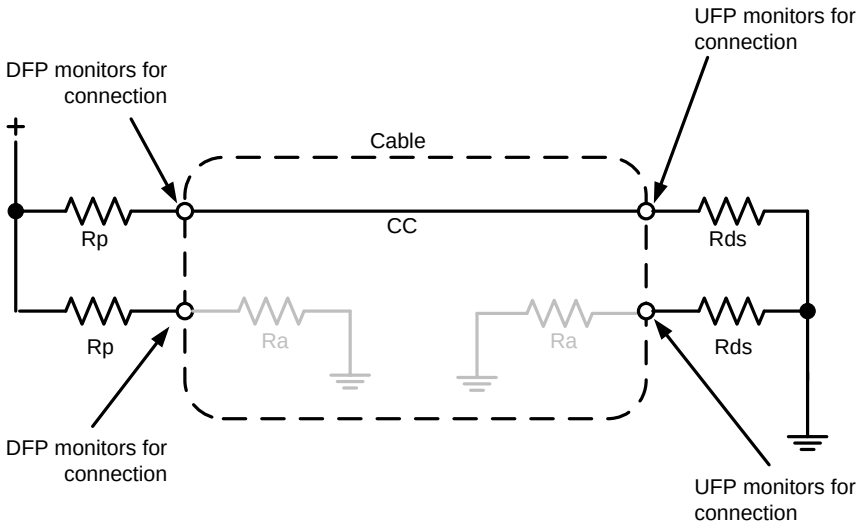
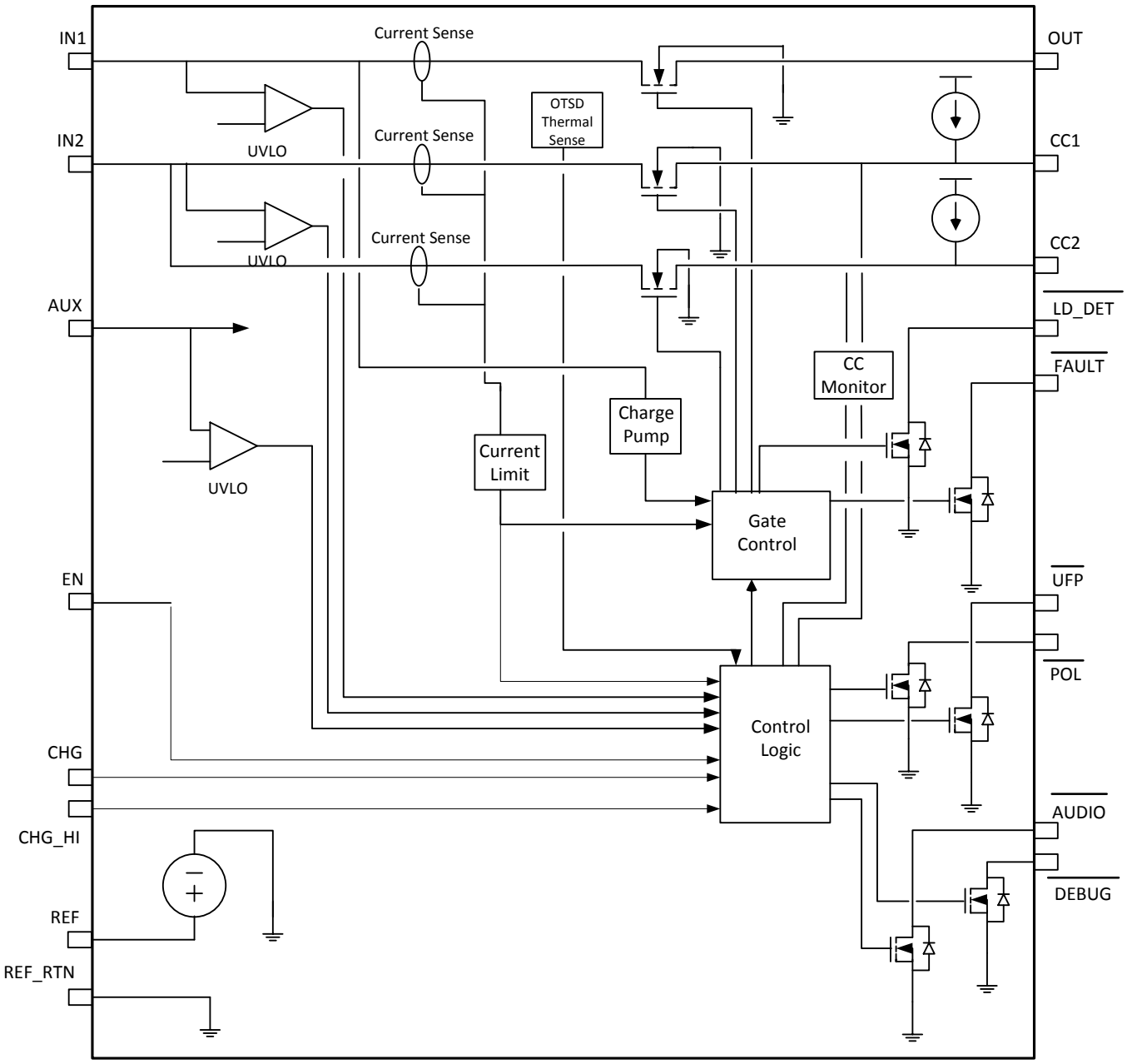


Figure 12. DFP-UFP Connection

7.2 Functional Block Diagram



7.3 Feature Description

The TPS25810 is a DFP Type C port controller with integrated power switch for VCONN and VBUS. The TPS25810 does not support BC1.2 charging modes since it does not interact with USB D+/D- data lines. It can be used in conjunction with a BC 1.2 device like the TPS2514A, to support BC1.2 and Type C charging modes in a single Type C DFP port. See the TPS25810 EVM user's guide (SLVUAI0) and *Application and Implementation* section of this data sheet for more details. The TPS25810 can be used in a USB 2.0 only or USB 3.1 port implementation. When used in a USB 3.1 port, the TPS25810 can control an external super speed MUX to handle the Type C flippable feature.

Feature Description (continued)

7.3.1 Configuration Channel Pins CC1 and CC2

The TPS25810 has two pins, CC1 and CC2 that serve to detect an attachment to the port and resolve cable orientation. These pins are also used to establish current broadcast to a valid UFP, configure VCONN, and detect Debug or Audio Adapter Accessory attachment.

Table 2 lists TPS25810 response to various attachments to its port.

Table 2. TPS25810 Response

TPS25810 TYPE C PORT	CC1	CC2	TPS25810 RESPONSE(1)					
			OUT	V_{CONN} On CC1 or CC2	$\overline{POL}$	$\overline{UFP}$	$\overline{AUDIO}$	$\overline{DEBUG}$
Nothing Attached	OPEN	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
UFP Connected	Rd	OPEN	IN1	NO	Hi-Z	LOW	Hi-Z	Hi-Z
UFP Connected	OPEN	Rd	IN1	NO	LOW	LOW	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	OPEN	Ra	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	Ra	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Rd	Ra	IN1	CC2	Hi-Z	LOW	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Ra	Rd	IN1	CC1	LOW	LOW	Hi-Z	Hi-Z
Debug Accessory Connected	Rd	Rd	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	LOW
Audio Adapter Accessory Connected	Ra	Ra	OPEN	NO	Hi-Z	Hi-Z	LOW	Hi-Z

(1) $\overline{POL}$, $\overline{UFP}$, $\overline{AUDIO}$, and $\overline{DEBUG}$ are open drain outputs; pull high with 100 kΩ to AUX when used. Tie to GND or leave open when not used.

7.3.2 Current Capability Advertisement and Overload Protection

The TPS25810 supports all three Type-C current advertisements as defined by the USB Type C standard. Current broadcast to a connected UFP is controlled by the CHG and CHG_HI pins. For each broadcast level the device protects itself from a UFP that draws current in excess of the port's USB Type-C Current advertisement by setting the current limit as shown in Table 3.

Table 3. USB Type-C Current Advertisement

CHG	CHG_HI	CC CAPABILITY BROADCAST	CURRENT LIMIT (typ)	LOAD DETECT THRESHOLD (typ)
0	0	STD	1.7 A	NA
0	1	STD	1.7 A	NA
1	0	1.5 A	1.7 A	NA
1	1	3 A	3.4 A	1.95 A

Under overload conditions, the internal current-limit regulator limits the output current to selected ILIM for OUT and fixed internal VCONN current limit as shown in the *Electrical Characteristics*. When an overload condition is present, the device maintains a constant output current, with the output voltage determined by (i_{OS} x RLOAD). Two possible overload conditions can occur. The first overload condition occurs when either: 1) input voltage is first applied, enable is true, and a short circuit is present (load which draws IOUT > i_{OS}), or 2) input voltage is present and the TPS25810 is enabled into a short circuit. The output voltage is held near zero potential with respect to ground and the TPS25810 ramps the output current to i_{OS}. The TPS25810 limits the current to i_{OS} until the overload condition is removed or the device begins to thermal cycle. This is demonstrated in Figure 24 where the device was enabled into a short, and subsequently cycles current off and on as the thermal protection engages.

The second condition is when an overload occurs while the device is enabled and fully turned on. The device responds to the overload condition within time i_{OS} (see Figure 1) when the specified overload (per *Electrical Characteristics*) is applied. The response speed and shape vary with the overload level, input circuit, and rate of application. The current-limit response varies between simply settling to i_{OS} or turnoff and controlled return to i_{OS}. Similar to the previous case, the TPS25810 limits the current to i_{OS} until the overload condition is removed or the device begins to thermal cycle.

The TPS25810 thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the above cases. This is due to the relatively large power dissipation [(VIN – VOUT) x i_{OS}] driving the junction temperature up. The device turns off when the junction temperature exceeds 135°C (min) while in current limit. The device remains off until the junction temperature cools 20°C and then restarts. The TPS25810 current limit profile is shown in Figure 13.

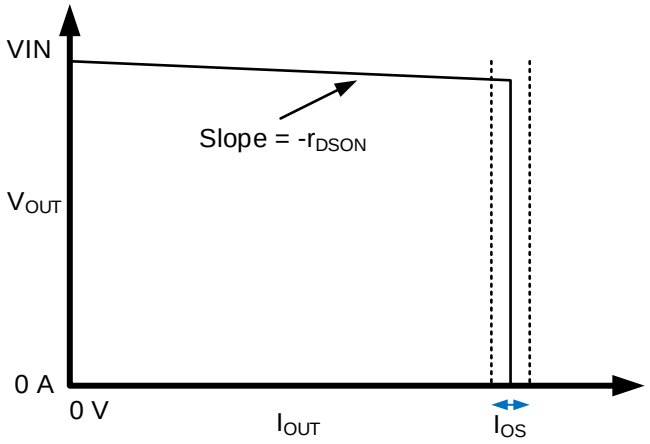


Figure 13. Current Limit Profile

7.3.3 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted on/off cycling due to input voltage droop during turn on.

7.3.3.1 Device Power Pins (IN1, IN2, AUX, OUT, and GND)

The device has multiple input power pins; IN1, IN2 and AUX. IN1 is connected to OUT by the internal power FET and serves the supply for the Type-C charging current. IN2 is the supply for VCONN and ties directly between the VCONN power switch on its input and CC1 or CC2 on its output. AUX or auxiliary input supply provides power to the chip. Refer to *Functional Block Diagram*.

In the simplest implementation where multiple supplies are not available; IN1, IN2, and AUX can be tied together. However in mobile systems (battery powered) where system power savings is paramount, IN1 and IN2 can be powered by the high power DC-DC supply (>3-A capability) while AUX can be connected to the low power supply that typically powers the system uC when the system is in hibernate or sleep power state. Unlike IN1 and IN2, AUX can operate directly from a 3.3-V supply commonly used to power the uC when the system is put in low power mode. A ceramic bypass capacitor close to the device from IN/AUX to GND is recommended to alleviate bus transients.

The recommended operating voltage range for IN1/IN2 is 4.5 V to 5.5 V while AUX can be operated from 2.9 V to 5.5 V. However IN1, the high power supply, can operate up to 6.5 V. This higher input voltage affords a larger IR drop budget in systems where a long cable harness is used and results in high IR drops with 3-A charging current. Increasing IN1 beyond 5.5 V enables longer cable/board trace lengths between the device and Type C receptacle while meeting the USB spec for VBUS at connector ≥ 4.75 V.

Figure 14 illustrates the point. In this example IN1 is at 5 V which restricts the IR drop budget from DC-DC to connector to 250 mV.

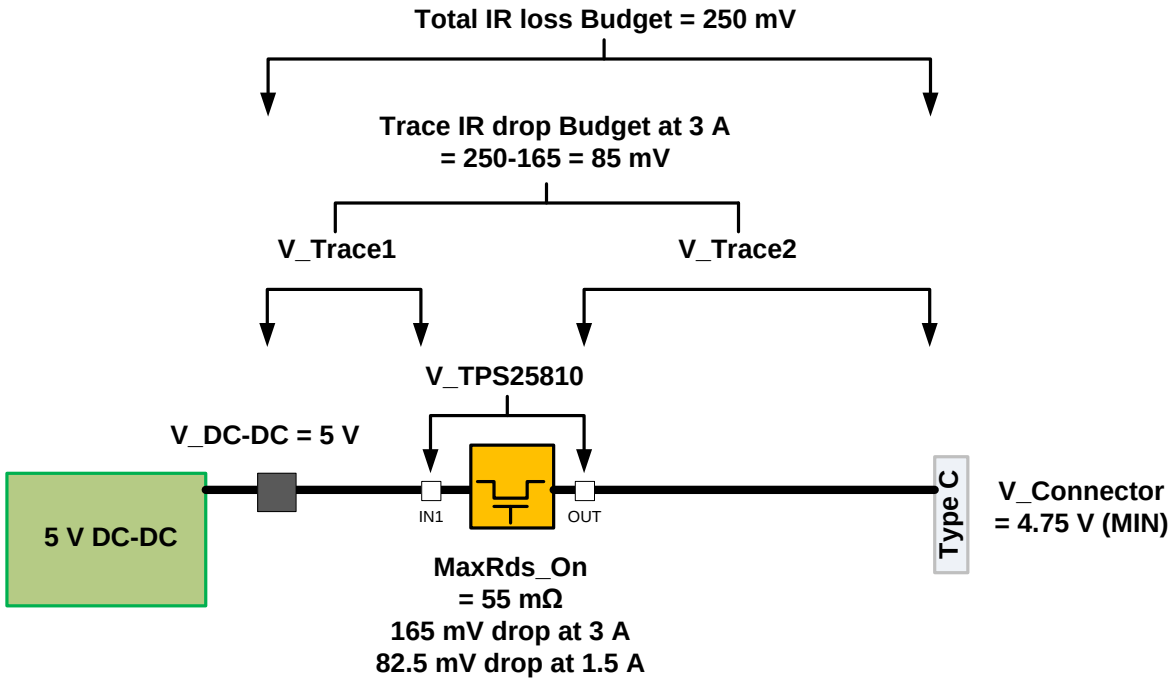


Figure 14. Total IR Loss Budget

7.3.3.2 FAULT Response

The $\overline{\text{FAULT}}$ pin is an open drain output that asserts (active low) when device OUT current exceeds its programmed value and the over temperature threshold is crossed (T_{TH_OTSD1}). Refer to the *Electrical Characteristics* for over current and temperature values. The $\overline{\text{FAULT}}$ signal remains asserted until the fault condition is removed and the device resumes normal operation. The TPS25810 is designed to eliminate false overcurrent fault reporting by using an internal deglitch circuit.

Connect $\overline{\text{FAULT}}$ with a pull-up resistor to AUX. $\overline{\text{FAULT}}$ can be left open or tied to GND when not used.

7.3.3.3 Thermal Shutdown

The device has two internal over temperature shutdown thresholds, T_{TH_OTSD1} and T_{TH_OTSD2}, to protect the internal FET from damage and overall safety of the system. $T_{TH\_OTSD2} > T_{TH\_OTSD1}$. $\overline{\text{FAULT}}$ is asserted low to signal a fault condition when device temperature exceeds T_{TH_OTSD1} and the current limit switch is disabled. However when T_{TH_OTSD2} is exceeded all open drain outputs are left open and the device is disabled such that minimum power/heat is dissipated. The device attempts to power-up when die temperature decreases by 20°C.

7.3.3.4 REF

A 100-kΩ (1% or better recommended) resistor is connected from this pin to REF_RTN. This pin sets the reference current required to bias the internal circuitry of the device. The overload current limit tolerance and CC currents depend upon the accuracy of this resistor, using a ±1% low tempco resistor, or better, yields the best current limit accuracy and overall device performance.

7.3.3.5 Audio Accessory Detection

The USB Type-C spec defines an audio adapter decode state which allows implementation of an analog USB Type-C to 3.5-mm headset adapter. The TPS25810 detects an audio accessory device when both CC1 and CC2 pins sees V_{Ra} voltage (when pulled to ground by Ra resistor). The device asserts the open drain $\overline{\text{AUDIO}}$ pin low to indicate the detection of such a device.

Table 4. Audio Accessory Detection

CC1	CC2	$\overline{\text{AUDIO}}$	STATE
Ra	Ra	Asserted (pulled low)	Audio Adapter Accessory Connected

Platforms supporting this extension can trigger off of the $\overline{\text{AUDIO}}$ pin to enable accessory mode circuits to support the audio function. When the Ra pull-down is removed from the CC2 pin, $\overline{\text{AUDIO}}$ is de-asserted or pulled high. The TPS25810 monitors the CC2 pin for audio device detach. When this function is not needed (for example in a data-less port) $\overline{\text{AUDIO}}$ can be tied to GND or left open.

7.3.3.6 Debug Accessory Detection

The Type-C spec supports an optional Debug Accessory mode used for debug only and must not be used for communicating with commercial products. When the TPS25810 detects V_{Rd} voltage on both CC1 and CC2 pins (when pulled to ground by an Rd resistor), it asserts $\overline{\text{DEBUG}}$ low. With $\overline{\text{DEBUG}}$ is asserted, the system can enter debug mode for factory testing or a similar functional mode. $\overline{\text{DEBUG}}$ de-asserts or pulls high when Rd is removed from CC1. The TPS25810 monitors the CC1 pin for Debug Accessory detach.

If Debug accessory mode is not used, tie $\overline{\text{DEBUG}}$ to GND or leave it open.

Table 5. Debug Accessory Detection

CC1	CC2	$\overline{\text{POL}}$	STATE
Rd	Rd	Asserted (pulled low)	Debug Accessory Mode connected

7.3.3.7 Plug Polarity Detection

Reversible Type-C plug orientation is reported by the $\overline{\text{POL}}$ pin when a UFP is connected. However when no UFP is attached, $\overline{\text{POL}}$ remains de-asserted irrespective of cable plug orientation. Table 6 describes the $\overline{\text{POL}}$ state based on which device CC pin detects V_{RD} from an attached UFP pull-down.

Table 6. Plug Polarity Detection

CC1	CC2	$\overline{\text{POL}}$	STATE
Rd	Open	Hi-z	UFP connected
Open	Rd	Asserted (pulled low)	UFP connected with reverse plug orientation

Figure 15 shows an example implementation which utilizes the $\overline{\text{POL}}$ terminal to control the SEL terminal on the HD3SS3212. The HD3SS3212 provides switching on the differential channels between Port B and Port C to Port A depending on cable orientation.

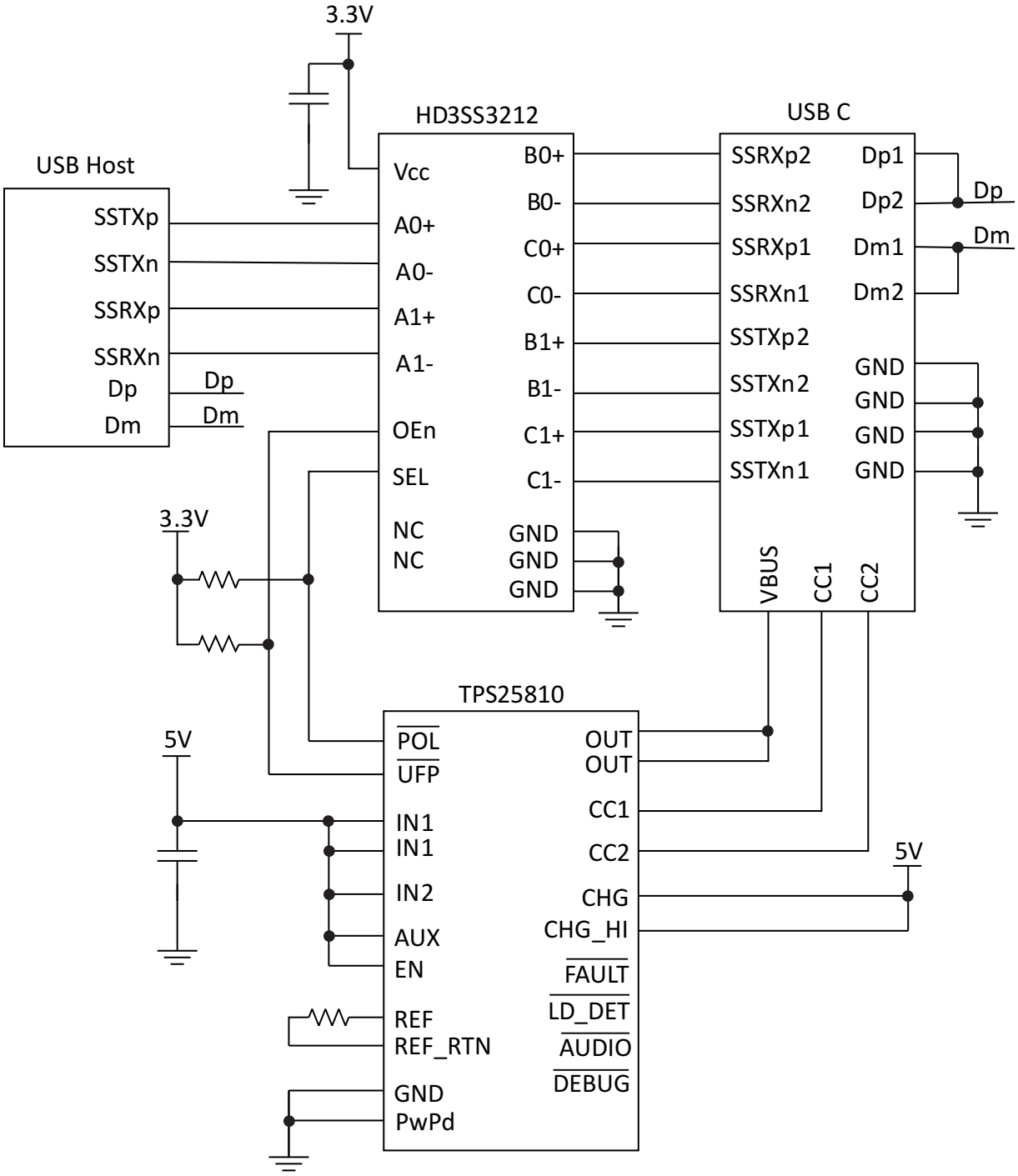


Figure 15. Example Implementation

7.3.3.8 Device Enable Control

The logic enable pin controls the power switch and device supply current. The supply current is reduced to less than 1 µA when a logic low is present on EN. The EN pin provides a convenient way to turn on or turn off the device while it is powered. The enable input threshold has hysteresis built-in. When this pin is pulled high, the device is turned on or enabled. When the device is disabled (EN pulled low) the internal FETs tied to IN1 and IN2 are disconnected, all open drain outputs are left open (Hi-Z), and the CC1/CC2 monitor block is turned off. The EN terminal should not be left floating.

7.3.3.9 Load Detect

The load detect function in the device is enabled when it is set to broadcast high current V_{BUS} charging (CHG = CHG_HI = High) on the CC pin. In this mode the device monitors the current to a UFP; if the current exceeds 1.95 A (TYP) the LD_DET pin asserts. Since LD_DET is an open drain output, pull it high with 100 kΩ to AUX when used; tie it to GND or leave open when not used.

7.3.3.10 Power Wake

The power wake feature supported in the TPS25810 offers the mobile systems designer a way to save on system power when no UFP is attached to the Type-C port. Refer to Figure 16. To enable power wake the UFP from device #1 and #2 are tied together (each with its own 100-kΩ pull-up) to the enable pin of a 5 V/6 A dc-dc buck converter. When no UFP is detected on both Type-C ports, the EN pin of the dc-dc is pulled high thereby disabling it. Since both TPS25810s are powered by an always-on 3.3-V LDO, turning off the IN1/IN2 supply does not affect its operation in detach state. Anytime a UFP is detected on either port, the corresponding TPS25810 UFP pin is pulled low enabling the dc-dc to provide charging current to the attached UFP. Turning off the high power dc-dc when ports are unattached saves on system power. This method can save a significant amount of power considering the TPS25810 only requires < 5 µA when no UFP device is connected.

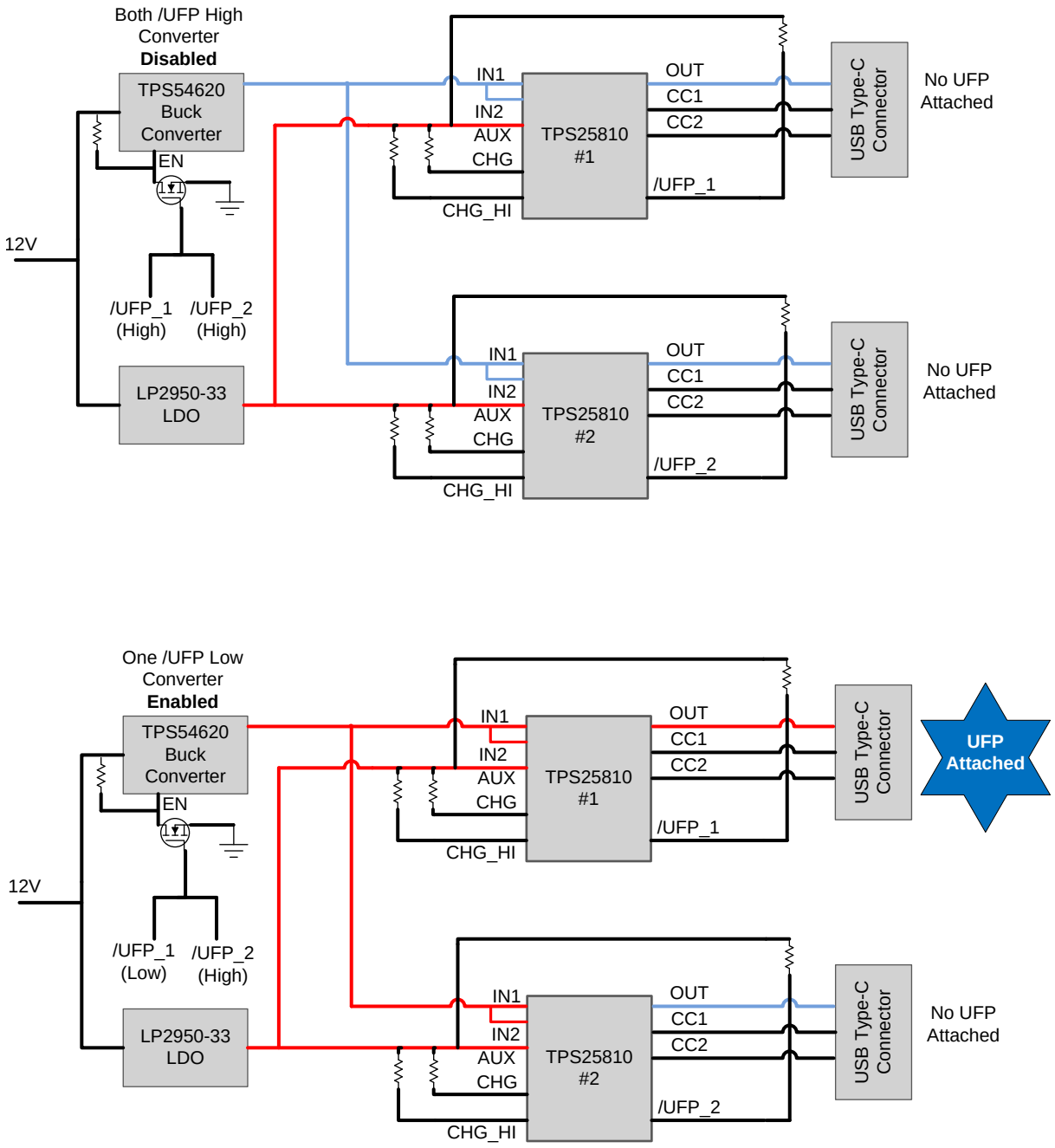


Figure 16. Power Wake Implementation

7.3.3.11 Port Power Management (PPM)

PPM is the intelligent and dynamic allocation of power made possible with the use of the $\overline{\text{LD\_DET}}$ pin. It is for systems that have multiple charging ports but cannot power them all at their maximum charging current simultaneously.

Goals of PPM are:

1. Enhances user experience since user does not have to search for high current charging port.
2. Lowered cost and size of power supply needed for implementing high current charging in a multi-port system.

7.3.3.12 Implementing PPM in a System with Two Type-C Ports

Figure 17 shows PPM and power wake implemented in a system with two Type C ports both initially set to broadcast high current charging (3 A, CHG and CHG_HI pulled high via a 100 kΩ to AUX). To enable PPM tie the LD_DET pin from TPS25810 #1 to CHG_HI of TPS25810 #2 and vice versa as shown in Figure 17. Each device independently monitors charging current drawn by its attached UFP.

IN1, IN2 are connected to a TPS54620; a 6-A synchronous step-down converter. AUX is powered by a LP2950-33; a low quiescent current 3.3-V LDO. With no UFP attached to either Type C port the TPS25810 is powered by the LP2950-33. This method saves a significant amount of power considering the TPS25810 requires less than 2 µA when no USB device is connected.

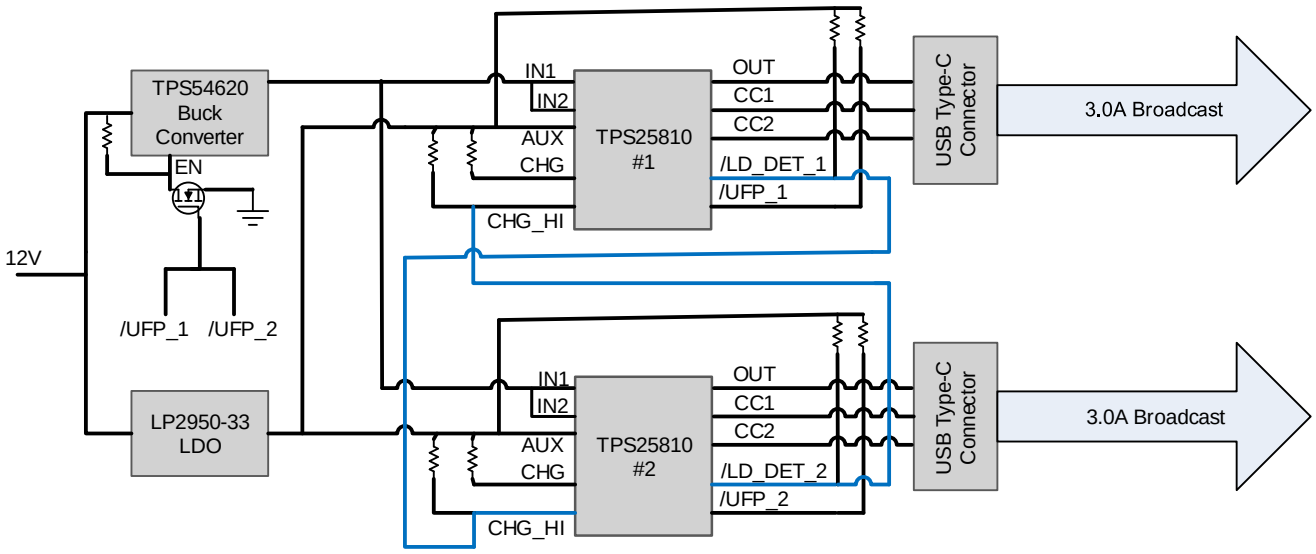


Figure 17. PPM and Power Wake Implemented

7.3.3.13 PPM Operation

When no UFP is attached, or either of the two attached UFP is drawing current less than the LD_DET threshold (1.95 A typical), the LD_DET output for both devices is high (shown in blue in Figure 18). Now when a UFP is attached to device #1 that draws a charging current higher than the LD_DET threshold (1.95 A), this causes LD_DET to assert or pull-low (shown in red in Figure 18). Since the LD-DET pins of the #1 and #2 devices are connected to the other devices CHG_HI pin, a high current detection on device #1 forces device #2 to broadcast 1.5 A or medium charging current capability on its CC pin. The Type C specification requires a UFP to monitor the CC pins continuously and adjust its current consumption (within 60 ms) to remain within the value advertised by the DFP.

Figure 19 shows the case when a UFP attached to Device 1 reduces its charging current below the LD_DET threshold, which causes LD-DET to de-assert, thereby toggling device #2 CH_HI pin from low to high.

This scheme:

- Delivers a better user experience as the user does not have to worry about the maximum charging current rating of the host ports, both ports initially advertise high current charging.
- Enables a smaller and lower cost power supply as the loading is controlled and never allowed to exceed 5 A.

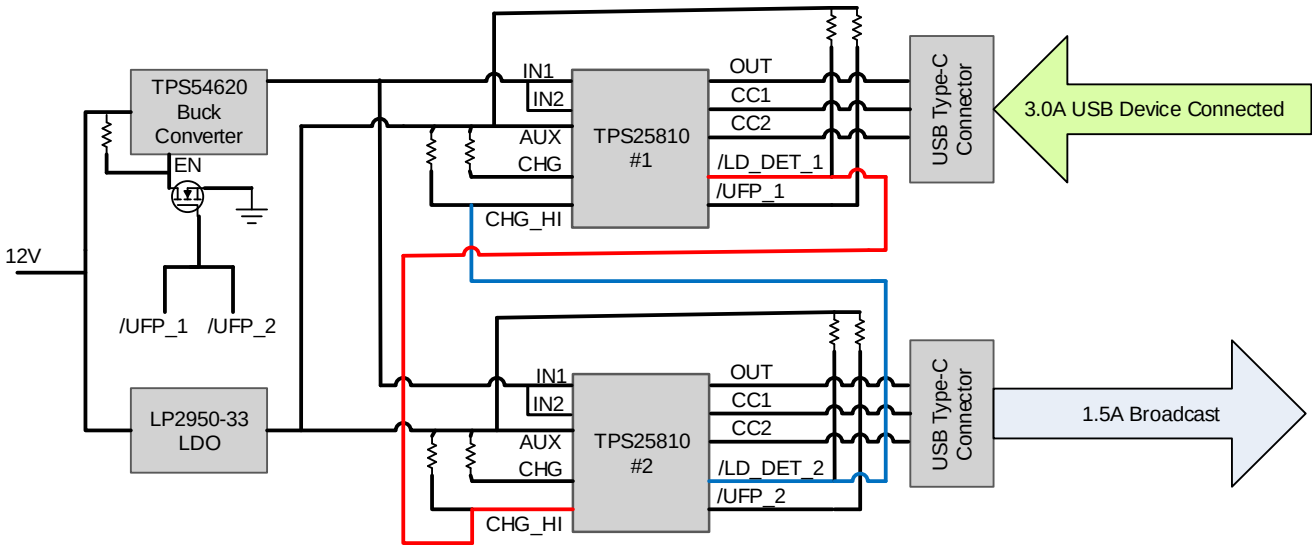


Figure 18. 3-A USB Device Connected

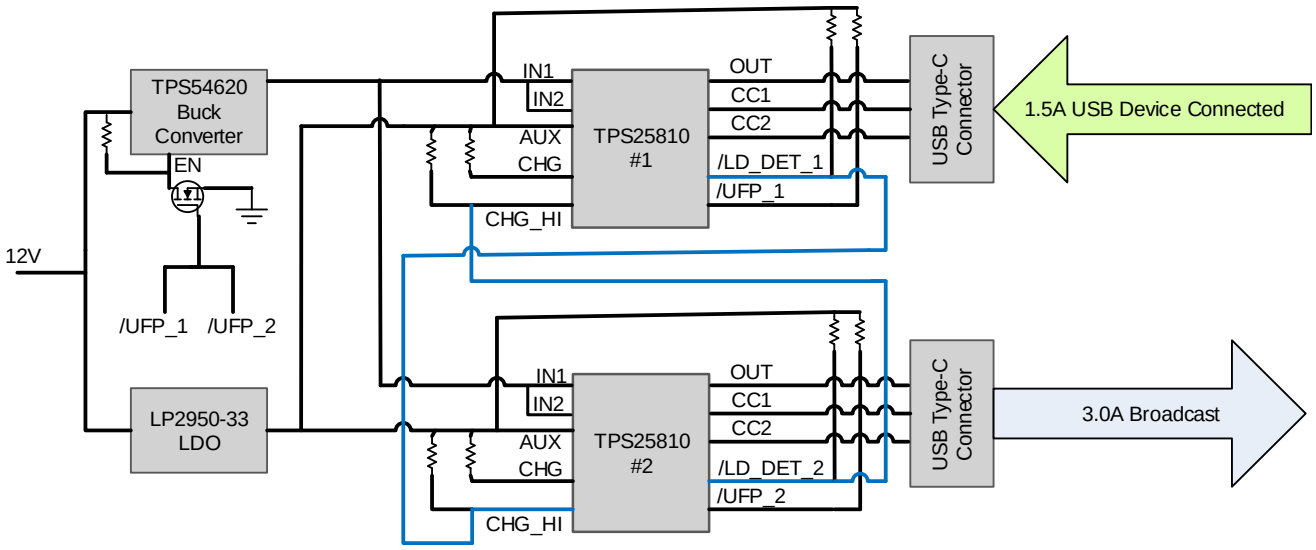


Figure 19. 1.5-A USB Device Connected

7.4 Device Functional Modes

The TPS25810 is a Type-C controller with integrated power switch that supports all Type-C functions in a downstream facing port. It is also used to manage current advertisement and protection to a connected UFP and active cable. The device starts its operation by monitoring the AUX bus. When VAUX exceeds the under voltage-lockout threshold, the device samples the EN pin. A high level on this pin enables the device and normal operation begins. Having successfully completed its start-up sequence, the device now actively monitors its CC1 and CC2 pins for attachment to a UFP. When a UFP is detected on either the CC1 or CC2 pin the internal MOSFET starts to turn-on after the required de-bounce time is met. The internal MOSFET starts conducting and allows current to flow from IN1 to OUT. If Ra is detected on the other CC pin (not connected to UFP), VCONN is applied to allow current to flow from IN2 to the CC pin connected to Ra. For a complete listing of various device operational modes refer to Table 2.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS25810 is a Type-C DFP controller that supports all Type-C DFP required functions. The TPS25810 only applies power to V_{BUS} when it detects that a UFP is attached and removes power when it detects the UFP is detached. The device exposes its identity via its CC pin advertising its current capability based on CHG and CHG_HI pin settings. The TPS25810 also limits its advertised current internally and provides robust protection to a fault on the system V_{BUS} power rail.

After a connection is established by the TPS25810, the device is capable of providing V_{CONN} to power circuits in the cable plug on the CC pin that is not connected to the CC wire in the cable. V_{CONN} is internally current limited and has its own supply pin IN2. Apart from providing charging current to a UFP, the TPS25810 also supports Audio and Debug accessory modes.

The following design procedure can be used to implement a full featured Type-C DFP.

NOTE

BC 1.2 is not supported in the TPS25810. To support BC1.2 with Type-C charging modes in a single C connector, a device like a TPS2514A will need to be used.

8.2 Typical Applications

8.2.1 Type C DFP Port Implementation without BC 1.2 Support

Figure 20 shows a minimal Type-C DFP implementation capable of supporting 5-V and 3-A charging.

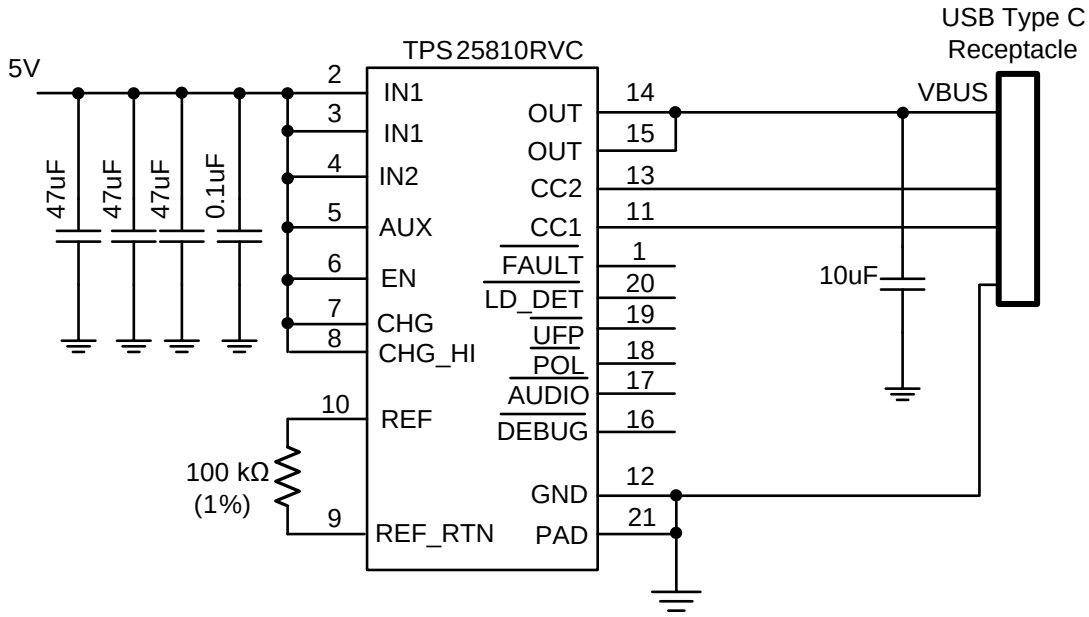


Figure 20. Type-C DFP Port Implementation without BC 1.2 Support

Typical Applications (continued)

8.2.1.1 Design Requirements

8.2.1.1.1 Input and Output Capacitance

Input and output capacitance improves the performance of the device. The actual capacitance should be optimized for the particular application. For all applications, a 0.1-µF or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise de-coupling.

All protection circuits such as the TPS25810 have the potential for input voltage overshoots and output voltage undershoots. Input voltage overshoots can be caused by either of two effects. The first cause is an abrupt application of input voltage in conjunction with input power bus inductance and input capacitance when the IN terminal is high impedance (before turn on). Theoretically, the peak voltage is 2 times the applied. The second cause is due to the abrupt reduction of output short circuit current when the TPS25810 turns off and energy stored in the input inductance drives the input voltage high. Input voltage droops may also occur with large load steps and as the TPS25810 output is shorted. Applications with large input inductance (for instance connecting the evaluation board to the bench power-supply through long cables) may require large input capacitance to reduce the voltage overshoot from exceeding the absolute maximum voltage of the device.

The fast current-limit speed of the TPS25810 to hard output short circuits isolate the input bus form faults. However, ceramic input capacitance in the range of 1 µF to 22 µF adjacent to the TPS25810 input aids in both response time and limiting the transient seen on the input power bus. Momentary input transients to 6.5 V are permitted. Output voltage undershoot is caused by the inductance of the output power bus just after a short has occurred and the TPS25810 has abruptly reduced OUT current. Energy stored in the inductance drives the OUT voltage down and potentially negative as it discharges. An application with large output inductance (such as from a cable) benefits from use of a high-value output capacitor to control voltage undershoot.

When implementing a USB standard application, 120 µF minimum output capacitance is required. Typically a 150-µF electrolytic capacitor is used, which is sufficient to control voltage undershoots. Since in Type-C DFP is a cold socket when no UFP is attached, the output capacitance should be placed at the IN pin versus OUT as is used in USB Type A ports. It is also recommended to put a 10-µF ceramic capacitor on the OUT pin for better voltage bypass.

8.2.1.2 Detailed Design Procedure

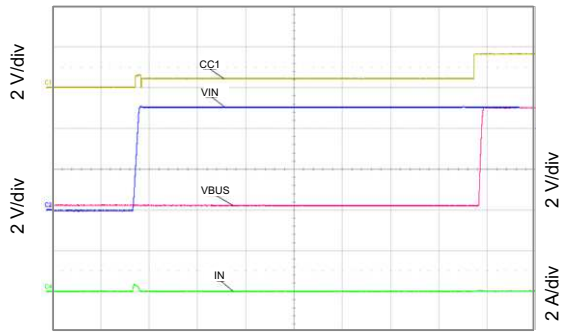
The TPS25810 device supports three different input voltages based on the application. In the simplest implementation all input supplies are tied to a single voltage source as shown in Figure 20 which is set to 5 V. However, it is recommended to set a slightly higher (100 mV to 200 mV) input voltage, when possible, to compensate for IR drop from the source to the Type C connector.

Other design considerations are listed below:

- Place at least 120 µF of bypass capacitance close to the IN pins versus OUT as Type C is a cold socket connector.
- A 10-µF bypass capacitor is recommended placed near a Type-C receptacle V_{BUS} pin to handle load transients.
- Depending on the max current level advertisement supported by the Type-C port in the system, set CHG and CHG_HI levels accordingly. 3 A advertisement is shown in Figure 20.
- EN, CHG, and CHG_HI pins can be tied directly to GND or VAUX without a pull-up resistor.
  - CHG and CHG_HI can also be dynamically controlled by a µC to change the current advertisement level to the UFP.
- When an open drain output of the TPS25810 is not used, it can be left as NC or tied to GND.
- Use a 1% 100-kΩ resistor to connect between the REF and REF_RTN pins placing it close to the device pin and isolated from switching noise on the board.

Typical Applications (continued)

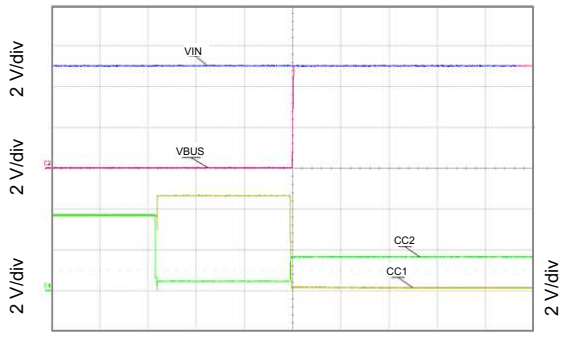
8.2.1.3 Application Curves



Time 20 ms/div

Basic Start-Up: IN1 = IN2 = AUX = EN = CHG = CHG_HI = 5 V, CC1 = Rd, CC2 = Open

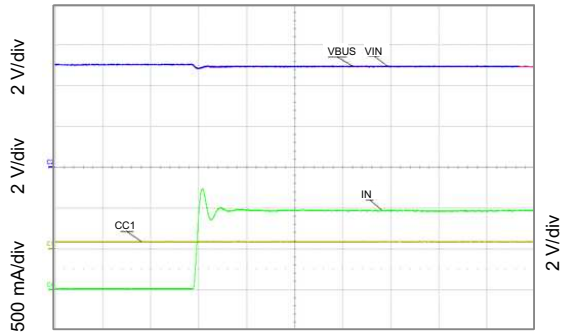
Figure 21. Basic Start-Up



Time 50 ms/div

IN1 = IN2 = AUX = EN = CHG = CHG_HI = 5 V, CC1 = Open, CC2 = Open then Rd

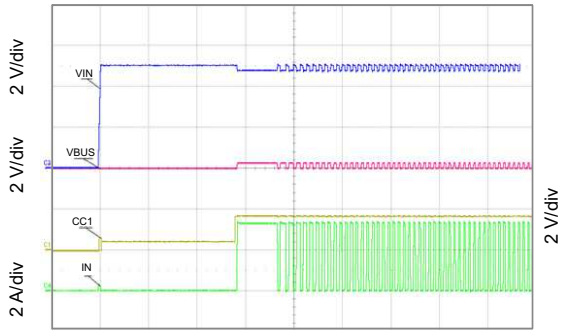
Figure 22. Start-Up



Time 200 µs/div

IN1 = IN2 = AUX = EN = 5 V; CHG = CHG_HI = 0 V, CC1 = Open, CC2 = Rd, OUT = Open→5 Ω

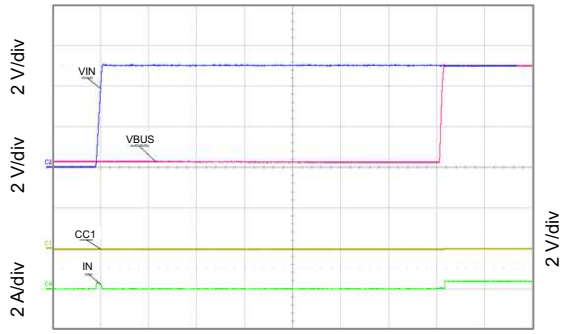
Figure 23. Load Step



Time 50 ms/div

IN1 = IN2 = AUX = EN = CHG = CHG_HI = 5 V, CC1 = Rd, CC2 = Open, OUT = Shorted

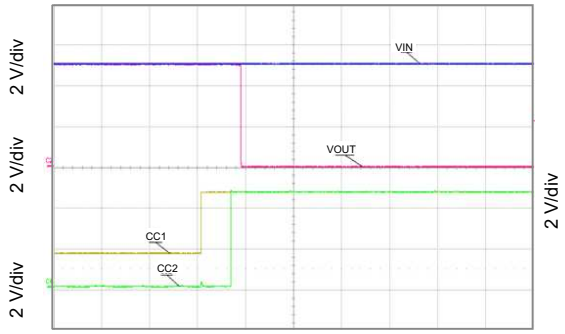
Figure 24. Hot-Plug to Short



Time 20 ms/div

IN1 = IN2 = AUX = EN = CHG = CHG_HI = 5 V, CC1 = Short, CC2 = Rd

Figure 25. Short On CC1

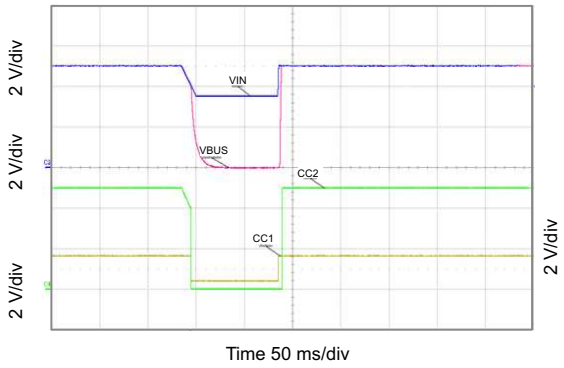


Time 20 ms/div

IN1 = IN2 = AUX = EN = CHG = CHG_HI = 5 V, CC1 = Open, CC2 = Rd→Open

Figure 26. Remove Rd

Typical Applications (continued)



V_{IN} 5 V→3.5 V (100 ms)→5 V (1 V/ms),
IN1 = IN2 = AUX = EN = CHG = CHG_HI = 5 V,
CC1 = Rd,
CC2 = Ra

Figure 27. Brown-Out Test

Typical Applications (continued)

8.2.2 Type-C DFP Port Implementation with BC 1.2 (DCP Mode) Support

Figure 28 shows a Type-C DFP implementation capable of supporting 5 V and 3 A charging in a Type-C port that is also able to support charging of legacy devices when used with a Type C – µB cable assembly for charging phones and handheld devices equipped with µB connector.

This implementation requires the use of a TPS2514A, a USB dedicated charging port (DCP) controller with auto-detect feature to charge not only BC1.2 compliant handheld devices but also popular phones and tablets that incorporate their own propriety charging algorithm. Refer to TPS2514A specifications available at www.ti.com for more details.

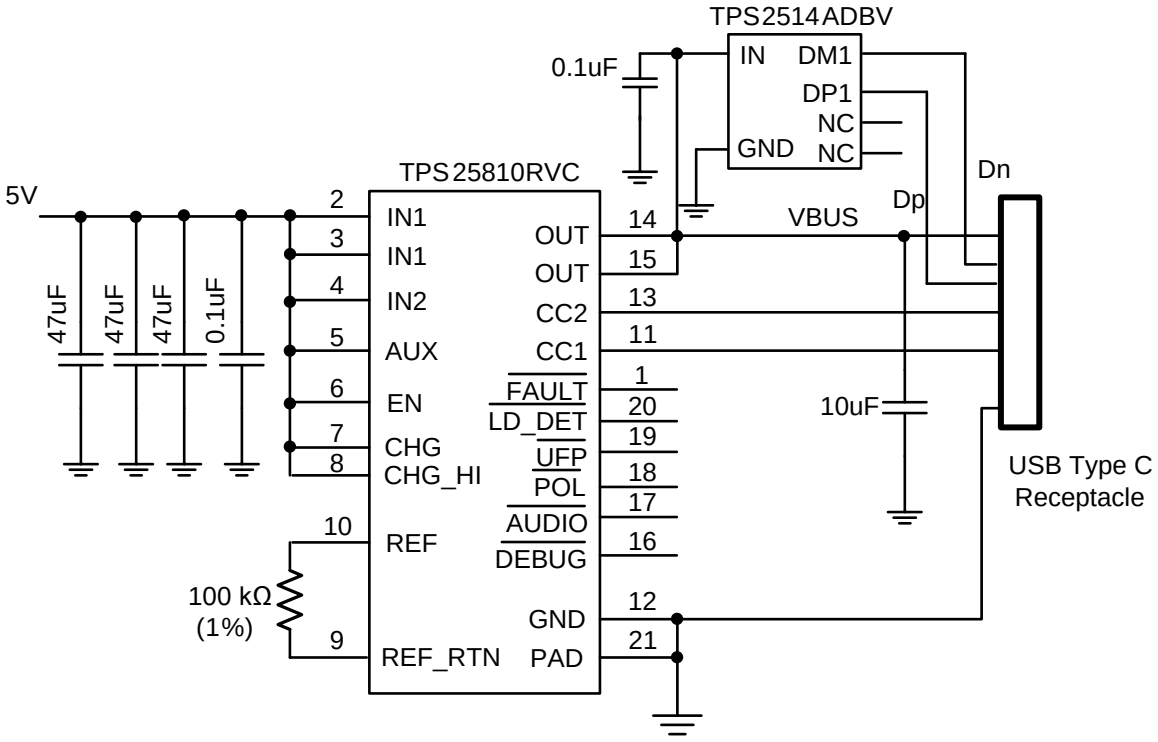


Figure 28. Type C DFP Port Implementation with BC 1.2 (DCP Mode) Support

8.2.2.1 Design Requirements

Refer to *Design Requirements* for the Design Requirements.

8.2.2.2 Detailed Design Procedure

Refer to *Detailed Design Procedure* for the Detailed Design Procedure.

8.2.2.3 Application Curves

Refer to *Application Curves* for the Application Curves.

9 Power Supply Recommendations

The device has three power supply inputs; IN1, which is directly connected to OUT via the power MOSFET, is tied to the VBUS pin in the Type-C receptacle. IN2 also has a current limiting switch and is MUXed either to the CC1 or CC2 pin in the Type-C receptacle depending on cable plug polarity. AUX is the chip supply. In most applications all three supplies are tied together. In a special implementation like power wake IN1/IN2 are tied to a single supply while AUX is powered by a supply that is always ON and can be as low as 2.9 V.

USB Specification Revisions 2.0 and 3.1 require VBUS voltage at the connector to be between 4.75 V to 5.5 V. Depending on layout and routing from supply to the connector the voltage droop on VBUS has to be tightly controlled. Locate the input supply close to the device. For all applications, a 10-µF or greater ceramic bypass capacitor between OUT and GND is recommended as close to the Type-C connector of the device as possible for local noise decoupling. The power supply should be rated higher than the current limit set to avoid voltage droops during over current and short-circuit conditions.

10 Layout

10.1 Layout Guidelines

Layout best practices as it applies to the TPS25810 are listed below.

- For all applications a 10-µF ceramic capacitor is recommended near the Type-C receptacle and another 120-µF ceramic capacitor close to IN1 pin.
  - The optimum placement of the 120-µF capacitor is closest to the IN1 and GND pins of the device.
  - Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN1 pin, and the GND pin of the IC. See Figure 29 for a PCB layout example.
- High current carrying power path connections to the device should be as short as possible and should be sized to carry at least twice the full-load current.
  - Have the input and output traces as short as possible. The most common cause of voltage drop failure in USB power delivery is the resistance associated with the VBUS trace. Trace length, maximum current being supplied for normal operation, and total resistance associated with the VBUS trace must be taken into account while budgeting for voltage drop.
  - For example, a power carrying trace that supplies 3 A, at a distance of 20 inches, 0.100-in. wide, with 2-oz. copper on the outer layer will have a total resistance of approximately 0.046 Ω and voltage drop of 0.14 V. The same trace at 0.050-in.-wide will have a total resistance of approximately 0.09 Ω and voltage drop of 0.28 V.
  - Make power traces as wide as possible.
- The resistor attached to the REF pin of the device has several requirements:
  - It is recommended to use a 1% 100-kΩ low tempco resistor.
  - It should be connected to pins REF and REF_RTN (pin 9 and pin 10 respectively).
  - The REF_RTN pin should be isolated from the GND plane. See Figure 29.
  - The trace routing between the REF and REF_RTN pins of the device should be as short as possible to reduce parasitic effects on current limit and current advertisement accuracy. These traces should not have any coupling to switching signals on the board.
- Locate all TPS25810 pull-up resistors for open-drain outputs close to their connection pin. Pull up resistors should be 100 kΩ.
  - When a particular open drain output is not used/needed in the system leave the associated pin open or tied to GND.
- Keep the CC lines close to the same length.
- Thermal Considerations:
  - When properly mounted, the thermal pad package provides significantly greater cooling ability than an ordinary package. To operate at rated power, the thermal pad must be soldered to the board GND plane directly under the device. The thermal pad is at GND potential and can be connected using multiple vias to inner layer GND. Other planes, such as the bottom side of the circuit board can be used to increase heat sinking in higher current applications. Refer to Technical Briefs: *PowerPad™ Thermally Enhanced Package* (TI literature Number SLMA002) and *PowerPAD™ Made Easy* (TI Literature Number SLMA004) or more information on using this thermal pad package.
  - The thermal via land pattern specific to the TPS25810 can be downloaded from the device web page at www.ti.com.
  - Obtaining acceptable performance with alternate layout schemes is possible; however the layout example in the following section has been shown to produce good results and is intended as a guideline.
- ESD Considerations
  - TPS25810 has built in ESD protection for CC1 and CC2. Keep trace length to a minimum from the type-C receptacle to the TPS25810 on CC1 and CC2.
  - 10-uF output cap should be placed near Type-C receptacle
  - Refer to the TPS25810EVM-745 Evaluation Module for an example of a double layer board that passes IEC61000-4-2 testing
  - Do not create stubs or test points on the CC lines. Keep the traces short if possible and use minimal via along the traces (1-2 inches or less).
  - Refer to ESD Protection Layout Guide for additional information (TI Literature Number SLVA680)

Layout Guidelines (continued)

– Have a dedicated ground plane layer if possible to avoid differential voltage buildup

10.2 Layout Example

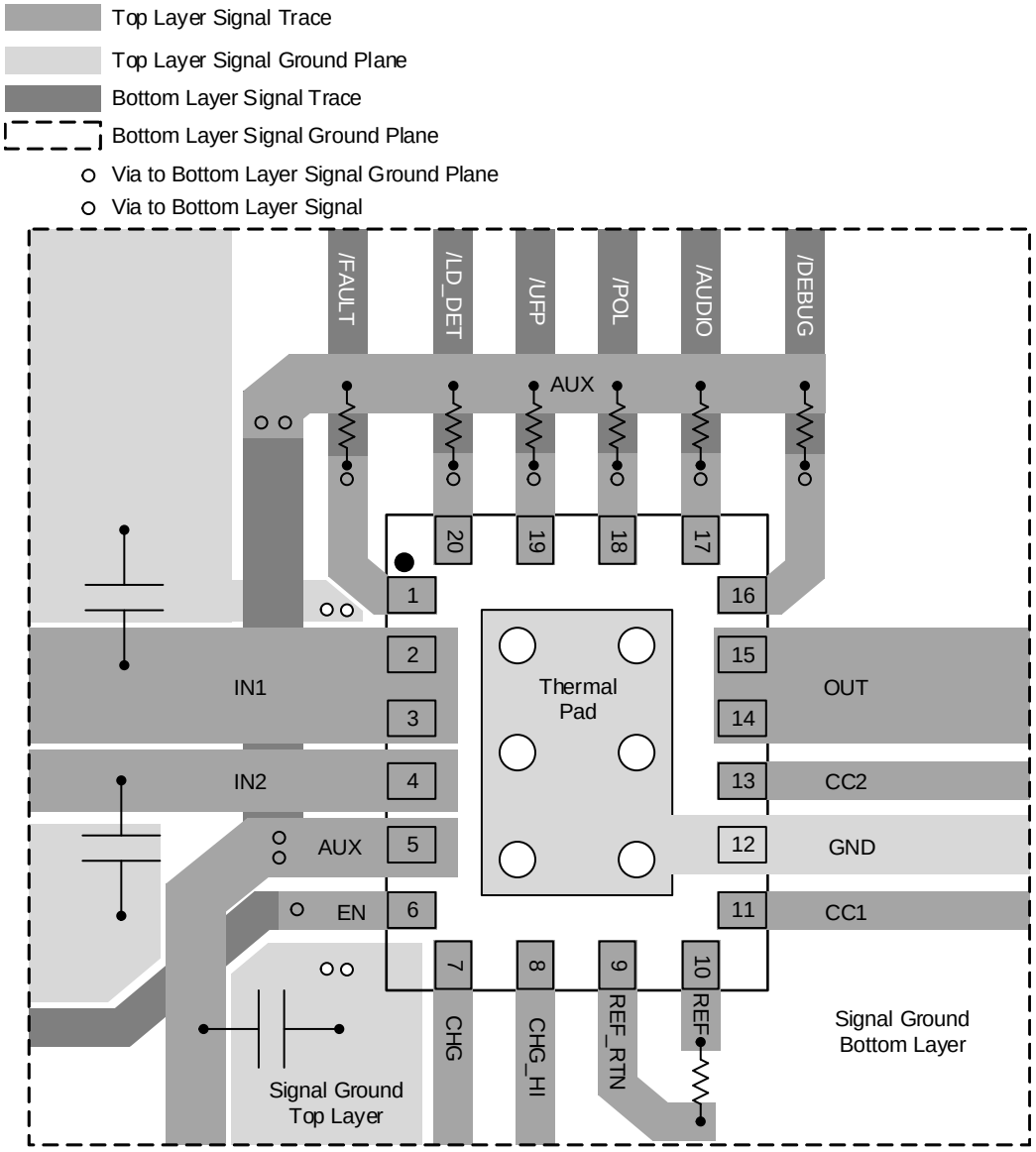


Figure 29. Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

PowerPad™ Thermally Enhanced Package (TI literature Number SLMA002)

PowerPAD™ Made Easy (TI Literature Number SLMA004)

TPS25810EVM-745 User's Guide (SLVUAI0)

Protecting the TPS25810 from High Voltage DFPs (SLVA751)

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

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11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS25810RVCR	ACTIVE	WQFN	RVC	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	25810	Samples
TPS25810RVCT	ACTIVE	WQFN	RVC	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	25810	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

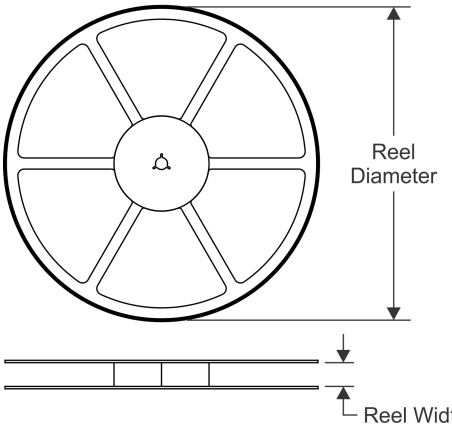
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

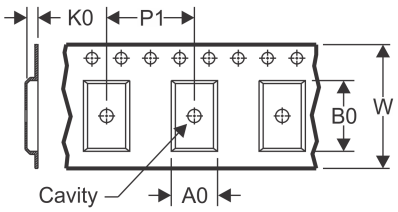
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

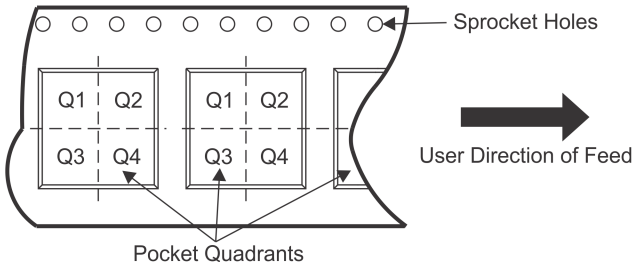


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

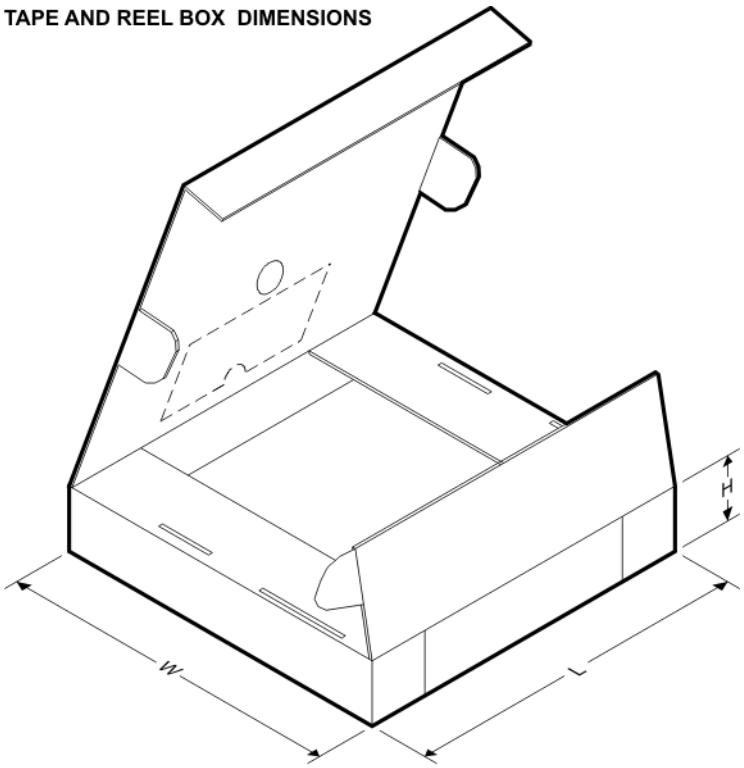
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS25810RVCR	WQFN	RVC	20	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
TPS25810RVCT	WQFN	RVC	20	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1

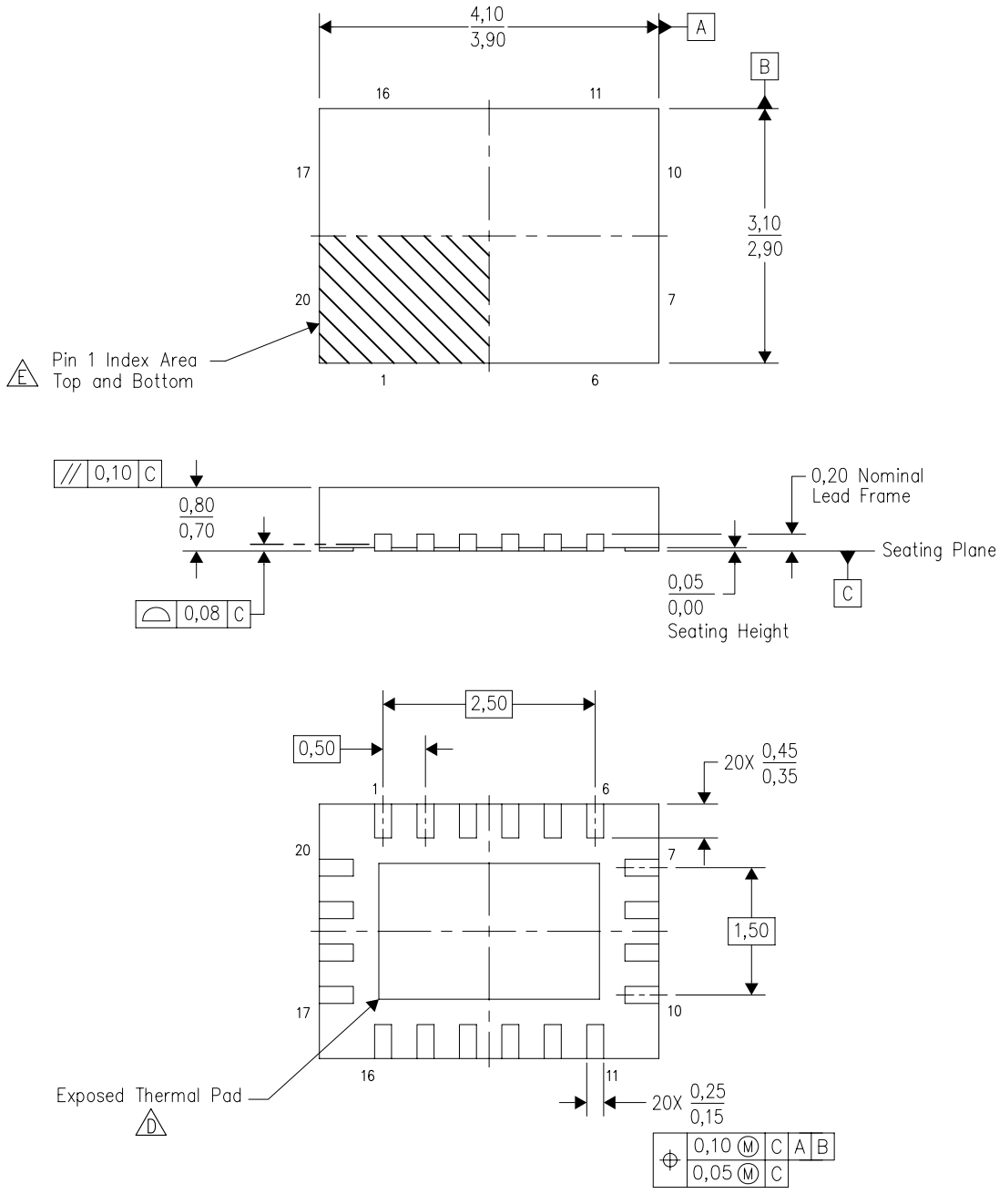
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS25810RVCR	WQFN	RVC	20	3000	367.0	367.0	35.0
TPS25810RVCT	WQFN	RVC	20	250	210.0	185.0	35.0

RVC (R–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

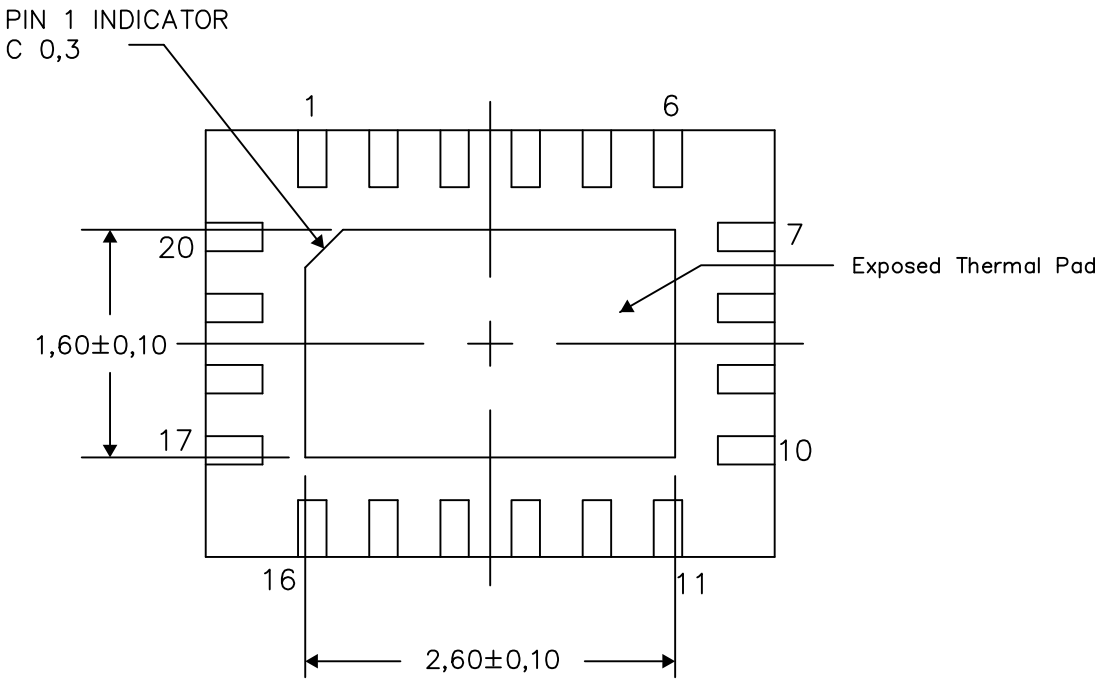
RVC (R–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4209820–2/F 03/15

NOTE: All linear dimensions are in millimeters

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