250mA Dual Outputs AMOLED Display Power Supply

Check for Samples: TPS65137AS

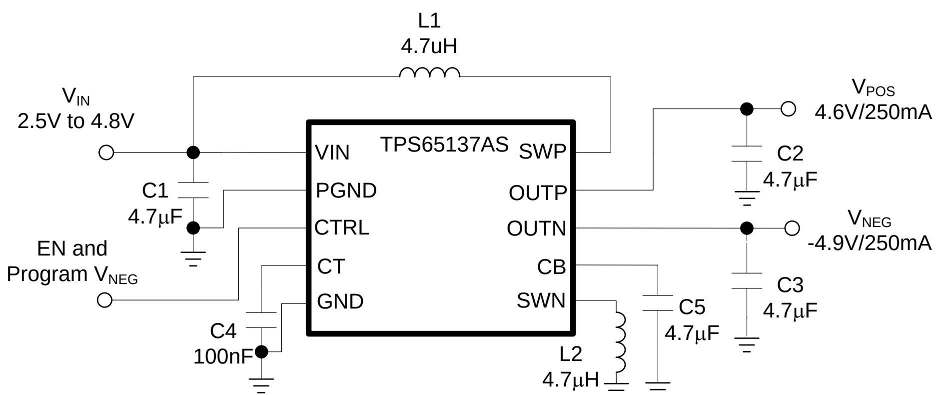
FEATURES

- **2.5 V to 4.8 V Input Voltage Range**
- **0.8% Output Voltage Accuracy V_{POS}**
- **Excellent Line Transient Regulation**
- **250 mA Output Current**
- **Fixed 4.6 V V_{POS} Output Voltage**
- **Digitally Programmable V_{NEG}, –2.2V to –5.2V**
- **–4.9V Default Value for V_{NEG}**
- **Short Circuit Protection**
- **Thermal Shutdown**
- **3mm × 3mm 10-Pin QFN Package**

APPLICATIONS

- **Active Matrix OLED**

TYPICAL APPLICATION



DESCRIPTION

The TPS65137AS is designed to drive AMOLED displays (Active Matrix Organic Light Emitting Diode) requiring positive and negative voltage supply rails. The device integrates a boost converter with LDO post regulator and an inverting buckboost converter suitable for battery operated products. The digital control pin (CTRL) allows programming the negative output voltage in digital steps. The TPS65137AS uses a novel technology enabling excellent line and load regulation. This is required to avoid disturbance of the AMOLED display by the input voltage disturbances occurring during transmit periods in mobile phones.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION (1) (2)

T_A	PACKAGE (2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	10-Pin 3x3 QFN	TPS65137ASDSCR	PPGC

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE MIN	VALUE MAX	UNIT
Pin Voltage (2)	PVIN, SWP, OUTP, CTRL, VL, CB		5.5	V
	OUTN		–6.5	V
	SWN	–6.5	5.5	V
	CT		3.6	V
ESD rating	HBM		2	kV
	MM		200	V
	CDM		500	V
T_J	Operating junction temperature range	–40	50	°C
T_A	Operating ambient temperature range	–40	85	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) With respect to GND pin.

THERMAL INFORMATION

THERMAL METRIC (1)		TPS65137AS DSC 10	UNITS
$θ_{JA}$	Junction-to-ambient thermal resistance	56.5	°C/W
$θ_{JB}$	Junction-to-board thermal resistance	25.2	
$ψ_{JT}$	Junction-to-top characterization parameter	1.0	
$ψ_{JB}$	Junction-to-board characterization parameter	17.9	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{IN}	Input supply voltage range	2.5	3.7	4.8	V
T_A	Operating ambient temperature	–40	25	85	°C
T_J	Operating junction temperature	–40	85	125	°C

ELECTRICAL CHARACTERISTICS

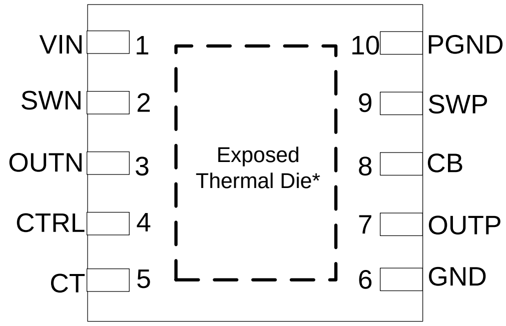
V_{IN} = 3.7V, CTRL = V_{IN}, V_{POS} = 4.6V, V_{NEG} = –4.9V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT AND THERMAL PROTECTION						
V_{IN}	Input voltage range		2.5		4.8	V
I_Q	Operating quiescent current into V_{IN}	V_{POS} and V_{NEG} have no load[(1)]		16		mA
I_{SD}	Shutdown current into V_{IN}	CTRL = GND		0.1		µA
V_{UVLO}	Under-voltage lockout threshold	V_{IN} falling			2.0	V
		V_{IN} rising			2.3	
	Thermal shutdown			145		°C
OUTPUT V_{POS}						
V_{POS}	Positive output voltage regulation		–0.8%	4.6	0.8%	V
$r_{DS(ON)}$	SWP MOSFET on-resistance	I_{SWP} = 200 mA		200		mΩ
	SWP MOSFET rectifier on-resistance	I_{SWP} = 200 mA		250		mΩ
f_{SWP}	SWP Switching frequency	I_{POS} = 0 mA		1.6		MHz
I_{SWP}	SWP switch current limit	Inductor valley current	0.9	1.2		A
$V_{P(SCP)}$	Short circuit threshold in operation	V_{POS} falling		3.7		V
I_{PLEAK}	Leakage current into V_{POS}	CTRL = GND		2	5	µA
V_{DROP}	LDO drop out voltage	I_{POS} = 100 mA		400		mV
	Line regulation	I_{POS} = 0 mA		0		%/V
	Load regulation	I_{POS} = 0 to 250 mA		0.28		%/A
OUTPUT V_{NEG}						
V_{NEG}	Negative output voltage default			–4.9		V
	Negative output voltage range		–2.2		–5.2	V
	Negative output voltage regulation	–5.2 ≤ V_{NEG} ≤ –4.2	–1%		1%	
		–4.2 < V_{NEG} ≤ –2.2	–1.5%		1.5%	
$r_{DS(ON)}$	SWN MOSFET on-resistance	I_{SWN} = 200 mA		200		mΩ
	SWN MOSFET rectifier on-resistance	I_{SWN} = 200 mA		300		
f_{SWN}	SWN switching frequency	I_{NEG} = 100 mA		1.7		MHz
I_{SWN}	SWN switch current limit	V_{IN} = 2.9 V	1.2	2.2		A
$V_{N(SCP)}$	Short circuit threshold in operation	Voltage drop from programmed V_{NEG}		420		mV
	Short circuit threshold in start-up		0.18	0.21	0.24	V
$t_{N(SCP)}$	Short circuit detection time in start-up			10		ms
I_{NLEAK}	Leakage current out of V_{NEG}	CTRL = GND		2	5	µA
$R_{N(PD)}$	V_{NEG} Pull down resistor before start up	I_{NEG} = 1 mA		300		Ω
	Line regulation			0		%/V
	Load regulation	I_{NEG} = 0 to 250 mA		0.28		%/A
CTRL INTERFACE						
V_H	Logic high-level voltage		1.2			V
V_L	Logic low-level voltage				0.4	V
R	Pull down resistor		150	400	860	kΩ
t_{INIT}	Initialization time			300	400	µs
t_{OFF}	Shutdown time period		30		80	µs
t_{HIGH}	Pulse high level time period		2	10	25	µs
t_{low}	Pulse low level time period		2	10	25	µs
t_{STORE}	Data storage/accept time period		30		80	µs
R_T	C_T pin output impedance		150	325	500	kΩ

(1) With inductor DFE252012C 4.7 µH from TOKO

DEVICE INFORMATION

10 PIN TQFN PACKAGE
(TOP VIEW

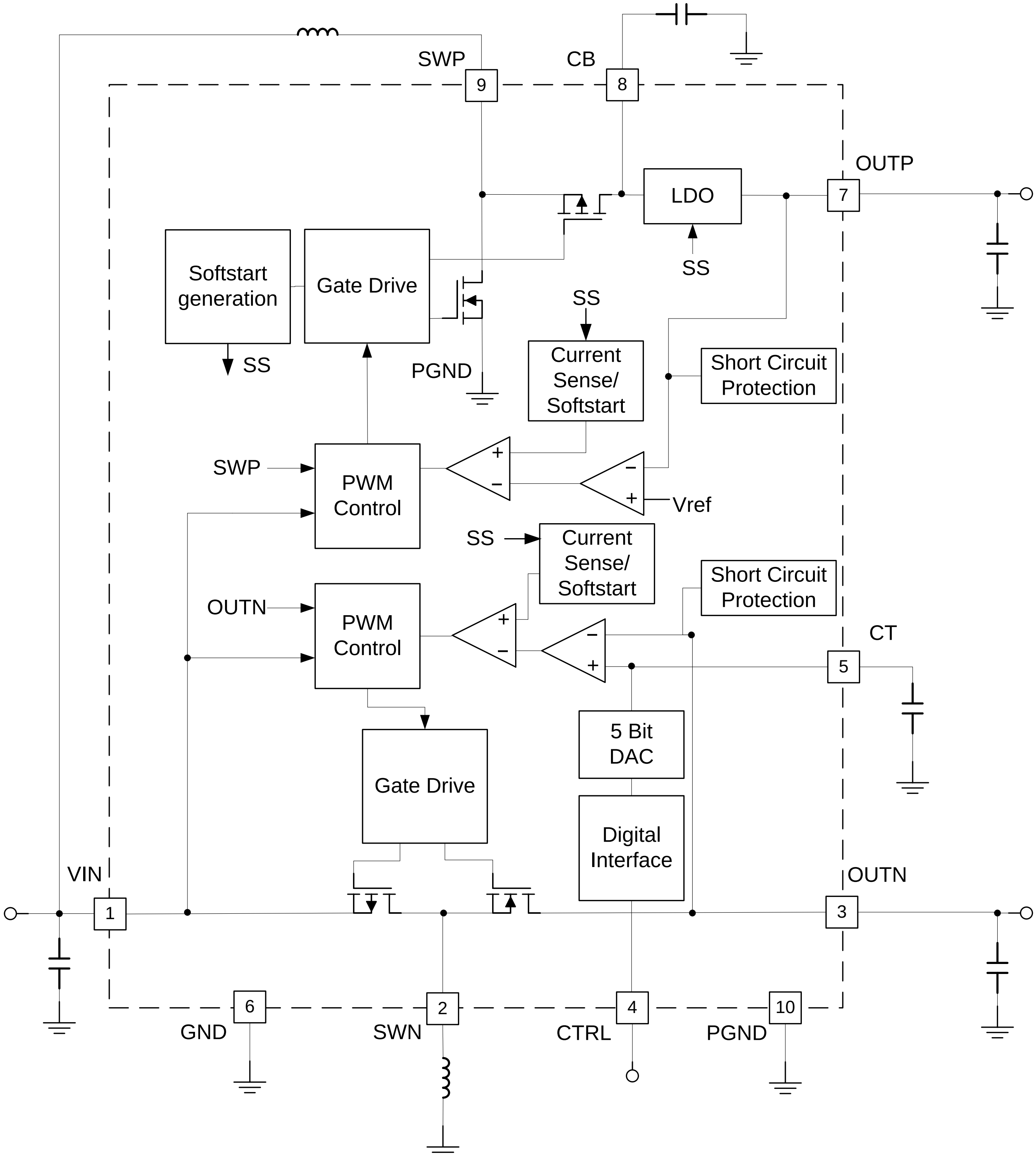


Pin Functions

PIN		I/O (1)	DESCRIPTION
NO.	NAME		
1	VIN	I	Input supply for the negative buck-boost converter generating V_{NEG}
2	SWN	I	Switch pin of the negative buck-boost converter
3	OUTN	O	Output of negative buck-boost converter
4	CTRL	I	Combined enable and V_{NEG} programming pin.
5	CT	O	Sets the settling time for the voltage on V_{NEG} when programmed to a new value
6	GND	G	Analog ground
7	OUTP	O	Output of the boost converter
8	CB	O	Internal boost converter bypass capacitor
9	SWP	I	Switch pin of the boost converter
10	PGND	G	Power ground of boost converter
Exposed thermal die		G	Connect this pad to analog GND.

(1) G = Ground, I = Input, O = Output

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

		FIGURE
Efficiency versus Output current (Output current is from V_{POS} to V_{NEG})	V_{POS} = 4.6 V, V_{NEG} = –4.9 V	Figure 1
Startup		Figure 2
Switch pins and output waveforms (Output current is from V_{POS} to V_{NEG})	I_{OUT} = 100 mA, Boost and BuckBoost	Figure 3
	I_{OUT} = 250 mA, Boost and BuckBoost	Figure 4
	I_{OUT} = 250 mA, Boost	Figure 5
	I_{OUT} = 250 mA, BuckBoost	Figure 6

EFFICIENCY vs OUTPUT CURRENT (V_{POS} 4.6V, V_{NEG} -4.9V)

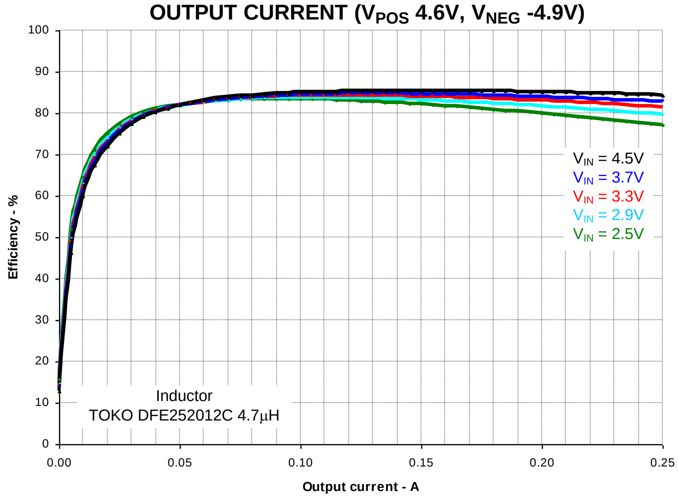


Figure 1.

STARTUP

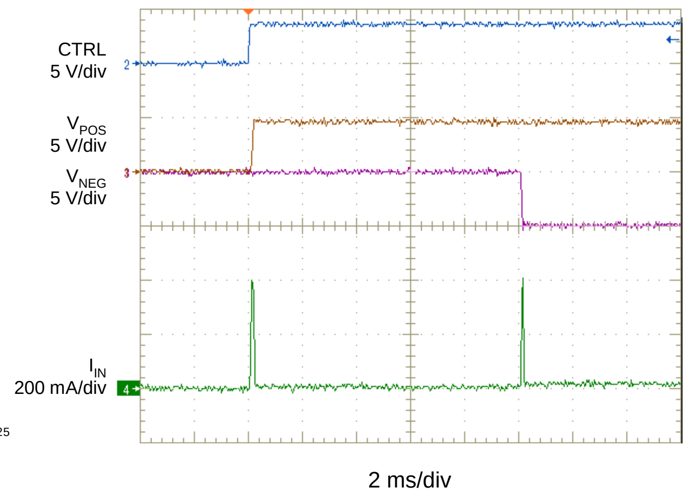


Figure 2.

SWITCH PINS AND OUTPUTS BOOST AND BUCKBOOST, I_{OUT} 100mA

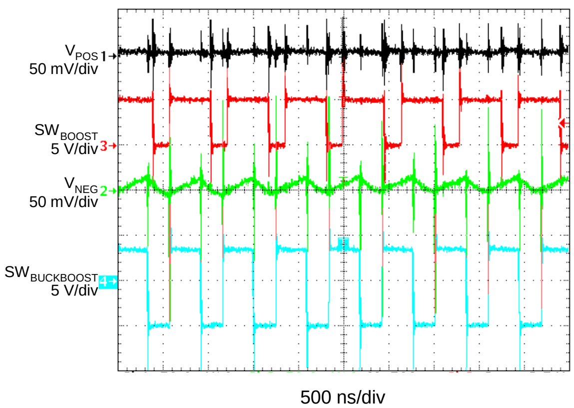


Figure 3.

SWITCH PINS AND OUTPUTS BOOST AND BUCKBOOST, I_{OUT} 250mA

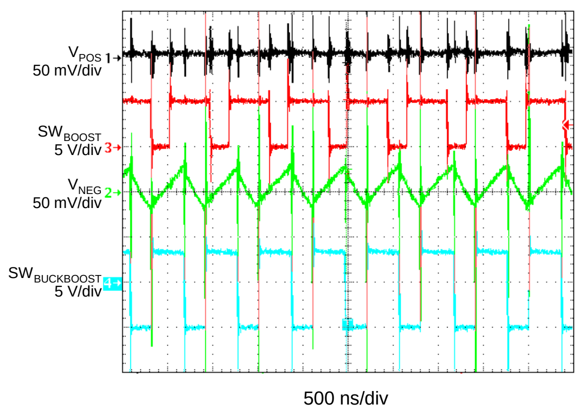


Figure 4.

SWITCH PINS AND OUTPUTS BOOST, I_{OUT} 250mA

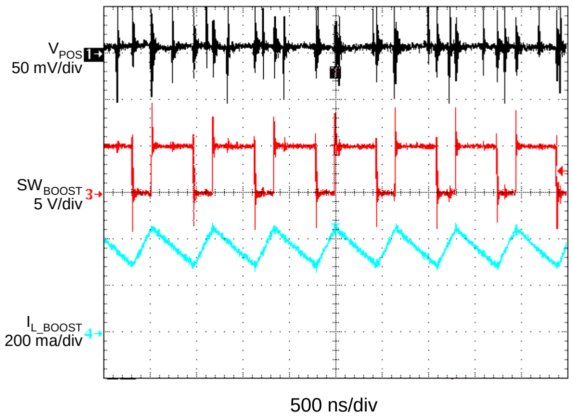


Figure 5.

SWITCH PINS AND OUTPUTS BUCKBOOST, I_{OUT} 250mA

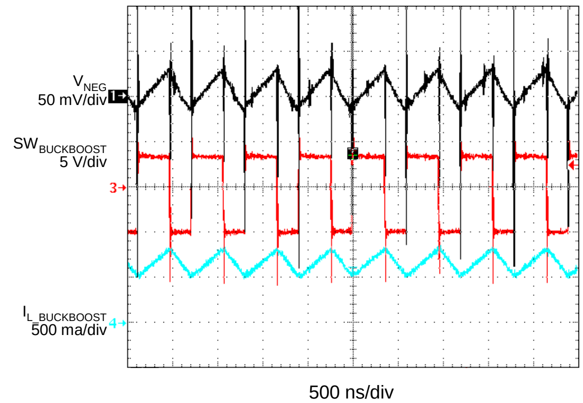


Figure 6.

APPLICATION FOR TYPICAL CHARACTERISTICS

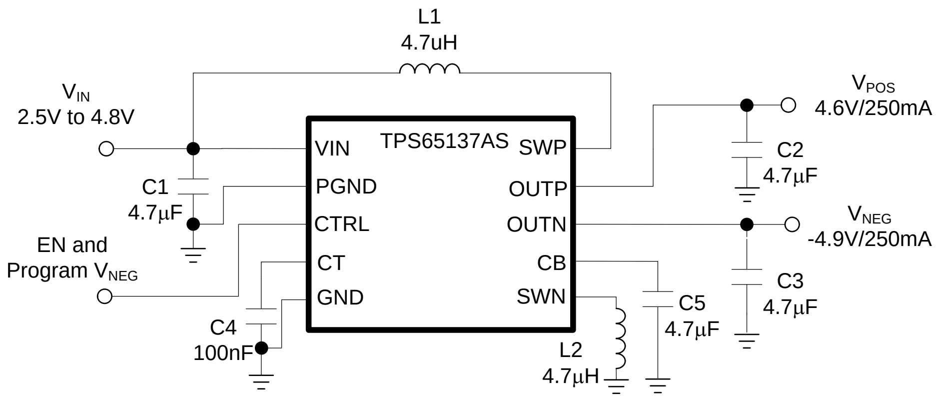


Figure 7. Application for Typical Characteristics

Table 1. Bill of Materials for Typical Characteristics

	Value	Part Number	Manufacturer
C1, C2, C3, C5	4.7 µF, X5R	GRM21BR61C475KA88	Murata
C4	100 nF, X7R	GRM21BR71E104KA01	Murata
L1, L2	4.7 µH	DFE252012C 4.7 µH	TOKO

DETAILED DESCRIPTION

The TPS65137AS consists of a boost converter using an LDO as post regulator and an inverting buck-boost converter. The positive output is fixed at 4.6V. The negative output is programmable by a digital interface in the range of –2.2V to –5.2V, the default is –4.9V. The transition time of the negative output is adjustable by the CT pin capacitor.

SOFT START and START-UP SEQUENCE

The device has a soft start to limit the in-rush current. When the device is enabled by the CTRL pin going HIGH, the boost converter starts with a reduced switch current limit. 8ms after CTRL going HIGH, the buck-boost converter starts with the default value of –4.9V. The typical start-up sequence is shown in Figure 8.

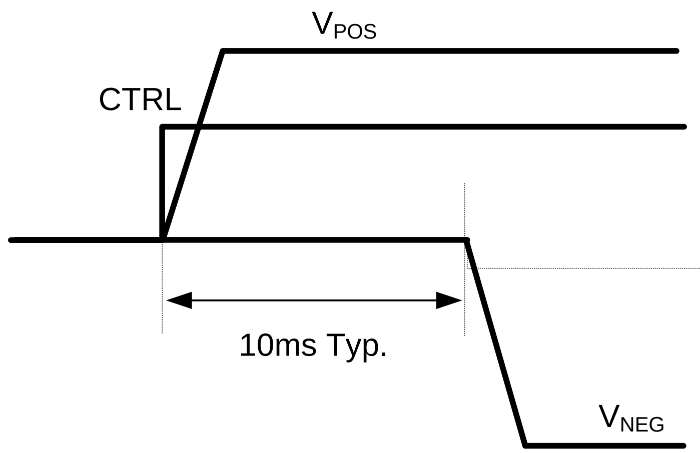


Figure 8. Start-up Sequence

SHORT CIRCUIT PROTECTION

The device is protected against short circuits of the outputs to ground and short circuit of the outputs to each other. During normal operation, an error condition is detected if V_{POS} falls below 3.7V for more than 3ms or V_{NEG} gets above 420mV above the programmed value for more than 3ms. In either case, the device goes into shutdown and this state is latched. The input and the outputs are disconnected. To resume normal operation, V_{IN} has to cycle below UVLO or CTRL has to toggle LOW and HIGH.

During start up, an error condition is detected in the following cases:

- V_{POS} is not in regulation 10ms after CTRL goes HIGH.
- V_{NEG} is higher than threshold level 10ms after CTRL goes HIGH.
- V_{NEG} is not in regulation 20ms after CTRL goes HIGH.

In the above cases, the device goes into shutdown and this state is latched. The input and the outputs are disconnected. To resume normal operation, VIN has to cycle below UVLO or CTRL has to toggle LOW and HIGH.

ENABLE (CTRL PIN)

The CTRL pin serves two functions. One is to enable and disable the device the other is the output voltage programming of the device. If the digital interface is not required the CTRL pin can be used as a standard enable pin for the device and the device will come up with its default value on V_{NEG} of –4.9V. When CTRL is pulled high, the device is enabled. The device is shut down with CTRL low.

DIGITAL INTERFACE (CTRL)

The digital interface allows programming the negative output voltage V_{NEG} in digital steps. If the digital output voltage setting is not required then the CTRL pin can also be used as a standard enable pin.

The digital output voltage programming of V_{NEG} is implemented by a simple digital interface with the timing shown in Figure 9.

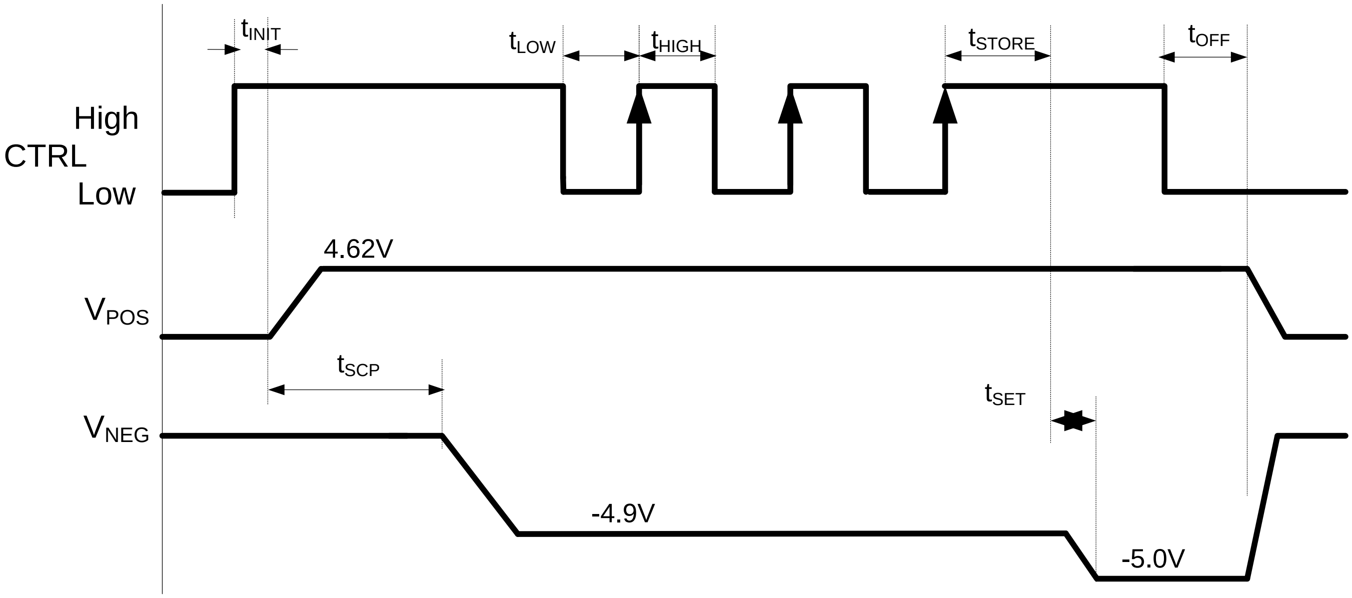


Figure 9. Digital Interface Using CTRL

Once CTRL is pulled high the device will come up with its default voltage of –4.9V. The device has a 6-bit DAC implemented with the corresponding output voltages as given in the table below. The interface counts now the rising edges applied to the CTRL pin once the device is enabled. For the example above, V_{NEG} is programmed to –5.0V since 3 rising edges are detected. Other output voltages can be programmed according Table 2.

Table 2. Programming Table for V_{NEG}

BIT/RISING EDGES	V_{NEG}	DAC VALUE	BIT/RISING EDGES	V_{NEG}	DAC VALUE
0/ no pulse	–4.9 V	00000	16	–3.7 V	10000
1	–5.2 V	00001	17	–3.6 V	10001
2	–5.1 V	00010	18	–3.5 V	10010
3	–5.0 V	00011	19	–3.4 V	10011
4	–4.9 V	00100	20	–3.3 V	10100
5	–4.8 V	00101	21	–3.2 V	10101
6	–4.7 V	00110	22	–3.1 V	10110
7	–4.6 V	00111	23	–3.0 V	10111
8	–4.5 V	01000	24	–2.9 V	11000
9	–4.4 V	01001	25	–2.8 V	11001
10	–4.3 V	01010	26	–2.7 V	11010
11	–4.2 V	01011	27	–2.6 V	11011
12	–4.1 V	01100	28	–2.5 V	11100
13	–4.0 V	01101	29	–2.4 V	11101
14	–3.9 V	01110	30	–2.3 V	11110
15	–3.8 V	01111	31	–2.2 V	11111

SETTING TRANSITION TIME t_{set} for V_{NEG} (C_T)

The device allows setting the transition time t_{set} using an external capacitor connected to pin CT. The transition time is the time period required to move V_{NEG} from one voltage level to the next programmed voltage level. The capacitor connected to pin CT does not influence the soft start time t_{ss} of the V_{NEG} default value. When the CT pin is left open then the shortest possible transition time is programmed. When connecting a capacitor to the CT pin then the transition time is given by an R-C time constant. This is given by the output impedance of the CT pin typically 325kΩ and the external capacitance. Within one τ the output voltage V_{NEG} has reached 70% of its programmed value. An example is given when using 100nF for C_T.

$$\tau \approx t_{set70\%} = 325\ k\Omega \times C_T = 325\ k\Omega \times 100\ nF = 32.5\ mS$$

The output voltage is almost at its programmed value after 3τ.

PCB LAYOUT

Figure 10 and Figure 11 show an example of a PCB layout design.

1. Place the input capacitor on VIN and the output capacitor on OUTN as close as possible to the device.
   Use short and wide traces to connect the input capacitor to VIN and the output capacitor to OUTN.
2. Place the output capacitor on OUTP and the capacitor on CB as close as possible to the device.
   Use short and wide traces to connect the output capacitor to OUTP.
3. Connect the ground of the CT capacitor to the GND pin, pin 6, directly.
4. Connect the input ground and the output ground on the same board layer, not through vias.

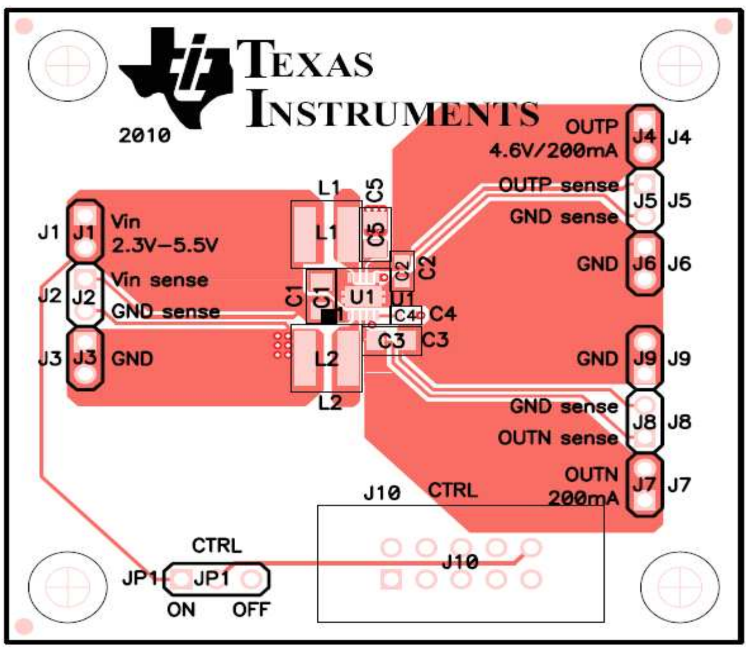


Figure 10. Example of PCB Layout Design (Top layer)

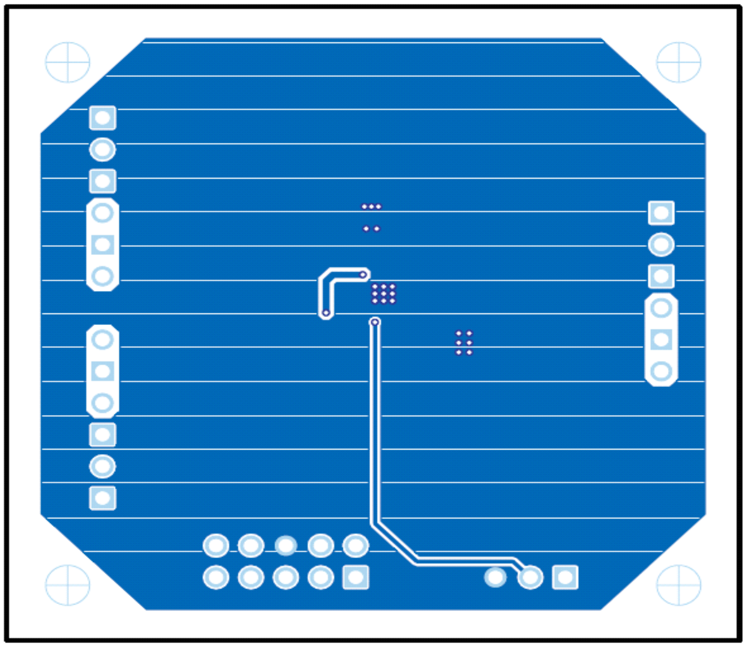


Figure 11. Example of PCB Layout Design (Bottom layer)

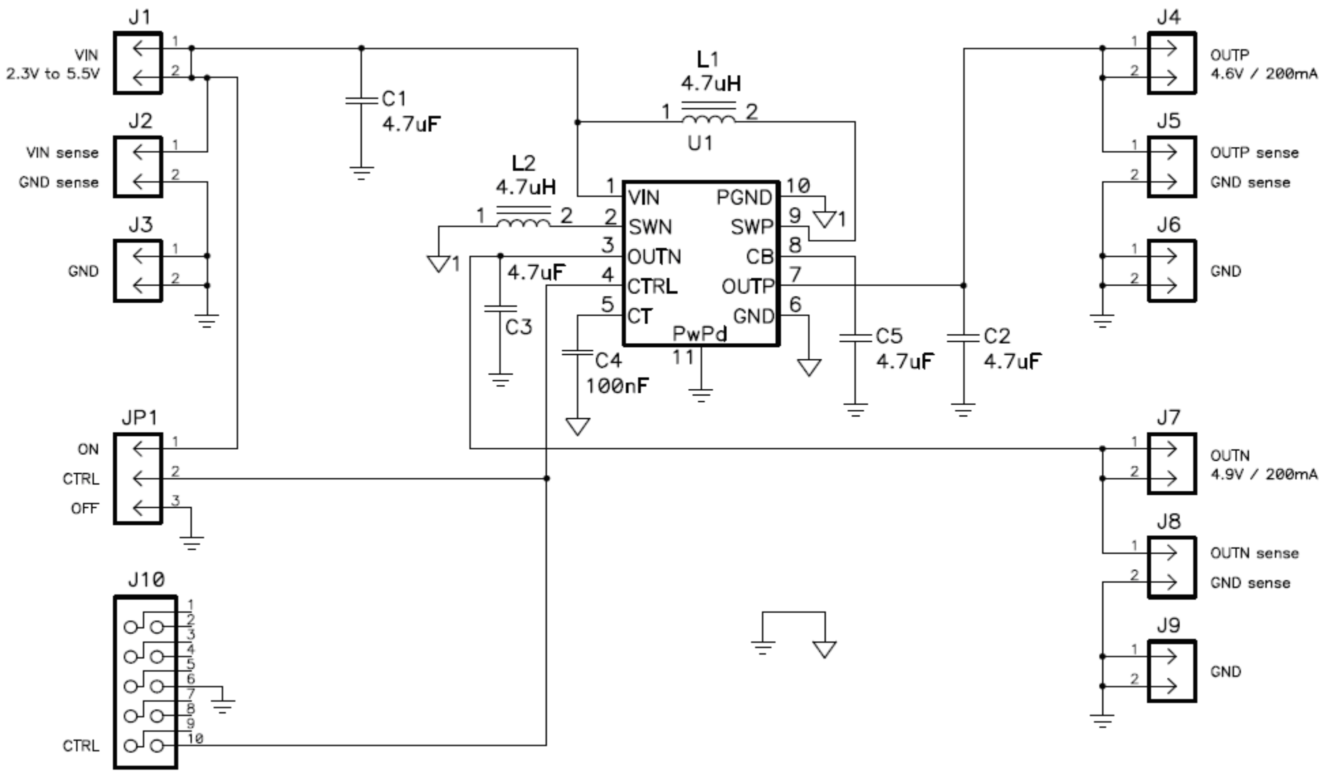


Figure 12. Schematic for the Example of PCB Layout Design

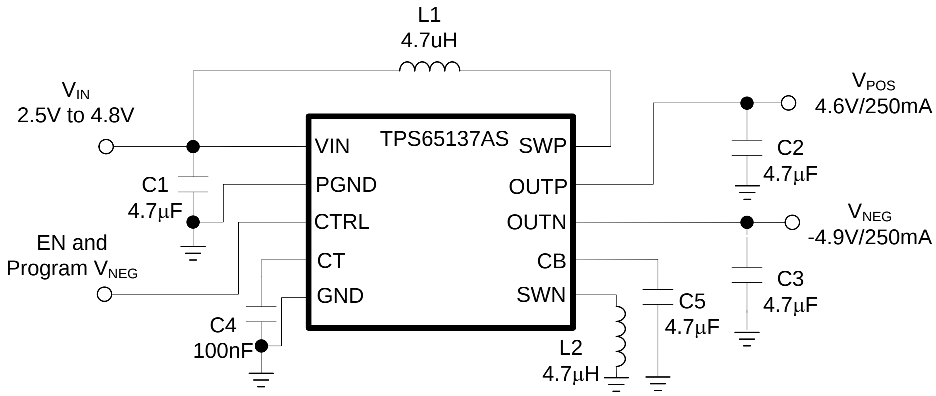


Figure 13. Typical Application Circuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65137ASDSCR	ACTIVE	WSON	DSC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PPGC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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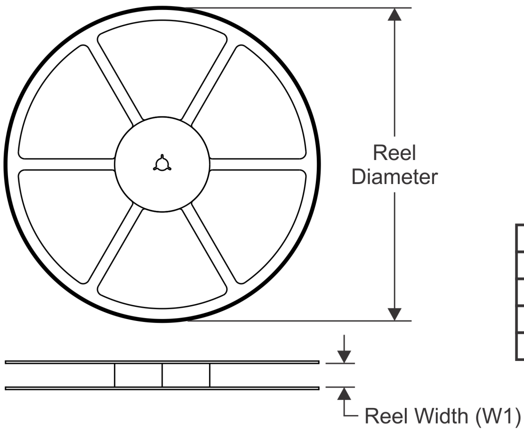
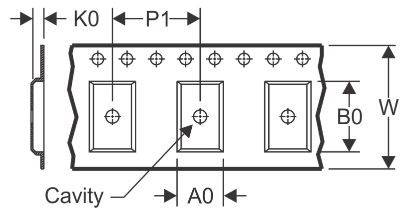
TAPE AND REEL INFORMATION

REEL DIMENSIONS

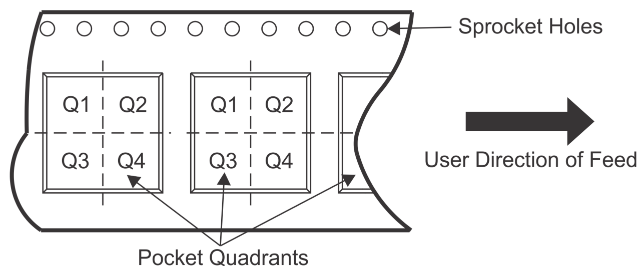


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

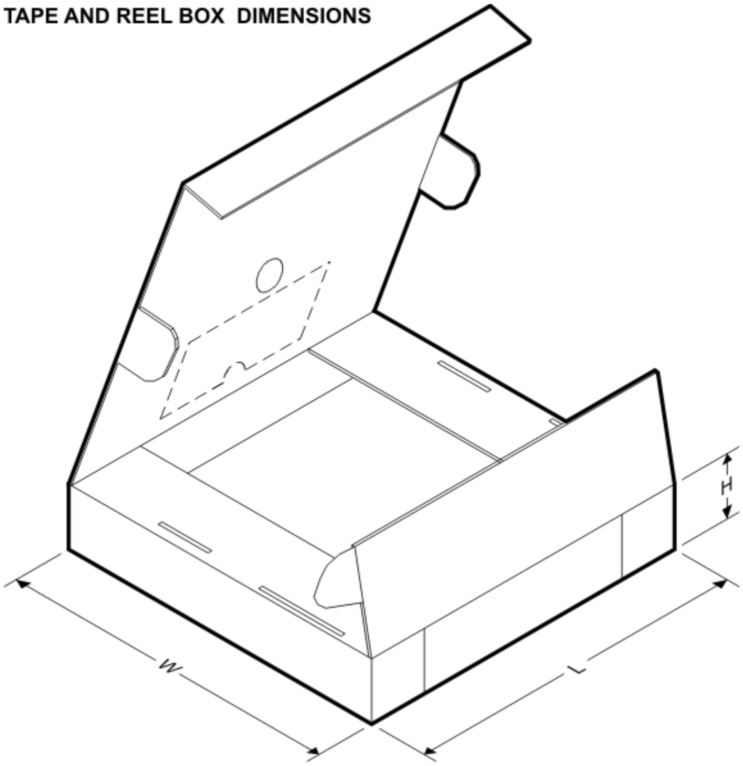
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65137ASDSCR	WSON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS65137ASDSCR	WSON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

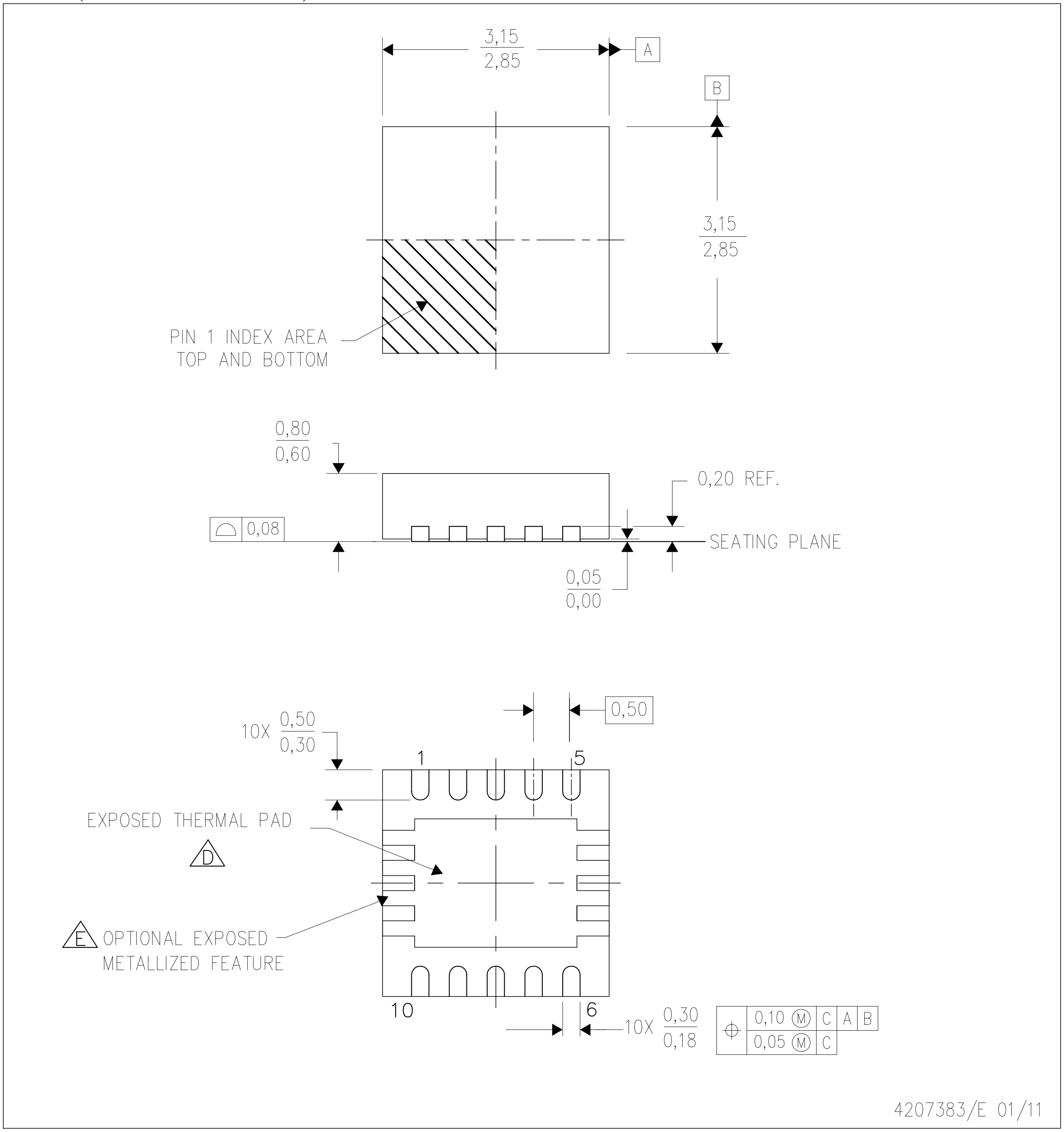
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65137ASDSCR	WSON	DSC	10	3000	552.0	367.0	36.0
TPS65137ASDSCR	WSON	DSC	10	3000	367.0	367.0	35.0

DSC (S-PWSON-N10) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Small Outline No-Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

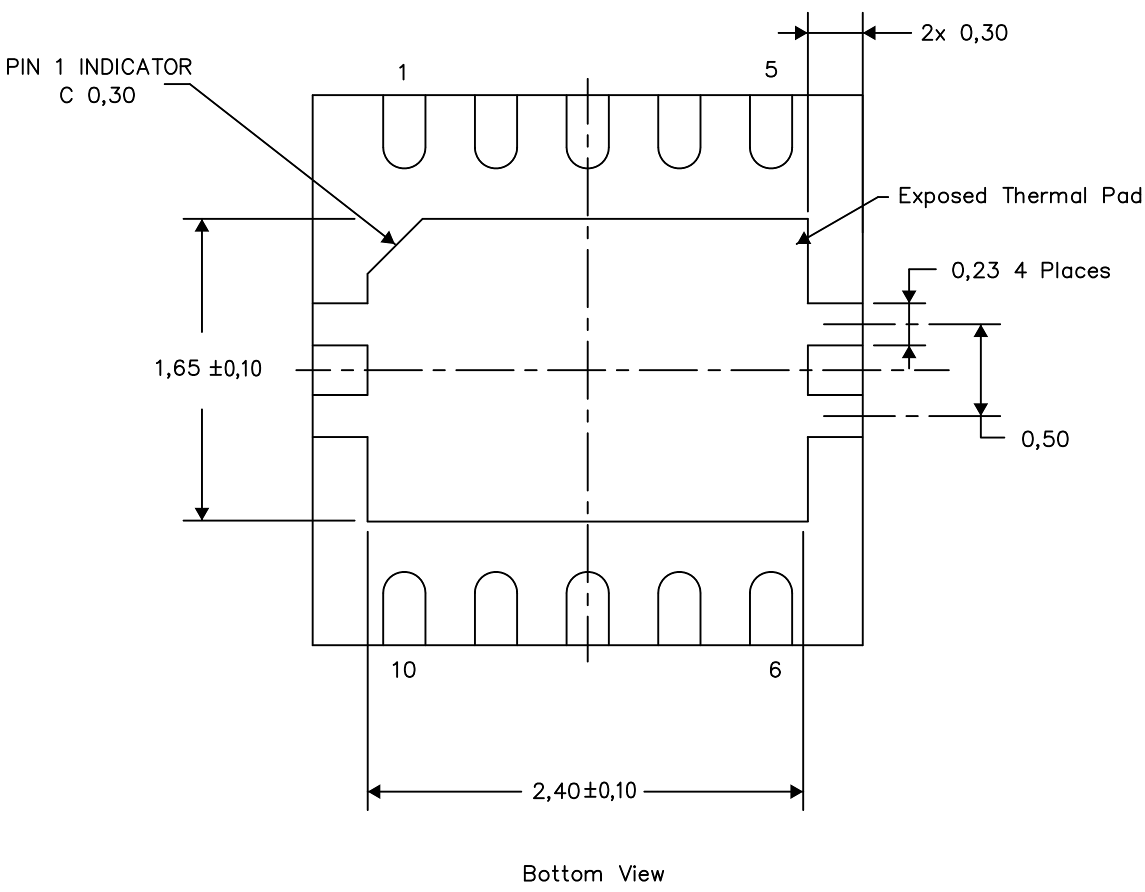
DSC (S-PWSON-N10) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4210391-2/M 08/13

NOTE: A. All linear dimensions are in millimeters

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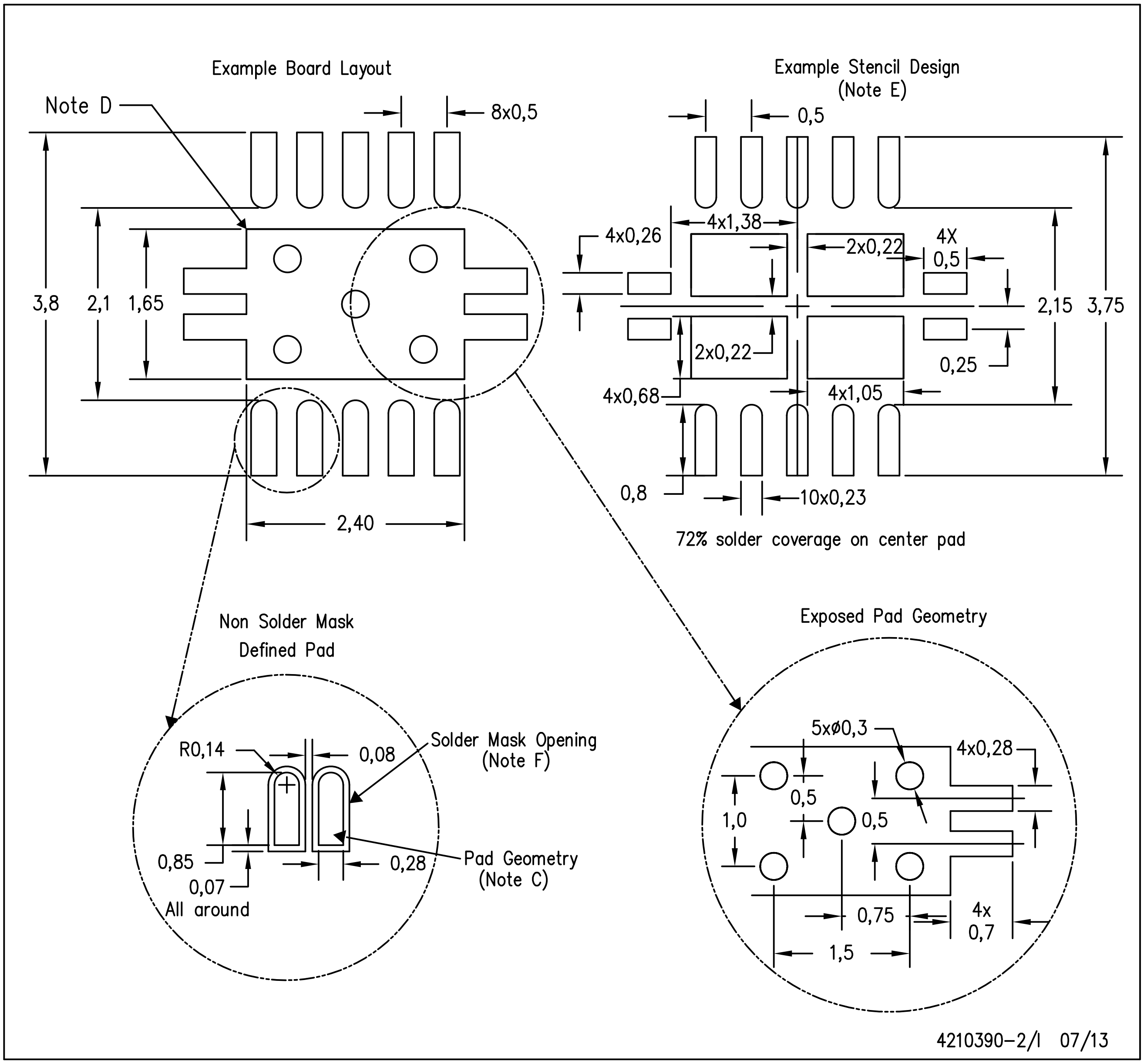

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

IMPORTANT NOTICE

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