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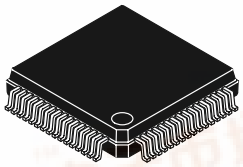
Configurable Motor Driver IC with Power Supplies

34921

MOTOR DRIVERS & POWER SUPPLIES



AE SUFFIX (Pb FREE)
98ARH98426A
64-LEAD LQFP-EP

The 34921 power IC integrates multiple motor drivers, multiple power regulators, and most other analog functions a small consumer motion-enabled product needs. The 34921's circuitry is fully protected with current limiting, short-circuit shutdown, over-temperature, over-voltage, and under-voltage detection. Supervisory functions can be read and programmed through a 8-MHz Serial Interface.

A 5.0 V dual-mode (linear or switching) voltage regulator, 3.3 V switching buck regulator, and a voltage-selectable (1.5 V, 1.8 V, 2.5 V) linear regulator provide power management. Two H-Bridges and a configurable motor driver are provided for controlling two dc motors and one unipolar stepper motor.

The highly integrated 34921 brings together sensing, communication, power management, system protection, and motor control in one device.

Features

- Two Functionally Identical Pulse-Width Modulated (PWM) DC Motor Drivers
- One Switching, One Linear, and One Dual-Mode Regulator
- Dual Mode Switching/Linear 5.0 V Regulator
- Supervisory Functions (Power-ON Reset and Error Reset Circuitry)
- 8-Channel, 8-Bit Analog-to-Digital Converter (ADC)
- Charge Pump for High-Side MOSFET Drive
- Complete Support for Analog Quadrature Encoder
- Pb Free package is designated by suffix AE

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC34921AE/R2	0°C to 70°C	64 LQFP-EP

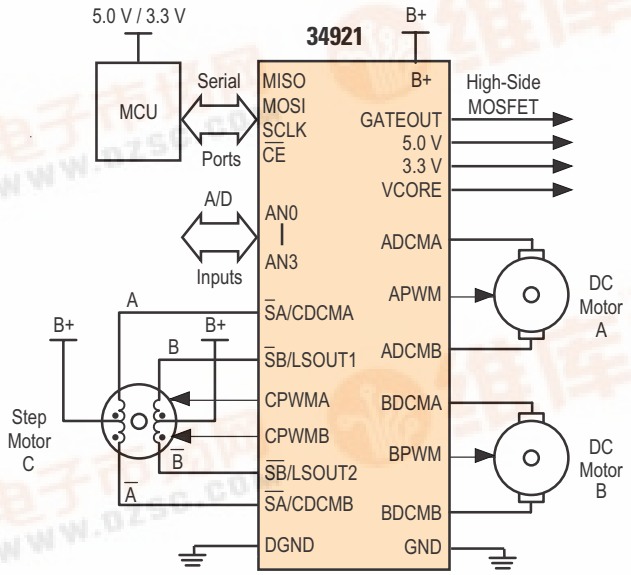


Figure 1. 34921 Simplified Application Diagram

ADVANCE INFORMATION*

*This document contains information on a product under development.
Specifications and information herein are subject to change without notice.

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INTERNAL BLOCK DIAGRAM

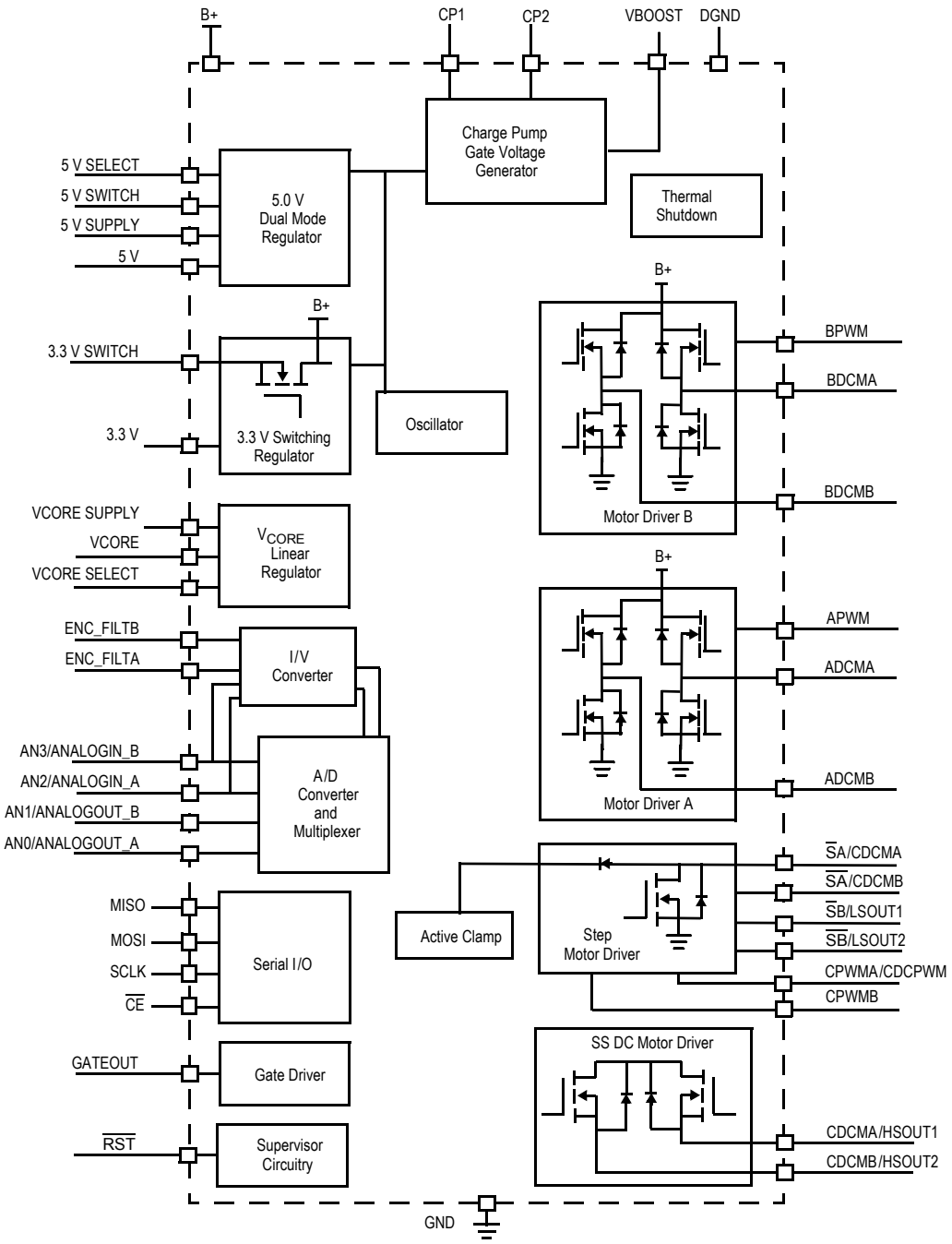


Figure 2. 34921 Simplified Internal Block Diagram

TERMINAL CONNECTIONS

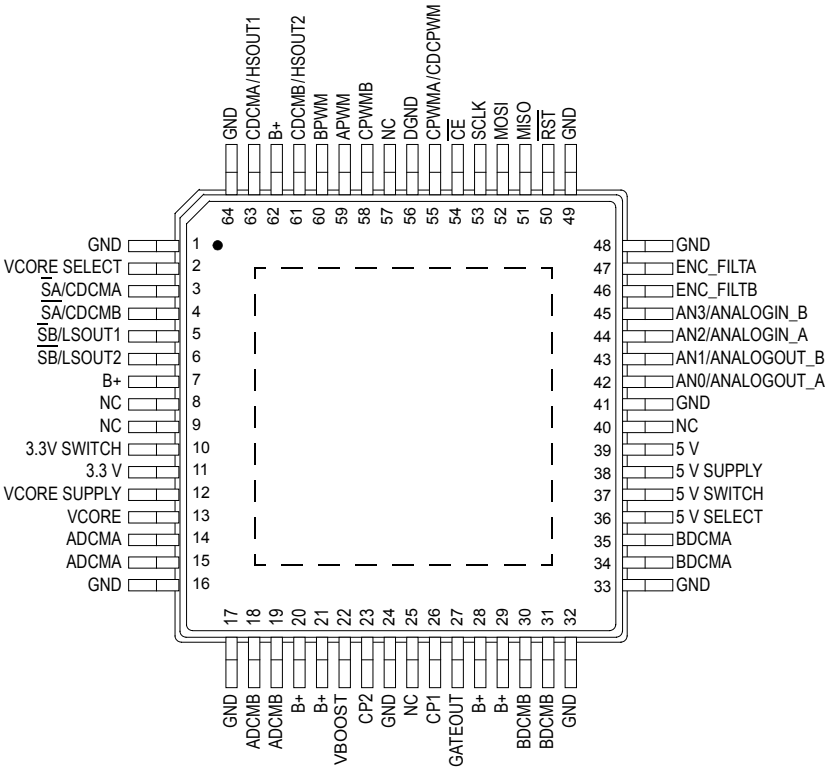


Figure 3. Terminal Function Description

Table 1. Terminal Function Description

A functional description of each terminal can be found in the Functional Terminal Description section beginning on page 18

Terminal	Terminal Name	Formal Name	Definition
1, 16, 17, 24, 32, 33, 41, 48, 49, 64	GND	Ground	Ground.
2	VCORE SELECT	Core Voltage Output Select	Core voltage regulator output voltage select.
3	$\overline{S}$A/CDCMA	Unipolar Step A/ DC Motor C Output A	Step Motor Output A or DC Motor C Output A.
4	$\overline{SA}$/CDCMB	Unipolar Step $\overline{A}$/ DC Motor C Output B	Step Motor Output $\overline{A}$ or DC Motor C Output B.
5	$\overline{S}$B/LSOUT1	Unipolar Step B/ Low-Side 1	Step Motor Output B or Low-Side Output 1.
6	$\overline{SB}$/LSOUT2	Unipolar Step $\overline{B}$/ Low-Side 2	Step Motor Output $\overline{B}$ or Low-Side Output 2.
7, 20, 21, 28, 29, 62	B+	Power Supply Input	Motor and regulator input voltage.
8, 9, 25, 40, 57	NC	No Connect	No internal connection to this terminal.

Table 1. Terminal Function Description (continued)

A functional description of each terminal can be found in the Functional Terminal Description section beginning on page 18

Terminal	Terminal Name	Formal Name	Definition
10	3.3 V SWITCH	3.3 V Switching Regulator Switch Output	3.3 V regulator switching output.
11	3.3 V	3.3 V Regulator Feedback	Feedback terminal for 3.3 V switching regulator and internal logic supply.
12	VCORE SUPPLY	Core Voltage Regulator Input	Core regulator input supply.
13	VCORE	Core Voltage Regulator Output	Core regulator output voltage.
14, 15	ADCMA	DC Motor A Output A	DC motor driver A output A.
18, 19	ADCMB	DC Motor A Output B	DC motor driver A output B.
22	VBOOST	Boost Voltage	Boost voltage storage node.
23	CP2	Switching Capacitor 2	Charge pump capacitor connection 2.
26	CP1	Switching Capacitor 1	Charge pump capacitor connection 1.
27	GATEOUT	High-Side MOSFET Gate Driver	Gate driver for external N-channel switch.
30, 31	BDCMB	DC Motor B Output B	DC motor driver B output B.
34, 35	BDCMA	DC Motor B Output A	DC motor driver B output A.
36	5 V SELECT	5.0 V Regulator Mode Select	5.0 V regulator operating mode select.
37	5 V SWITCH	5.0 V Switching Regulator Switch Output	5.0 V switching regulator switching output.
38	5 V SUPPLY	5.0 V Regulator Input Supply	5.0 V regulator input voltage.
39	5 V	5.0 V Regulator Feedback	5.0 V regulator feedback.
42	AN0/ANALOGOUT_A	AN0/Analogout_A	A/D input 0 or analog encoder output A.
43	AN1/ANALOGOUT_B	AN1/Analogout_B	A/D input 1 or analog encoder output B.
44	AN2/ANALOGIN_A	AN2/Analogin_A	A/D input 2 or analog encoder input A.
45	AN3/ANALOGIN_B	AN3/Analogin_B	A/D input 3 or analog encoder input B.
46	ENC_FILTB	Analog Encoder Channel B Filter	I/V amplifier channel B filter.
47	ENC_FILTA	Analog Encoder Channel A Filter	I/V amplifier channel A filter.
50	$\overline{\text{RST}}$	Reset	Reset input and output.
51	MISO	Master In Slave Out	Serial data out to MCU.
52	MOSI	Master Out Slave In	Serial data in from MCU.
53	SCLK	Serial Clock	Serial data clock.

Table 1. Terminal Function Description (continued)

A functional description of each terminal can be found in the Functional Terminal Description section beginning on page 18

Terminal	Terminal Name	Formal Name	Definition
54	$\overline{CE}$	Chip Enable	Serial data strobe.
55	CPWMA/CDCPWM	Motor Driver C PWM Input A	Step motor driver Phase A PWM or DC motor driver PWM.
56	DGND	Digital Ground	Digital ground.
58	CPWMB	Motor Driver C PWM Input B	Step motor driver Phase B PWM.
59	APWM	Motor Driver A PWM Input	PWM input for DC motor driver A.
60	BPWM	Motor Driver B PWM Input	PWM input for DC motor driver B.
61	CDCMB/HSOUT2	Motor Driver C DC Motor Output or High-Side Output 2	Step motor driver C output or high-side output 2.
63	CDCMA/HSOUT1	Motor Driver C DC Motor Output or High-Side Output 1	Step motor driver C output or high-side output 1.

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Max	Unit
ELECTRICAL Ratings			
Input Power Supply Voltage I_{B+} = 0.0 A	B+	-0.3 to 38	V
Logic Input Voltage	V_{IN}	-0.3 to $V_{5.0}$+0.3	V
Boost Supply Voltage	V_{BOOST}	B^+ +15	V
Input Power Supply Ripple Voltage Ripple Voltage Measured at < 20 MHz	$V_{RIPPLEB}$	400	mV_{PP}
Motor Drivers A & B Maximum Output Voltage	V_{OUTMAX}	40	V
5.0 V Linear Regulator Maximum Output Voltage Startup	$V_{5.0}$	5.4	V
5.0 V Switching Regulator Maximum Output Voltage Startup	$V_{5.0}$	5.4	V
3.3 V Switching Regulator Maximum Output Voltage Startup	$V_{3.3}$	3.6	V
VCORE Linear Regulator Maximum Output Voltage I_{CORE} = 0.0 A	V_{CORE}	V_{CORE_NOM} +10%	V
Motor Drivers A, B, and C (Motor Driver C Configured as Step Motor Driver)[1] Motor Driver A Sink or Source Current Motor Driver B Sink or Source Current Motor Driver C Sink or Source Current	 $I_{PWM}(A)$ $I_{PWM}(B)$ $I_{PWM}(C)$	 ±4.5 ±4.5 ±1.5	A
Motor Driver C in Step Mode Step Motor Output Current Output x or $\overline{x}$ On	I_{STEP}	2.0	A
Motor Driver C in Step Mode Standoff Voltage Output Off, I_{DSS} = 10 mA	V_{BVDS}	60	V
ESD Voltage[2] Non-Operating, Unbiased, Human Body Model Machine Model Charge Device Model	V_{ESD}	 ±2000 ±200 ±250	V

Notes

1. B+ = 34 V, Motor Stalled and Saturated
2. ESD testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω), and the Charge Device Model.

Table 2. Maximum Ratings(continued)

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Max	Unit
THERMAL RATINGS			
Operating Temperature Ambient Junction	 T_A T_J	 -20 to 85 150	°C
Storage Temperature	T_{STG}	-55 to 150	°C
Thermal Resistance Junction to Ambient[3] Junction to Board[4] Junction to Case	 $R_{\theta JA}$ $R_{\theta JB}$ $R_{\theta JC}$	 40 14 <1.0	°C/W
Peak Package Reflow Temperature During Solder Mounting [5]	T_{SOLDER}	245	°C
THERMAL RESISTANCE AND PACKAGE DISSIPATION RATINGS			
Power Dissipation (T_A = 25° C) [6]	P_D	2.0	W

Notes

3. 1s PCB test board JESD51-2 and SEMI G38-87.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured at the package center lead foot. 2s2p test board, exposed pad soldered to PCB.
5. Terminal soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
6. Maximum power dissipation at indicated ambient temperature in free air with no heatsink used.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 16 V ≤ B+ ≤ 34 V, 0°C ≤ T_A ≤ 70°C, and 0°C ≤ T_J ≤ 100°C unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Serial Interfaces (MISO, MOSI, SCLK, $\overline{CE}$)					
Input Low Voltage from MCU $V_{5.0}$ = 5.0 V, $V_{3.3}$ = 3.3 V, I_{IN} ≤200 µA, V_{IN} Falling	V_{IL}	1.1	1.35	2.2	V
Input High Voltage $V_{5.0}$ = 5.0 V, $V_{3.3}$ = 3.3 V, I_{IN} ≤200 µA, V_{IN} Rising	V_{IH}	1.1	2.00	2.2	V
Input Hysteresis $V_{5.0}$ = 5.0 V, $V_{3.3}$ = 3.3 V	V_{HYS}	0.4	0.6	1.5	V
Output High-Level, MISO ($V_{5.0}$ = 5.0 V, $V_{3.3}$ = 3.3 V) I_{OUT} = 150 µA I_{OUT} = 20 µA	V_{OH}(MISO)	2.4 $V_{3.3}$-0.1	$V_{3.3}$-25 mV $V_{3.3}$-10 mV	$V_{3.3}$ $V_{3.3}$	V
Output Low-Level, MISO ($V_{5.0}$ = 5.0 V, $V_{3.3}$ = 3.3 V) I_{OUT} ≤ 20 µA I_{OUT} ≤ 150 µA	V_{OL}(MISO)	0.0 0.0	10 25	100 400	mV
Input Pulldown Current $V_{5.0}$ = 5.0 V, $V_{3.3}$ = 3.3 V, V_{IN} = 5.0 V, Includes $\overline{RST}$	$I_{PULLDOWN}$	50	120	175	µA
MISO High-Impedance Current MISO = 3.3 V or GND	I_{HI-Z}	-100	0.1	100	µA
5.0 V Linear Regulator					
Logic Supply Voltage $I_{V5.0}$ = 10 mA to 50 mA, 16 V ≤ B+ ≤ 20 V, R_{EXT} = 140 Ω	$V_{5.0}$	4.8	5.0	5.2	V
Load Regulation I_{LOAD} = 10 mA to 50 mA	V_{ILOAD}	–	–	±100	mV
Current Limit Threshold R_{EXT} = 0 Ω	I_{LIMIT}	75	135	600	mA
$V_{5.0}$ to Turn On/Off $V_{3.3}$ Regulator [7]	$V_{5_3.3t}$	–	2.2	–	V
Hysteresis for $V_{5_3.3t}$ [7]	$V_{5_3.3t_hys}$	–	175	–	mV

Notes

7. See Figure 9, Power-Up Sequencing, page 21.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 16 V ≤ B+ ≤ 34 V, 0°C ≤ T_A ≤ 70°C, and 0°C ≤ T_J ≤ 100°C unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
5.0 V Switching Regulator					
Vreg Threshold	$V_{5.0}$	4.8	5.0	5.2	V
Cycle-by-Cycle Current Limit Threshold $V_{5.0}$ = 2.0 V to Max $V_{5.0}$ ≤ 1.0 V	I_{LIMIT}	 0.75 –	 1.2 1.0	 2.25 –	A
$V_{5.0}$ to Turn On/Off $V_{3.3}$ Regulator [8]	$V_{5_3.3t}$	–	2.2	–	V
Hysteresis for $V_{5_3.3t}$ [8]	$V_{5_3.3t_hys}$	–	175	–	mV
3.3 V Switching Regulator					
Vreg Threshold	$V_{3.3}$	3.15	3.28	3.45	V
Cycle-by-Cycle Current Limit Threshold $V_{3.3}$ = 2.0 V to Max $V_{3.3}$ ≤ 1.0 V	I_{LIMIT}	 2.75 –	 3.6 3.5	 5.5 –	A
VCORE 3.3V Linear Regulator					
Voltage Tolerance I_{CORE} = 0.02 A to 0.3 A, V_{NOM} = 2.5 V I_{CORE} = 0.02 A to 0.3 A, V_{NOM} = 1.8 V I_{CORE} 0 0.02 A to 0.3 A, V_{NOM} = 1.5 V	V_{CORE_TOL}	 2.35 1.675 1.4	 2.49 1.78 1.49	 2.66 1.925 1.6	V
Load Regulation I_{LOAD} = 20 mA to 300 mA	V_{ILOAD}	–	±10	±100	mV
Current Limit Threshold	I_{LIMIT}	400	750	1200	mA
Motor Drivers in DC Mode					
Motor Driver A High- or Low-Side Switch Voltage Drop I_{PWM} = 1.7 A, GND or B+ to Output	$V_{DROP}(A)$	–	.65	1.5	V
Motor Driver A Output Current Limit	$I_{LIMIT}(A)$	3.6	4.9	7.2	A
Motor Driver B High- or Low-Side Switch Voltage Drop I_{PWM} = 2.0 A, GND or B+ to Output	$V_{DROP}(B)$	–	.70	1.4	V
Motor Driver B Output Current Limit	$I_{LIMIT}(B)$	2.8	4.9	7.2	A
Motor Driver C High- or Low-Side Switch Voltage Drop I_{PWM} = 0.375 A, GND or B+ to Output	$V_{DROP}(C)$	–	.75	1.5	V
Motor Driver C Current Limit—Top Side	$I_{LIMIT1}(C)$	0.75	1.2	1.5	A
Motor Driver C Current Limit—Bottom Side	$I_{LIMIT2}(C)$	1.0	1.65	2.0	A

Notes

8. See Figure 9, Power-Up Sequencing, page 21.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 16 V ≤ B+ ≤ 34 V, 0°C ≤ T_A ≤ 70°C, and 0°C ≤ T_J ≤ 100°C unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Motor Drivers in DC Mode (cont)					
Output MOSFET Leakage Current V_{GS} = 0.0 V, V_O = 0.0 V or 20 V	I_{DSS}	–	0.1	±40	µA
Current Limit Maximum Duty Cycle[9]	IDC_{LIMIT}	1.0	2.0	4.0	%
Current Limit Pulse Width[9]	$I_{LIMITPW}$	0.5	1.5	6.0	µs
Motor Driver C in Step Mode					
Switch Voltage Drop, Output to Ground I_{STEP} = 0.375 A, GND to Output	V_{SDROP}	–	–	1.5	V
Step Motor Current Limit B+ = 20 V	$I_{STEP(LIMIT)}$	1.0	–	2.0	A
Voltage at Which Internal Clamp Activates I_{DSS} = 1.0 mA, B+ = 20 V	V_{CLAMP}	44	51	59	V
Tested Maximum High-Voltage Leakage Current $V_S = V_{CLAMP}$ +4.0	$I_{BREAKDOWN}$	–	0.5	40	µA
Any Step Driver Output Leakage Current to Ground B+ = 20 V, V_S = 20 V	$I_{LEAKAGE}$	–	0.1	40	µA
Current Limit Maximum Duty Cycle	td_{ILIMIT}	5.0	11	15	%
Current Limit Pulse Width	$I_{LIMITPW}$	5	10	20	µs
V_b Charge Pump					
Boost Voltage I_B = 0.5 mA	V_b	B^++10	B^++11.5	B^++15	V
External N-FET Gate Drive Output					
GATEOUT High Output I_{OH} = 4.0 mA I_{OH} = 200 µA	V_{OH2}	V_b - 6.0 V_b - 0.3	V_b - 2.5 V_b - .1	V_b V_b	V
GATEOUT Low Output I_{OL} = -200 µA	V_{OL}	–	0.1	0.3	V

Notes

9. Motor driver A, B, C Top Side only. For C Bottom Side, see Motor Driver C in Step Mode: Current Limit Maximum Duty Cycle and Current Limit Pulse Width

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 16 V ≤ B+ ≤ 34 V, 0°C ≤ T_A ≤ 70°C, and 0°C ≤ T_J ≤ 100°C unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Supervisor Circuitry					
Minimum Function B+ for Charge Pump, Oscillator Up Reset/Fault Registers Valid [10]	B+	9.0	–	–	V
Minimum Function $V_{5.0}$ for $\overline{RST}$ Operational $\overline{RST}$ V_{OL} ≤ 0.05 V @ 1.0 mA [10]	$V_{5.0\ \overline{RST}}$	2.0	–	–	V
Minimum Function $V_{3.3}$ for $\overline{RST}$ Operational $\overline{RST}$ V_{OL} ≤ 0.05 V @ 1.0 mA [10]	$V_{3.3\ \overline{RST}}$	2.0	–	–	V
$\overline{RST}$ Low Voltage [11] $I_{\overline{RST}}$ ≤ 5.0 mA	V_{OL}	–	0.1	0.25	V
$\overline{RST}$ $V_{5.0}$ Threshold $V_{5.0}$ Rising $V_{5.0}$ Falling	 $V_{5.0\,t+}$ $V_{5.0\,t-}$	 – 4.5	 4.65 4.6	 4.75 4.70	V
$\overline{RST}$ Hysteresis for $V_{5.0}$	$V_{HYSV5.0}$	10	50	–	mV
$\overline{RST}$ $V_{3.3}$ Threshold $V_{3.3}$ Rising $V_{3.3}$ Falling	 $V_{3.3t+}$ $V_{3.3t-}$	 – 2.8	 2.9 2.9	 3.15 3.0	V
$\overline{RST}$ Hysteresis for $V_{3.3}$	$V_{HYS_3.3}$	10	15	–	mV
$\overline{RST}$ V_{CORE} Threshold V_{CORE} Falling	V_{CORE}	85	86	90	% V_{CORE_NOM}
$\overline{RST}$ Hysteresis for V_{CORE}	$V_{HYS\ CORE}$	–	10	–	mV
Overtemperature Junction Temperature[12] T_J Rising	$T_{J(OVER)}$	140	–	–	°C
Overtemperature Hysteresis[12] T_J Falling	$T_{J(HYS)}$	10	–	30	°C
Thermal Warning [12]	T_W	T_J-30	–	T_J-20	°C
B+ Undervoltage Threshold to Assert $\overline{RST}$ $V_{5.0}$ = +5.0 V, B+ Falling	$B+_{(FAULT)}$	12	12.75	13.5	V
B+ Undervoltage Threshold Hysteresis[13]	$B+_{FAULT(HYS)}$	1.0	1.5	2.0	V
Minimum B+ Necessary to Clear B+ Fault $V_{5.0}$ = +5.0 V, B+ Rising	$B+_{RECOVERY}$	–	–	15.25	V

Notes

10. If any of these conditions for this not is true, then $\overline{RST}$ is activated until all operating conditions are met.
11. The $\overline{RST}$ terminal uses an external pull-up, which may be to 5.0 V or 3.3 V.
12. Guaranteed by design.
13. Alternately, the minimum B+ fault threshold voltage must not be lower than 12 V, and the B+ fault clear voltage must not be higher than 15.25 V. The hysteresis may be greater than 2.0 V if this requirement is met.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 16 V ≤ B+ ≤ 34 V, 0°C ≤ T_A ≤ 70°C, and 0°C ≤ T_J ≤ 100°C unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Analog Encoder Interface Current-to-Voltage Conversion Stage					
Minimum Offset Current	I_{OFFSET_MIN}	-6.0	-8.0	-10	µA
Midpoint Offset Current	I_{OFFSET_MID}	-0.5	0.0	0.5	µA
Maximum Offset Current	I_{OFFSET_MAX}	6.0	8.0	10	µA
Offset Step Size (1 LSB)	$I_{OFFSTEP}$	0.25	0.5	0.75	µA
Analog-to-Digital Converter					
Resolution, No Missing Codes	ADC	–	–	8.0	Bits
Measurement Range for Correct Conversion	IMR	0.0	–	5.0	V
Linearity Error [16] Over Input Voltage Range of 4% to 96% Ideal Measurement Range (IMR) max. Over Time and Temperature [14], [15] V_{IN} = -0.5 to 5.5 V [17]	I_{NL}	–	0.4	±1.0 LSB	–
Input Leakage Current (ANx) $V_{5.0}$ = 5.0 V, T_J = 25°C, V_{ANx} = 5.0 V, ANALOG_TEST MODE = 0, Channel Not Selected	$I_{LEAKAGE}$	–	0.1	10	µA

Notes

14. Errors include effects of multiplexer and sample and hold circuitry, including droop.
15. The Linearity Error is the worst case error caused by the differential and integral nonlinearity.
16. An LSB (least significant bit) is defined as follows:

$$LSB = \frac{IMR}{2^{\#BITS}-1} \text{ Volts}$$

Where:
- IMR is the Ideal Measurement Range.
- #BITS is the resolution of the ADC.

17. The ADC will read full scale at V_{IN} = 5.0 V. If V_{IN} on one input exceeds this value, the value of other inputs may become unreadable.

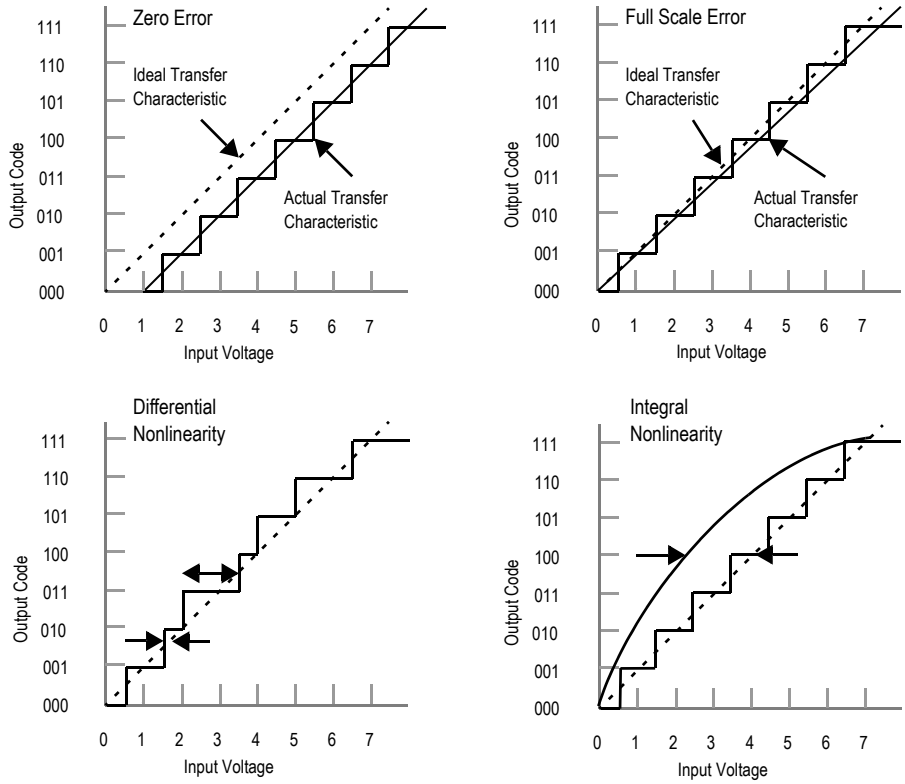
Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 16 V ≤ B+ ≤ 34 V, 0°C ≤ T_A ≤ 70°C, and 0°C ≤ T_J ≤ 100°C unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Analog-to-Digital Converter (cont)					
Zero Error [18], [19]	E_Z	–	±1.0	±8.0	LSB[20]
Zero Error Drift Over Time and Temperature [18]	E_{ZD}	–	±4.0	–	LSB
Full Scale Error [18], [19], [21]	E_{FS}	–	±2.0	±8.0	LSB

Notes

18. Errors include effects of multiplexer and sample and hold circuitry, including droop.
19. The Zero Error is defined as the number of LSB values away from the ideal value of 1/2 LSB that the ADC output count will transition from 0 to 1 when the input is swept through the range of interest. The transition must occur within the specified range.



20. An LSB is defined as follows:

$$LSB = \frac{IMR}{2^{\#BITS}-1} \text{ Volts}$$

Where:

- IMR is the Ideal Measurement Range.
- #BITS is the resolution of the ADC.

21. The Full Scale Error is defined as the number of LSB values away from the ideal value of -1/2 LSB from Full Scale that the ADC output count actually transitions from -1 LSB count to Full Scale count when the input voltage is swept through the voltage range of interest. The transition must occur within the specified range.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 16 V ≤ B+ ≤ 34 V, 0°C ≤ T_A ≤ 70°C, and 0°C ≤ T_J ≤ 100°C unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Serial Interface Timing[22]					
Setup Time for $\overline{CE}$ to rising edge of SCLK (C_L = 50 pF)	$t_{setup(\overline{CE})}$	–	15	–	ns
Hold Time for $\overline{CE}$ after falling edge of SCLK (C_L = 50 pF)	$t_{hold(\overline{CE})}$	–	15	–	ns
Setup Time for MOSI to rising edge of SCLK (C_L = 50 pF)	$t_{setup(MOSI)}$	–	15	–	ns
Hold Time for MOSI after falling edge of SCLK (C_L = 50 pF)	$t_{hold(MOSI)}$	–	15	–	ns
Delay for MISO valid after rising edge of SCLK (C_L = 50 pF)	$t_{delay(MISO)}$	–	35	55	ns
Period for SCLK (C_L = 50 pF)	$t_{period(SCLK)}$	125	–	750	ns
Duty Cycle of SCLK	$t_{duty(SCLK)}$	45	–	55	%
5.0 V Switching Regulator					
Switching Rise and Fall Time Load Resistance = 100 Ω, B+ = 18 V	t_r, t_f	10	30	50	ns
3.3 V Switching Regulator					
Switching Rise and Fall Time Load Resistance = 100 Ω, B+ = 18 V	t_r, t_f	10	16	50	ns
Motor Drivers					
Motor Drivers A and B Output Waveform Rise Time R = 7.0 Ω, V_{DCX} = (5.0 V) to (0.90 x B+), B+ = 18 V	t_r	100	175	300	ns
Motor Driver C Output Waveform Rise Time R = 25 Ω, V_{DCX} = (5.0 V) to (0.90 x B+), B+ = 18 V	t_r	100	175	300	ns
Output Waveform Fall Time V_{DCX} = (0.90 x B+) to 5.0 V, R = 7.0 Ω, B+ = 18 V	t_f	100	–	300	ns
Crossover Dead Time [23]	t_{dead}	15	600	2000	ns
Motor Driver C in Step Mode					
Output Rise Time V_{XPHASE} = 5.0 V to 0.90 x B+, R_w = 20 Ω, B+ = 18 V	t_r	100	175	350	ns
Output Fall Time V_{XPHASE} = 0.90 x B+ to 5.0 V, R_w = 20 Ω, B+ = 18 V	t_f	100	155	350	ns
Delay from Phase Turn-Off to Counterphase Turn-On R_w = 20 Ω, 0.90 x B+ Rising to 0.90 x B+ Falling, B+ = 18 V Falling	$t_{delay\ (C)}$	0.0	300	400	ns

Notes

22. See Figure 4, Serial Interface Timing, page 16.
23. This parameter is guaranteed by design but not production tested.

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 16 V ≤ B+ ≤ 34 V, 0°C ≤ T_A ≤ 70°C, and 0°C ≤ T_J ≤ 100°C unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Supervisor Circuitry					
$\overline{RST}$ Delay $V_{5.0}$ = ≥ +4.9 V [24]	t_{delay} ($\overline{RST}$)	128	–	128	t_{SCLK}
$\overline{RST}$ Filter Time $V_{5.0}$ = 5.0 V	t_{filter}	–	3.25	–	µs
$\overline{RST}$ Fall Time $V_{5.0}$ = 5.0 V, C_L = 100 pF, I_{PULLUP} = 0.75 mA(external), 90% to 10% of $V_{5.0}$	t_f	–	7.0	20	ns
External Input Low to $\overline{RST}$ Pulled Low $V_{5.0}$ = 5.0 V [25]	t_{slpl}	–	26	60	ns
Analog Encoder Interface Variable Gain Stage					
Adjustable Gain (Ideal) Settings S = 0 to 15, Default 0 Settings S = 16 to 31, Default 0	G (Ideal)	(1.0+0.1 ∗ S) (1.0+0.1 ∗ [S-16])/0.375			
Gain Setting = 0 Setting = 31	G	0.8 6.0	1.0 6.6	1.2 7.2	V/V
Gain Step Factor Tolerance Gain Step Size Gs/G(s-$_1$) S = 1 to 31	GSF	1.01	1.02	1.2	V/V
Analog Encoder Interface Digital Signal Conversion Stage					
Operating Frequency	$f_{OP(MAX)}$	0	–	15	kHz
Comparator Filter Time[24] Filter Configuration Bit Set to 0 Filter Configuration Bit Set to 1	t_{filter}	3.0 6.0	– –	4.0 7.0	SCLK Cycles
ADC					
Sample and Hold Acquisition Time A/D Speed Bit = 0 A/D Speed Bit = 1	t_{sh}	15 31	– –	16 32	t_{SCLK}
Conversion Time (Return Word Clocked Out Immediately Following t_c) A/D Speed Bit = 0 A/D Speed Bit = 1	t_c	– –	– –	48 96	t_{SCLK}
Master Oscillator					
Operating Frequency B+ ≥ 12 V	f_{OP}	150	200	250	kHz

Notes

24. Guaranteed by design.
25. See Figure 6, RST Timing, page 17.

TIMING DIAGRAMS

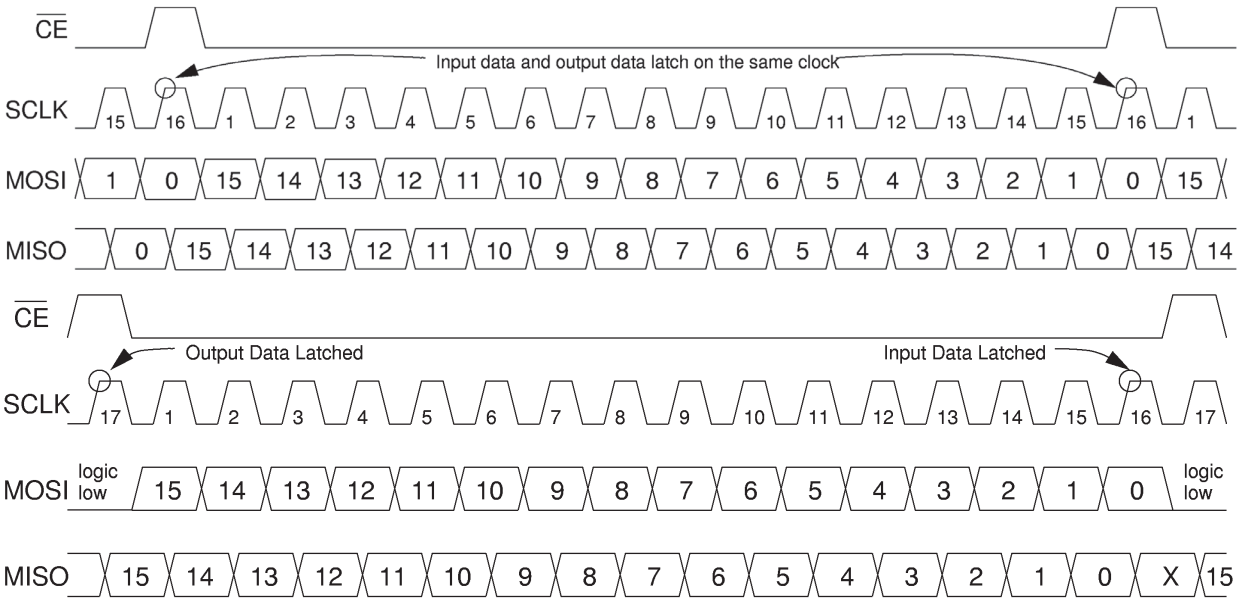


Figure 4. Serial Interface Timing

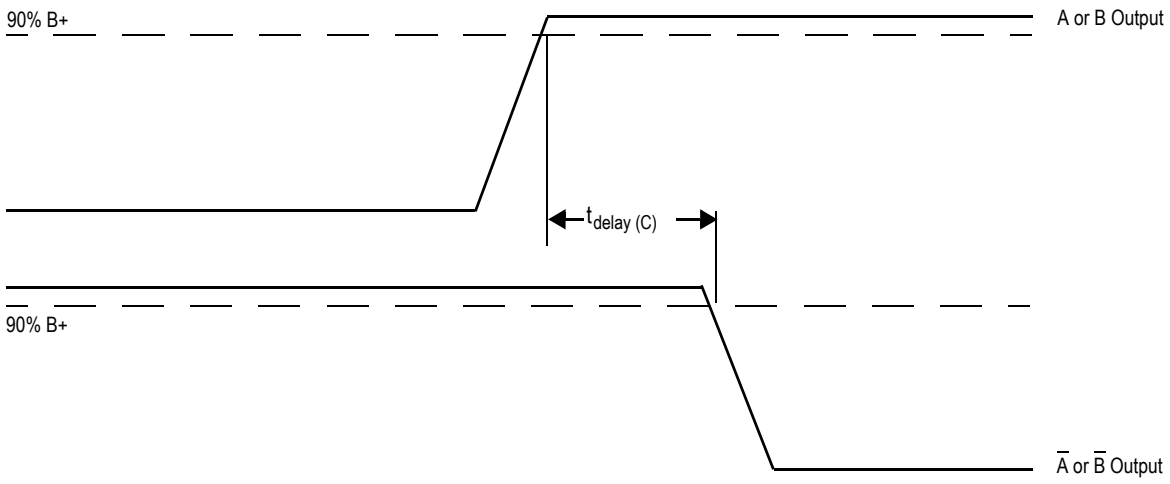


Figure 5. Step Motor Crossover Delay Timing

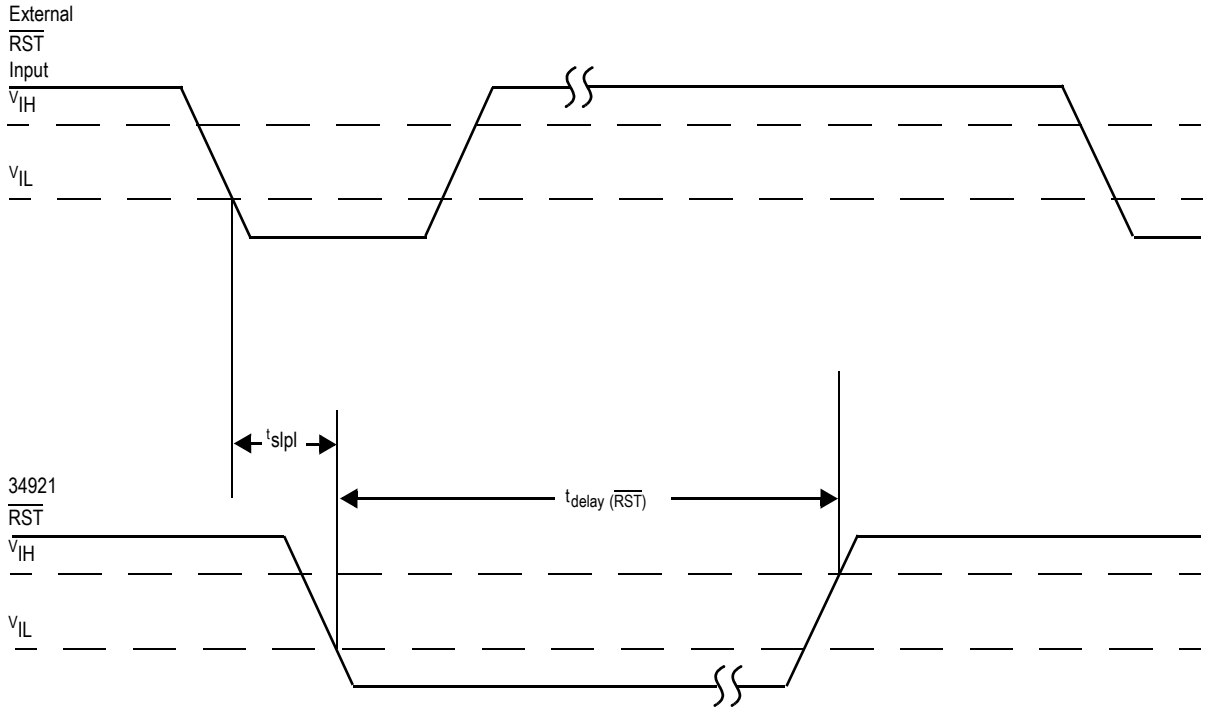


Figure 6. $\overline{\text{RST}}$ Timing

FUNCTIONAL DESCRIPTION

INTRODUCTION

The serial interface of the MC34921 is a three input, one output interface similar to a Serial Peripheral Interface (SPI) port in general form, but different in specific clocking requirements due to the fact that an A/D converter cannot reliably run without a continuous clock. The 34921 serial interface communicates to a microcontroller unit (MCU) at up to 16 MHz. The serial signals are SCLK, $\overline{CE}$, MOSI, and MISO. The SCLK signal pin requires a free-running clock (up to 16 MHz) which is provided by the MCU. This signal is required to ensure proper operation of both the ADC and the reset timer circuitry. The serial data transfers between the MCU and the 34921 via the MOSI and MISO terminals. The serial data from the MCU is handled in the MC34921 via two input registers -- the NORMAL input register contains bits controlling the motor drivers as well as the A/D converter, and the CONFIG register contains bits relating to the general configuration setup of the device. The MC34921 also has two output registers -- the NORMAL output register reports A/D conversion data as well as digital encoder data, and the IREQ output register reports under voltage, temperature, and other device status data.

FUNCTIONAL TERMINAL DESCRIPTION

GROUND (GND)

Main ground. It is used for the B+ filters and motor filter grounds, as well as the ground return for external components which are used with the linear and switching regulators.

COVER VOLTAGE OUTPUT SELECT (VCORE SELECT)

This terminal is used to select the output voltage provided by the VCORE linear regulator. The VCORE Select potential is latched in during the MC34921's power-on sequence. The MC34921 will not respond to changes in VCORE Select after power up.

Unipolar Step A/DC Motor C Output A ($\overline{SA}$/CDCMA)

A low-side driver output is configurable for either stepper motor control ($\overline{SA}$) or C DC motor (as CDCMA, which requires an external hardwire to pin 63) via the serial I/O. The driver is PWM controlled via the CPWMA/CDCPWM pin, and direction controlled via the Serial I/O. It includes an active voltage clamp, current limit, and thermal shutdown protection.

Unipolar Step $\overline{A}$/DC Motor C Output B ($\overline{SA}$/CDCMB)

A low-side driver output is configurable for either stepper motor control ($\overline{SA}$) or C DC motor (as CDCMB, it requires external hardwire to pin 61) via the serial I/O. The driver is PWM controlled via the CPWMA/CDCPWM pin, and direction controlled via the Serial I/O. It includes active voltage clamp, current limit, and thermal shutdown protection.

Unipolar Step B/LOW-SIDE 1 ($\overline{SB}$/LSOUT1)

A low-side driver output is configurable for either stepper motor control ($\overline{SB}$) or as a general purpose low-side driver (LSOUT1) via the serial I/O. The $\overline{SB}$ is PWM controlled via the CPWMB pin. The direction and LSOUT1 are controlled via the serial I/O. It includes active voltage clamp, current limit and thermal shutdown protection.

Unipolar Step $\overline{B}$/LOW-SIDE 2 ($\overline{SB}$/LSOUT2)

A low-side driver output is configurable for either stepper motor control ($\overline{SB}$) or as a general purpose low-side driver (LSOUT2) via the serial I/O. The $\overline{SB}$ is PWM controlled via the CPWMB pin. The direction and LSOUT2 are controlled via the serial I/O. It includes active voltage clamp, current limit and thermal shutdown protection.

POWER SUPPLY INPUT (B+)

This is the main power supply input for the regulators and DC motor drivers.

3.3 V SWITCHING REGULATOR SWITCH OUTPUT (3.3 V SWITCH)

The high-side driver output is used for the 3.3v switching regulator. It uses the internal 200KHZ clock.

3.3 V REGULATOR FEEDBACK (3.3 V)

This terminal is the error amp feedback for the 3.3v switching regulator. It is also the output point for the 3.3v switching supply.

CORE VOLTAGE REGULATOR INPUT (VCORE SUPPLY)

The input voltage terminal for the VCORE linear supply, which is usually provided by externally hardwiring the 3.3v switching regulator output.

CORE VOLTAGE REGULATOR OUTPUT (VCORE)

The output terminal of the VCORE linear regulator. Voltage options of 1.5v, 1.8v, or 2.5v are set by the potential of the VCORE Select pin at power up. It features current limit and thermal shutdown protection. It is typically used to supply a micro processor core or embedded DRAM.

DC MOTOR A OUTPUT A (ADCMA)

A high-side and low-side driver output terminal, which when combined with ADCMB forms the A H-bridge DC motor driver. The driver is PWM controlled via the APWM input, and direction controlled via the Serial I/O. It features current limit and thermal shutdown protection.

DC MOTOR A OUTPUT B (ADCMB)

A high-side and low-side driver output terminal, which when combined with ADCMA forms the A H-bridge DC motor driver. The driver is PWM controlled via the APWM input and direction controlled via the Serial I/O. It features current limit and thermal shutdown protection.

BOOST VOLTAGE (VBOOST)

This is the boost voltage storage node for the charge pump circuit. It provides the gate drive voltage for the high-side FETS in the DC motor drivers, switch mode controllers, and Gateout pin.

SWTICHING CAPACITOR (CP1 AND CP2)

These are the connections for the charge pump flying capacitor.

HIGH-SIDE MOSFET GATE DRIVER (GATEOUT)

The output terminal for an external N-channel high-side driver. Enabled via the Serial I/O, it provides gate drive control for an external N-channel MOSFET high-side switch.

DC MOTOR B OUTPUT B (BDCMB)

A high-side and low-side driver output terminal, which when combined with BDCMB, forms the B H-bridge DC motor driver. The drivers are PWM controlled via the BPWM input, and direction controlled via the Serial I/O. It features current limit and thermal shutdown protection.

DC MOTOR B OUTPUT A (BDCMA)

A high-side and low-side driver output terminal, which when combined with BDCMA, forms the B H-bridge DC motor driver. The drivers are PWM controlled via the BPWM input, and direction controlled via the Serial I/O. It features current limit and thermal shutdown protection.

5.0 V REGULATOR MODE SELECT (5 V SELECT)

This terminal is used to set the 5v regulator to operate in either linear or switching mode. Ground this terminal to operate in switching mode, or float to operate in linear mode.

5.0 V REGULATOR SWITCH OUTPUT (5 V SWITCH)

This terminal is the high-side driver output used for the 5v switching regulator. It uses the internal 200KHZ clock.

5.0 V REGULATOR INPUT SUPPLY (5 V SUPPLY)

The input voltage terminal for the 5v regulator. Limit it to 20v in linear mode. An additional series resistor is recommended to dissipate power off-chip.

5.0 V REGULATOR FEEDBACK (5 V)

This is the 5v feedback input terminal and output voltage point for the 5v regulator when in the switch configuration, and the output pin when tied to 5v SWITCH in linear configuration. It is also the power supply terminal for the MC34921AE on board logic.

AN0/ANALOGOUT_A (AN0/ANALOGOUT_A)

Mux input 0 for the A/D converter, which is also available in Freescale test mode as an output for the AN2 I/V converter.

AN1/ANALOGOUT_B (AN1/ANALOGOUT_B)

Mux input 1 for the A/D converter, which is also available in Freescale test mode as an output for the AN3 I/V converter.

AN2/ANALOGIN_A (AN2/ANALOGIN_A)

Mux input 2 for the A/D converter incorporating an I/V converter with offset and gain calibration via the Serial I/O.

AN3/ANALOGIN_B (AN3/ANALOGIN_B)

Mux input 3 for the A/D converter incorporating an I/V converter with offset and gain calibration via the Serial I/O.

ANALOG ENCODER CHANNEL B FILTER (ENC_FILTB)

Input to the AN3 I/V converter stage for feedback components used with the I/V converter op amp.

ANALOG ENCODER CHANNEL A FILTER (ENC_FILTA)

Input to the AN2 I/V converter stage for feedback components used with the I/V converter op amp.

RESET ($\overline{\text{RST}}$)

Supervisory function I/O, incorporating a comparator input and an open drain output, and typically connected to the $\overline{\text{RST}}$ of a microprocessor. As an input, $\overline{\text{RST}}$ resets internal registers to default states, turns step motor outputs off, forces DC motor drive low-side drives on, and sets MISO to a high Z state. As an output, $\overline{\text{RST}}$ is set during B+ UVLO, all regulators UVLO, current limit, and thermal shutdown events.

MASTER IN SLAVE OUT (MISO)

This is the master-in-slave-out terminal; the serial output port of the Serial I/O, which typically connects to the MISO of a microprocessor. MISO reports two data frames: NORMAL - A/D conversion and analog encoder signals, and INFO - Fault data and analog encoder signals.

The output data is loaded into the output shift register on each rising edge of SCLK, while $\overline{\text{CE}}$ is held in a logic high

state. This means the MISO pin shows the status of the most significant bit (bit 15) of the output frame until the first rising edge of SCLK after the $\overline{CE}$ pin is taken to a logic low state. The shift register will then shift data out on the MISO pin on each subsequent rising edge of SCLK while $\overline{CE}$ is held in the logic low state. During transfers, the most significant bit (MSB) is transferred first. After all 16 bits have been transferred, if any additional clocks are given while $\overline{CE}$ is in a logic low state, the data is undefined and should be ignored.

MASTER OUT SLAVE IN (MOSI)

This is the master-out-slave-in terminal; the serial input port of the Serial I/O, which typically connects to the MOSI of a microprocessor. It has two frames of operation - NORMAL and CONFIG, which are set by a bit in the NORMAL frame.The MOSI pin is used for serial instruction data input. MOSI information is clocked into the input shift register on the rising edge of SCLK. A logic high state present on MOSI will program a register bit on. The specific bit will turn on with the 16th rising edge of SCLK after placing the $\overline{CE}$ pin in a logic low state. Conversely, a logic low state present on the MOSI pin will program the register bit off. The specific bit will turn off with the 16th rising edge of SCLK after placing the $\overline{CE}$ pin in a logic low state. For each rising edge of the SCLK while $\overline{CE}$ is logic low, a data bit instruction (on or off) is loaded into the shift register per the data bit MOSI state. The last bit clocked in (bit 0) is the CONFIG bit. If this bit is in a logic high state at the 16th rising edge of SCLK after lowering the $\overline{CE}$ pin, the bits in the shift register will be loaded into the CONFIG register. If the bit is in a low logic state, the bits will be loaded into the NORMAL register. Care should be taken to keep the MOSI pin in a logic low state when it is not being used for transfers to avoid erroneous data. During transfers, the most significant bit (MSB) is clocked in first.

SERIAL CLOCK (SCLK)

As the serial clock terminal, the SCLK pin clocks the internal shift registers of the MC34921. The serial data input (MOSI) pin data is latched into the input shift register on the rising edge of the 16th clock after the falling edge of the chip select ($\overline{CE}$) pin. The serial data output (MISO) pin shifts data out of the shift register on the rising edge of the SCLK signal. False clocking of the shift register must be avoided to ensure validity of data. It is essential that one rising edge of SCLK occur while $\overline{CE}$ is in a logic high state to ensure the correct output data is latched into the output shift register. Clocking the SCLK pin for more than one clock period while $\overline{CE}$ is in a logic high state is not recommended and may have undesired effects. For this reason, it is recommended that the SCLK pin be clocked only once while $\overline{CE}$ is in a logic high state. The MC34921 is designed such that SCLK should be a continuous clock. This ensures that A/D sample rates are held as constant as possible.

CHIP ENABLE ($\overline{CE}$)

The chip enable port of the Serial I/O, typically connects to the $\overline{CE}$ of a microprocessor. The logic state of the $\overline{CE}$ pin activates clocking in and shifting out of data in and out of the MC34921. While the $\overline{CE}$ pin is in the logic high state, the output data in the NORMAL registers and the INFO registers are latched (depending on the state of the IREQ bit in the previous communication frame) in on each rising edge of the clock such that the state of the MSB (bit 15) is readable on the serial data output (MISO) pin. When $\overline{CE}$ is in a low logic state both the input shift register and output shift register shift data at the rising edge of SCLK.

MOTOR DRIVER C PWM INPUT A (CPWMA /CDCPWM)

This is the PWM logic input for the $\overline{SA}$/$\overline{SA}$/CDCM motor drivers. The motor driver outputs follow this signal.

MOTOR DRIVER C PWM INPUT B (CPWMB)

This is the PWM logic input for the $\overline{SB}$/$\overline{SB}$ motor drivers. The motor driver outputs follow this signal.

DIGITAL GROUND (DGND)

This terminal is used for the Serial I/O and A/D converter logic grounds, and should be kept isolated from the Analog ground on the application PCB.

MOTOR DRIVER A PWM INPUT (APWM)

The PWM logic input terminal for the ADCM motor drivers. The motor driver outputs follow this signal.

MOTOR DRIVER B PWM INPUT (BPWM)

The PWM logic input terminal for the BDCM motor drivers. The motor driver outputs follow this signal.

MOTOR DRIVER C STEP MOTOR OUTPUT OR HIGH-SIDE OUTPUT 2 (CDCMB / HSOUT2)

The high-side driver output is configurable for either C DC motor control (as CDCMB, it requires external hardwire to pin 4), or as a general purpose high-side driver (HSOUT2) via the serial I/O. The CDCMB is PWM controlled via the CPWMA/ CDCPWM pin. The direction and HSOUT2 are controlled via the serial I/O. It includes current limit and thermal shutdown protection.

MOTOR DRIVER C STEP MOTOR OUTPUT OR HIGH-SIDE OUTPUT 1 (CDCMA / HSOUT1)

The high-side driver output is configurable for either C DC motor control (as CDCMA, it requires external hardwire to pin 4), or as a general purpose high-side driver (HSOUT1) via the serial I/O. The CDCMA is PWM controlled via the CPWMA/ CDCPWM pin. The direction and HSOUT1 are controlled via the serial I/O. It includes current limit and thermal shutdown protection.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION

5.0 V AND 3.3 V REGULATORS

The 34921 5.0 V regulators have two operating modes—switching and linear—that share a dedicated input terminal, as illustrated in Figure 7 and Figure 8. The 5.0 V switching regulator operates off B+ directly. The 5.0 V linear regulator is only used when B+ < 20 V, and the dedicated input terminal is connected to B+ through an external power resistor to dissipate some power off-chip. The regulator that is used depends on the power requirement and $B+_{NOM}$ of the application. The designer is able to trade off power versus overall system cost for each particular application. The linear regulator mode is a low-current mode and has much less external component cost.

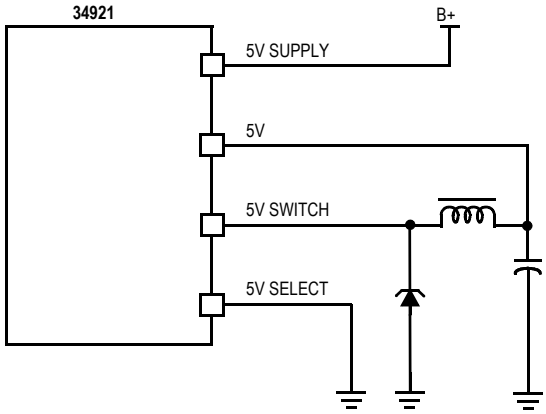


Figure 7. 5.0 V Switching Regulator Mode

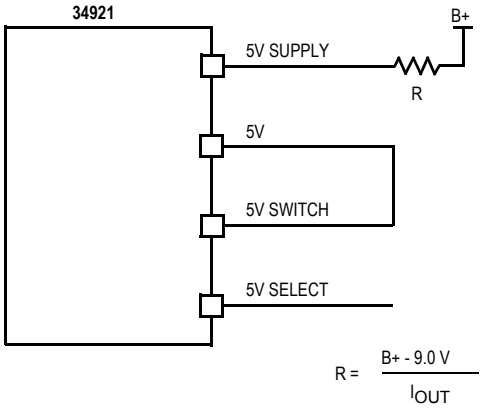


Figure 8. 5.0 V Linear Regulator Mode

The 5V SELECT terminal must be tied to ground for switching regulator mode. An internal pull-up is incorporated in the 34921 sufficient to avoid any problems owing to switching noise on this terminal.

The 5.0 V switching and linear regulators may supply external logic components of the overall assembly, depending on the application. For the 5.0 V linear regulator, an external capacitor on the output should be used for filtering.

5.0 V and 3.3 V Switching Regulators

The 5.0 V and 3.3 V switching regulators are implemented as constant ripple buck regulators. These regulators operate in both discontinuous and continuous mode. The clock source is the on-board 200 kHz master oscillator. The actual frequency of the switch terminal can vary owing to cycle skipping. The switch MOSFET is internal to the 34921 IC, but the remaining components—recovery diode, inductor, and output capacitor—must be externally supplied. The input voltage to the regulators is B+, and the regulators perform within specifications over the range of $I_{5.0} \leq 0.6$ A for the 5.0 V switching regulator and $I_{3.3} \leq 2.5$ A for the 3.3 V switching regulator. Each has cycle-by-cycle current limiting.

The power up sequence of the 5.0 V and 3.3 V switching regulators is controlled such that -1.0v <= V5 - V3.3 <= 2.6v. Figure 9 depicts the power-up sequence for the 5.0 V and 3.3 V regulators.

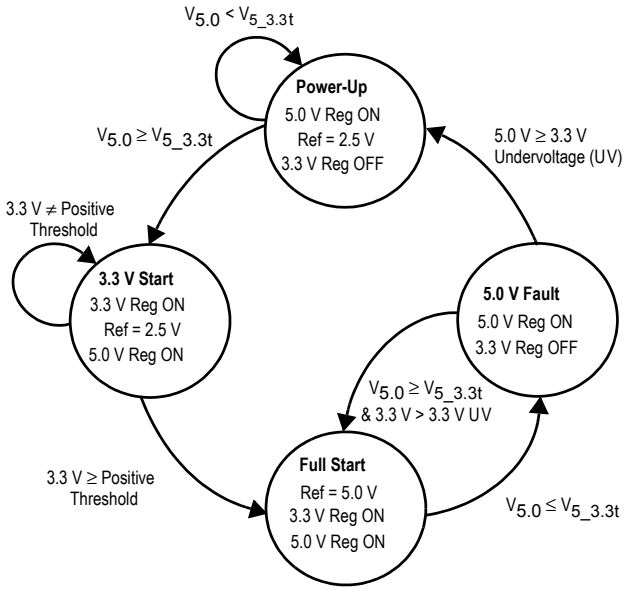


Figure 9. Power-Up Sequencing

VCORE Linear Regulator

The output voltage of the VCORE linear regulator is selectable for different applications. The output is selected with an external pull-up or pull-down, which instructs internal logic to select the appropriate regulator set-point (refer to Table 5). The VCORE linear regulator is available whenever the 3.3 V supply is in stable operation.

Current limiting is implemented to provide short circuit protection. The VCORE linear regulator is shut off by the local thermal shutdown sensor, thus protecting the 34921 IC from an over-temperature condition resulting from a VCORE short

circuit, but otherwise allowing VCORE to follow the 3.3 V switching regulator.

The VCORE SUPPLY terminal is the drain or collector of the linear regulator transistor and must be tied to the 3.3V terminal to use the internal regulator. This allows the option of using an external regulator if the internal 3.3 V regulator cannot supply enough current for a particular application. Use of an external regulator requires leaving this terminal open, thus disabling the internal regulator. The output of the external regulator is then connected to the VCORE terminal for under-voltage monitoring.

Table 5. V_{CORE} Regulator Output Voltage Select

$V_{CORE\ SELECT}$	V_{CORE_NOM} (Volts)
Tied to Ground terminal	1.5
Tied to 3.3V terminal	1.8
Floating	2.5

DC Motor Drivers

There are two DC motor drivers on the 34921 IC: if used in a printer application, for example, they might be the carriage motor driver and the paper motor driver. A third drive, Motor Driver C, can be configured as a DC motor driver or, when $B+_{NOM}$ = 18 V, as a step motor driver (refer to succeeding paragraph Step Motor Driver). Configuration bit 13 determines the mode: 0 = step mode, 1 = DC mode. A step motor driver can only be used in B+ = 12 V to 20 V applications. Step motor outputs are suppressed by the internal supervisor for B+ > 20 V. The ability to use the low-side MOSFETs for general purpose low-side outputs is included when the system is in DC motor mode (LSOUTx). Alternatively, the ability to use the high-side MOSFETs for general purpose high-side outputs (HSOUTx) has been included when the system is in step mode. (Refer to Table 20, page 31, and Table 21, page 32.)

The DC motor drivers are pulse width modulated (PWM'd) via inputs from the digital subsystem on the APWM and BPWM terminals, respectively. This signal is approximately 20 kHz to 40 kHz. The DC motor driver bridge direction may be reversed while there is significant current flowing in the motor. The purpose of this action is to brake the motor by rapidly lowering the current. There are pull-downs on the PWM input terminals so that, in the event of a connection failure, the driver will default to a safe condition.

The DC motor drivers provide high-side and low-side current limiting. The current limits have a 0.5 µs to 6.0 µs deglitch filter, followed by an off-timer. The off-timer shuts off the bridge long enough to meet the 4% duty cycle goal. The motor drivers also have thermal shutdown protection.

Step Motor Driver C

Step motor driver C can be configured as a DC motor driver or, when $B+_{NOM}$ = 18 V, as a step motor driver (refer to succeeding paragraph Step Motor Driver). Configuration bit 13 determines the mode: 0 = step mode, 1 = DC mode. The ability to use the low-side MOSFETs for general purpose low-side outputs is included when the system is in DC motor mode (LSOUTx). Alternatively, the ability to use the high-side MOSFETs for general purpose high-side outputs (HSOUTx) has been included when the system is in step mode. (Refer to Table 20, page 31, and Table 21, page 32.)

Step motor driver C is PWM'd via an input from the digital subsystem on the CPWMA/CDCPWM terminal. This signal is approximately 20 kHz to 40 kHz. There are pull-downs on the PWM input terminals so that DC motor drive C will default to a safe condition in the event of a connection failure.

Step Motor Driver

A step motor driver can be configured as a DC motor driver (refer to preceding paragraph DC Motor Drivers) or, when $B+_{NOM} \leq 20$ V, as a unipolar step driver. Serial input configuration frame bit 4 determines the mode: 0 = step mode, 1 = DC mode. A step motor driver will only be used in B+ = 12 V to 20 V applications.

Note It is possible to use the step motor driver with B+ > 20 V if the step motor is driven from a separate supply that is ≤ 20 V.

The step motor driver on the 34921 is a unipolar, voltage-mode wave drive circuit employing synchronous rectification. The centertap of each phase-counterphase pair is connected to B+.

Two PWM signals are sent directly from the digital subsystem. The CPWMA/CDCPWM terminal provides the PWM signal for the A and $\overline{A}$ outputs. The CPWMB terminal provides the PWM signal for the B and $\overline{B}$ outputs. The step motor driver employs synchronous rectification to control substrate currents. In synchronous rectification, when an output is turned off, the counterphase output MOSFET is turned on to maintain current continuity. In order to avoid a large shoot-through current, there is a dead time delay (t_{delay}) between phase off and counterphase on. Refer to Figure 5, Step Motor Crossover Delay Timing, page 16.

VBOOST Charge Pump

The high-side MOSFETs in the DC motor H-bridges and the external GATEOUT switch need a gate voltage in excess of B+, which is provided by the VBOOST supply. The VBOOST regulator is a charge pump, switching directly off the B+ supply and operating at 200 kHz.

External N-FET Gate Drive Output

The GATEOUT terminal is an output for a high-side N-channel MOSFET gate drive. The output will be used to drive an external high-side MOSFET switch (see figure below). When enabled, GATEOUT will be connected to the V_b supply. The edge rates when switching the transistors must be controlled so that shoot-through current does not affect B+.

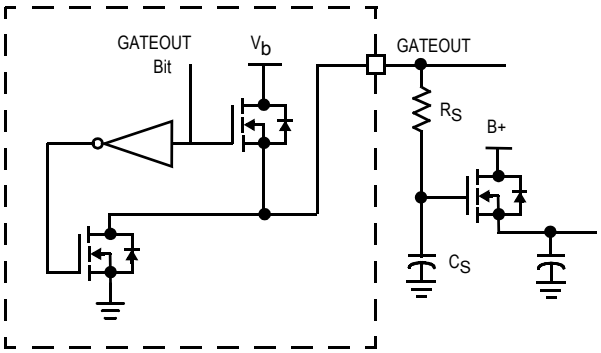


Figure 10. External N-FET Gate Drive Circuit

Clocking Schemes

There are two basic clocking schemes that can be used while clocking data into the MC34921 IC. One has 16 rising edges of SCLK while $\overline{CE}$ is in a logic low state and the other has 15 rising edges of SCLK. In the 15 SCLK clocking scheme, the input data and output data are latched on the same clock edge. In the timing diagram on page 16, the numbers on the MOSI line are the bits that will be clocked into the input shift register at the rising edge of SCLK. They are drawn occurring before SCLK to account for the required setup time (minimum 15ns). The numbers on the MISO line are the bits that will be clocked out at the rising edge of SCLK. They are drawn occurring after SCLK to account for the output delay from the rising edge of SCLK (maximum 40ns). The numbers on the SCLK line are for reference only.

Note: when using the 15 bit clocking method with exactly one rising edge of SCLK when CE is in a logic high state, the output data to be sent out is latched at the same time the IREQ bit is latched in. The next frame following the assertion of the IREQ bit is the IREQ data. I.e., the frame after the sending of the IREQ bit will have the data from the IREQ register rather than skipping one frame. Note: regarding the reporting of the DONE bit after the completion of an A/D conversion: the DONE bit is sent out every time a conversion completes. This requires the user to hold the MOSI pin in a low state when it is not being used to transmit data. Refer to Figure 4, Serial Interface Timing and Figure 5, Step Motor Crossover Delay Timing

SUPERVISORY (RST) FUNCTION

Supervisory Circuitry

The supervisor circuitry provides control of the $\overline{RST}$ line, an open drain signal, based on system operating conditions monitored by the 34921 IC. $V_{5.0}$, $V_{3.3}$, V_{CORE}, B+, and thermal shutdown detectors in various parts of the chip are monitored for error conditions. Because other devices in the system may trigger a reset, the $\overline{RST}$ line itself is also monitored, but the supervisor circuitry controls all reset timing, including externally generated resets. Driving the $\overline{RST}$ line low causes the system to be held in the reset state. $V_{5.0}$, $V_{3.3}$, V_{CORE}, B+, and TSD have both positive- and negative-going thresholds.

Static Operating Specifications

The state of $\overline{RST}$ is guaranteed as long as the minimum supervisor operating conditions of B+ ≥ 9.0 V and $V_{5.0}$ ≥ 2.0 V and $V_{3.3}$ ≥ 1.5 V and V_{CORE} are met. Once all these conditions are met, $\overline{RST}$ is dependent on system operating conditions. During initial power-up, $\overline{RST}$ is held low if any one of the following error conditions is present: +5.0 V(low), V_{CORE}(low), +3.3 V(low), B+(low), or TSD. Once all voltages reach their positive-going threshold, $\overline{RST}$ is set high after the appropriate timing.

Dynamic Operating Specifications

The $\overline{RST}$ is a bidirectional signal with an open drain output driver and a CMOS digital input gate (see Figure 11). This I/O structure allows wired OR connection to the CPU's $\overline{RST}$ I/O terminal, as well as allowing the CPU to initiate a reset cycle by driving its $\overline{RST}$ terminal low. When responding to a CPU request for a reset cycle, the 34921 IC must respond rapidly enough to prevent a glitch. Figure 6, RST Timing, page 17, shows the timing parameters for responding to an externally applied $\overline{RST}$ signal.

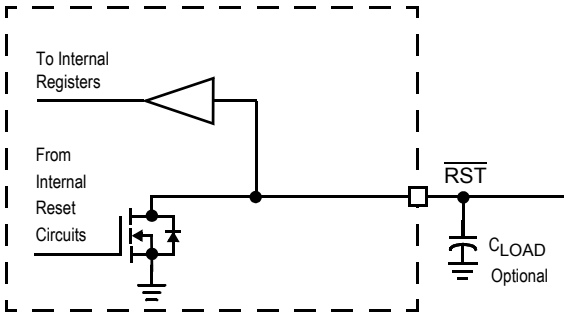


Figure 11. $\overline{RST}$ Terminal Interface

The rise time with the open drain circuit may be relatively slow, and the internal $\overline{RST}$ input gate must operate reliably (no oscillations during the transition) under these conditions; i.e., the $\overline{RST}$ input can be inhibited for up to t_{phsl} (max). Error conditions must be present for a minimum time, t_{filter}, before the 34921 responds to them. Once all error conditions are cleared, $\overline{RST}$ is held low for an additional time of t_{delay},

128 SCLK periods. If any monitored item falls below its negative-going threshold for t_{filter}, 1.5 µs to 5.0 µs, the t_{delay} count is restarted when system operating conditions are met, regardless of whether the t_{delay} count has been completed. The trigger for the t_{delay} retriggerable one shot is ([+5.0 V(low) + 3.3 V(low) + V_{CORE} (low) + B+(low) + TSD] and t_{filter}), where t_{filter} is the 1.5 µs to 5.0 µs delay.

$\overline{\text{RST}}$ and Thermal Shutdown State (TSD) Definition

There are seven registers in the INFO output word where the trigger for the reset is recorded. This includes externally generated resets as well as all the fault conditions listed in the Supervisory Functions section of this datasheet. These registers will remain valid as long as B+ ≥ 9.0 V. The fault registers will only be cleared upon an externally generated $\overline{\text{RST}}$ and will not be guaranteed for B+ < 9.0 V; i.e., initial power-up or a serious B+ fault. The EXT bit will only be set upon an externally generated reset.

Whenever $\overline{\text{RST}}$ is asserted and TSD is not set, the MISO terminal will enter a high-impedance state, all the step motor outputs will be off, and all the DC motor low-side drives will be on. In addition, all internal data registers excepting the $\overline{\text{RST}}$ fault registers in the INFO output word will be set to their default values.

The thermal shutdown circuitry will monitor the chip's internal temperature at various points. The overtemperature circuitry will disable all circuitry on the 34921 IC with the exception of the $\overline{\text{RST}}$ output. $\overline{\text{RST}}$ will be asserted when the temperature exceeds 140°C. This condition will be maintained (regulators shut down in accordance with Table 6, page 24) until the die temperature falls by the thermal hysteresis amount, at which time the 5.0 V and 3.3 V regulators will restart and the supervisor circuit will issue a full length reset pulse. The system will then perform a normal restart. The purpose of this circuitry is to prevent damage to the 34921 owing to inadvertent high dissipation in the motor drivers.

Table 6. Regulator Shutdown Schedule

Condition	XDCMA[26]	XDCMB[26]	$\overline{\text{SX}}$	$\overline{\text{SX}}$	5.0 V	V_{CORE}	3.3 V	Fault Registers	Other Data Registers
$\overline{\text{RST}}$	0	0	OFF	OFF	ON	ON	ON	Updated at falling $\overline{\text{RST}}$	Default value
TSD and $\overline{\text{RST}}$	Z	Z	OFF	OFF	OFF	ON	OFF	Updated at falling $\overline{\text{RST}}$	Default value
TSDCore and $\overline{\text{RST}}$	Z	Z	OFF	OFF	OFF	OFF	OFF	Updated at falling $\overline{\text{RST}}$	Default value

Notes
26. XDCMA and XDCMB: 0 means low-side ON, 1 means high-side ON, Z means both OFF.

ANALOG ENCODER INTERFACE

Introduction

The analog encoder interface is intended to provide a complete interface for an analog quadrature encoder, such as an Agilent Technologies HEDS-9710/HEDS-9711 series of analog output small optical encoder modules.

The Agilent HEDS-9710/HEDS-9711 incremental analog quadrature encoder is a 200 lpi encoder that outputs a quadrature analog current reflecting the position of the encoder codewheel/codestrip within the encoder. The analog encoder interface must provide six functions to support this encoder: force a bias point of 1.3 V, current-to-voltage conversion, offset current nulling, output amplitude adjust (variable gain), channel inversion, and digital phase generation (see Figure 12).

Note: Freescale does not assume liability, endorse, or warrant components from external manufacturers that are referenced in this document. While Freescale offers component recommendations, it is the customer's responsibility to validate their application.

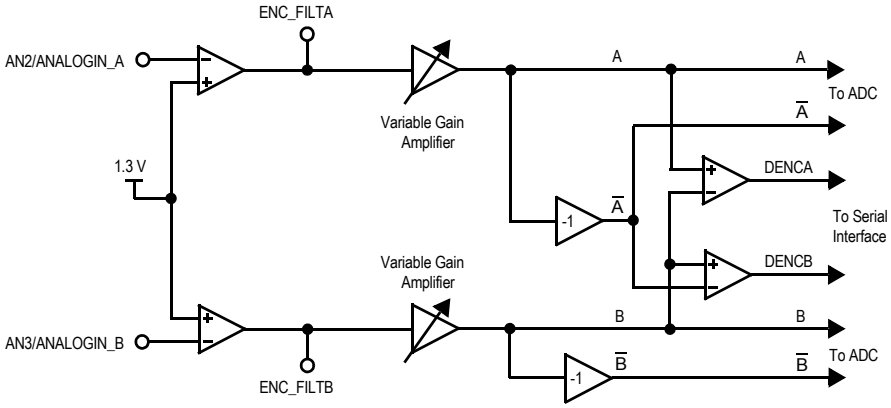


Figure 12. Analog Encoder Interface Block Diagram

I/V Conversion Stage

The I/V conversion stage is carried out by a transimpedance amplifier using an external resistor. There is a resistor to ground at the ANALOGIN_x input to allow offset current trim and force the proper bias point on the encoder. The feedback resistor should be sized to accommodate ±2.5 V output voltage swing for the full encoder current waveform. For example, if the encoder produces a ±50 μA signal, the feedback resistor needs to be 50 kΩ.

The resistor to ground must have a specific relationship to the feedback resistor. It needs to be 1.17 times the feedback resistor, or 58.5 kΩ for the example above. This ensures that the encoder is biased at 1.35 V, and that the output of the transimpedance amplifier is 2.5 V.

The I/V conversion stage can trim an encoder offset current of up to ±8.0 μA in the encoder output.

Variable Gain Amplifier

The I/V conversion stage is followed by a variable gain amplifier that can compensate for variations in the encoder output. This is designed to accommodate manufacturing variations in the encoder, as well as aging and other effects. The gain can be changed over the serial interface at any time.

The output of the variable gain amplifiers can be routed to the ANALOGOUT_x terminals for engineering evaluation. Otherwise, these terminals are general purpose A/D inputs.

Channel Inversion and Digital Phase Generation

The A and B channels are inverted by applying the function $\overline{\text{CHANNELx}}$ = 2.5 V - CHANNELx. This results in four signals: A, B, $\overline{A}$, and $\overline{B}$. These signals are used produce the digital encoder signals DENCA and DENCB, which are converted by the ADC to provide the analog position information. The value of the DENCA and DENCB signals determine which signal—A, B, $\overline{A}$, or $\overline{B}$—is converted. Refer to Table 7, page 26, for more information.

Position Information

The entire position information is produced by concatenating the value of the a quadrature counter, driven by DENCA and DENCB bits, and the 8 bits of “fractional” information from the ADC.

Calibration of the Encoder

It is necessary to adjust the gain and offset of the I/V circuit initially and periodically to compensate for encoder-to-encoder variation, aging, and other effects. The ADC “double conversion” function allows this by continuously sampling the A and B signals, allowing a map of the encoder output to be built up. The user will need to provide the necessary algorithm to use the waveform map to produce gain and offset calibration values for both channels.

ANALOG-TO-DIGITAL CONVERTER

Introduction

There is an 8-bit analog-to-digital converter (ADC) on the 34921 IC that uses the on-board voltage reference and derives all the necessary timing signals from the SCLK input. The ADC is referenced to the same ground as the system ground (GND).

ADC Input Selection

The ADC has an 8-channel analog multiplexer so that all inputs share one ADC. The input(s) to be converted are determined by the A/Da[2:0] bits in the serial normal input frame (refer to Table 11, page 28).

Three different types of conversion can occur (refer to Table 7):

- **Single Conversion** 00X does a single conversion of inputs AN0/ANALOGOUT_A or AN1/ANALOGOUT_B.
- **Double Conversion** 1XX does a double conversion of channels A and B, A and $\overline{A}$, B and $\overline{B}$, or AN2/ANALOGIN_A and AN3/ANALOGIN_B, respectively.
- **Auto-Select Conversion** 011 does a single conversion of one of the outputs from the analog encoder interface, as selected by the digital outputs of the analog encoder interface, DENCA and DENCB.

Table 7. A/D Input Conversion Channel Addressing

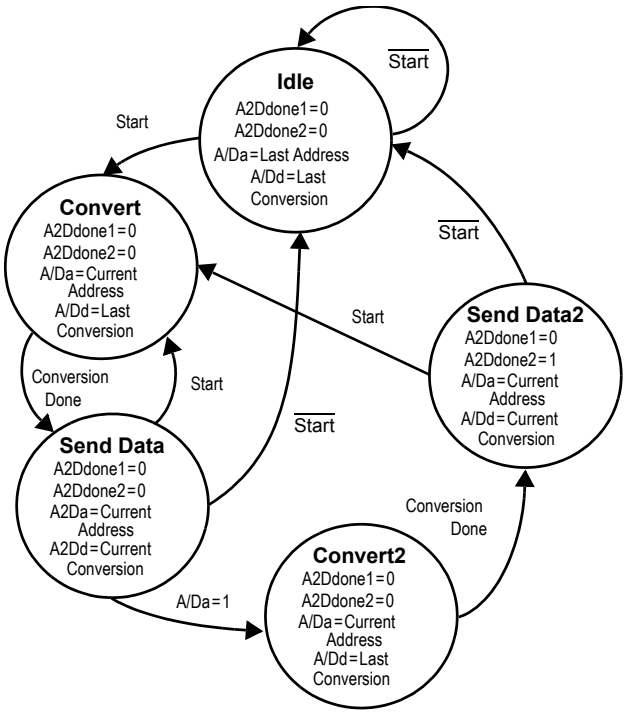
NORMAL Input Frame Bit 2	NORMAL Input Frame Bit 3	NORMAL Input Frame Bit 4	NORMAL Output Frame Bit 2[27]	NORMAL Output Frame Bit 3[27]	Input(s) Selected
A/Da0	A/Da1	A/Da2	DENCA	DENCB	
0	0	0	X	X	AN0/ANALOGOUT_A terminal
1	0	0	X	X	AN1/ANALOGOUT_B terminal
1	1	0	1	0	Analog encoder interface output A
1	1	0	0	1	Analog encoder interface output $\overline{A}$
1	1	0	1	1	Analog encoder interface output B
1	1	0	0	0	Analog encoder interface output $\overline{B}$
1	0	1	X	X	Analog encoder interface outputs A and $\overline{A}$ with S/H [28]
0	0	1	X	X	Analog encoder interface outputs A and B with S/H [28]
0	1	1	X	X	Analog encoder interface outputs B and $\overline{B}$ with S/H [28]
1	1	1	X	X	AN2/ANALOGIN_A and AN3/ANALOGIN_B terminals (direct input) with S/H [28]

Notes Notes

27. DENCA and DENCB values are captured at the output of the 3 or 6 Edge filter on SCLK rising edge, then immediately shifted out in the MISO data when $\overline{CE}$ is high.
28. Inputs are listed in order of conversion.

A/D Conversion Flow

There is a START conversion bit in the serial channel. The presence of this bit begins a conversion cycle on the input(s) selected in that frame. If the ADC is converting when a subsequent START bit arrives, this start request will be ignored. Figure 13, A/D Converter Input Structure, page 27, shows how this process works. The current conversion completes during the frame prior to the data being returned. If there is a START bit in that input frame, another conversion is begun as the previous conversion's data is being shifted out. If there is no START bit in the input frame, then another conversion is begun the frame following receipt of the start bit. The single conversion rate is paced at four frames for configuration bit 3 = 0 or eight frames (or less) for configuration bit 3 = 1, including sampling time (refer to Table 13, CONFIG Input Frame Bit Allocation, page 29). In order to simplify implementation of the 34921, the user must ensure that no A/D conversions are in progress when an INFO word is requested. For input pairs, the inputs are listed in the order of conversion in Table 7.



Note "Start" is bit 1 of the serial input normal frame.

A/D Converter Input Structure

The input impedance of a selected channel is an RC circuit. As shown in Figure 13, the input impedance of the selected channel is a resistor connected to the sample and hold (S/H) capacitor. The sample and hold time is $15 * t_{SCLK}$, or a minimum of 0.9285 µs. The tolerances of the internal S/H components are such that a time constant is about 93.6 ns. Therefore to achieve a proper level on the S/H capacitor (5*93.6 ns) = 0.468 µs, minimum, is required to satisfy internal component time constants. This only allows 460 ns for external time constants. Therefore, the maximum source impedance of the circuit driving the selected A/D channel is 7.8 kΩ when the SCLK speed matches the speed configuration bit.

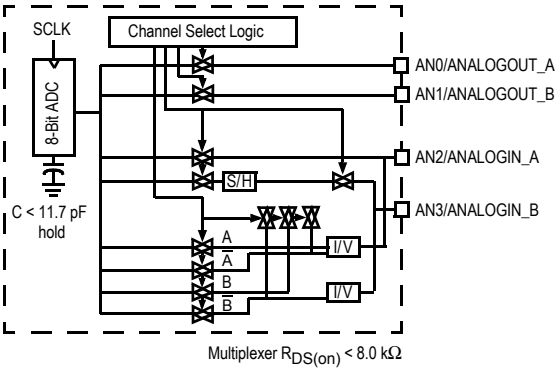


Figure 13. A/D Converter Input Structure

ADC Output Addressing

The return word to the digital subsystem also contains two conversion done bits, A/Ddone1 and A/Ddone2 (refer to Table 8). The A/Ddone1 bit is used for single conversions and the first conversion when input pairs are selected. The A/Ddone2 bit is used for the second conversion when input pairs are selected. A zero to one transition of these bits on successive return words indicates that a conversion cycle is complete and the data sent in that return word is valid for that conversion. The conversion done bits will only be asserted for one serial frame, although the data may be valid for multiple frames. The A/Dr bits indicate which A/D input is being reported when data is valid (refer to Table 9).

Table 8. A/D Done Bits

A/Ddone1	A/Ddone2	Return Data and A/Dr Value
Rising	0	Valid for single or first conversion
0	Rising	Valid for second conversion
0	0	Don't care

Table 9. A/D Channel of Current A/D Data

NORMAL Output Frame Bit 4	NORMAL Output Frame Bit 5	NORMAL Output Frame Bit 6	A/D Value Reported
A/Dr0	A/Dr1	A/Dr2	
0	0	1	A
1	0	1	B
0	1	1	A
1	1	1	B
0	0	0	AN0/ANALOGOUT_A
1	0	0	AN1/ANALOGOUT_B
0	1	0	AN2/ANALOGIN_A (direct input)
1	1	0	AN3/ANALOGIN_B (direct input)

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

NORMAL MODE:

Normal mode is the normal operating mode of the IC (as opposed to the Configuration mode or Information Request mode).

Table 10. NORMAL Mode Input Frame Programming Model

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OUT2	OUT1	$\overline{B}$	B	$\overline{A}$/Cdcb	A/Cdca	Adcb	Adca	Bdcb	Bdca	GATE OUT	A/Da2	A/Da1	A/Da0	start	config

Table 11. NORMAL Input Frame Bit Allocation [29]

Bit	Bit Name	Bit Description
15–14	OUT2, OUT1	High-side or low-side output control. Bit 4 of the configuration mode input frame determines which output is controlled. Output turns on when corresponding bit is asserted. Refer to Table 20 and Table 21 Truth Tables, page 31 and page 32, respectively, for operation.
13–10	$\overline{B}$, B, $\overline{A}$, A [31]	Step motor outputs, inverting. Corresponding output on when bit asserted. Refer to Table 22 Truth Table, page 32, for operation.
11–10	$\overline{A}$/Cdca, A/Cdcb [30]	Motor driver C direction bits. Outputs follow these bits, regardless of PWM value, when they are equal; i.e., 00 or 11. Refer to Table 19 Truth Table, page 31, for operation.
9–8	Adcb, Adca	Motor driver A direction bits. Outputs follow these bits, regardless of PWM value, when the are equal; i.e., 00 or 11. Refer to Table 19 Truth Table, page 31, for operation.
7–6	Bdcb, Bdca	Motor driver B direction bits. Outputs follow these bits, regardless of PWM value, when the are equal; i.e., 00 or 11. Refer to Table 19 Truth Table, page 31, for operation.
5	GATEOUT	Assertion puts V_b on the GATEOUT terminal. Deassertion connects the GATEOUT terminal to ground.
4–2	A/Da[2:0]	A/D conversion target channel. These bits determine which input(s) to the ADC are to be converted.
1	start	A/D conversion start bit. This bit causes the ADC to sample the input(s) specified by bits A/Da[2:0] (bits [4:2]) and begin an analog-to-digital conversion. This bit is ignored if a conversion is already in progress.
0	config	The input frame can be either a configuration frame or a normal frame. Bit 0 determines the type of frame being received. Bit 0 = 0 is a normal mode input frame.

Notes
29. All defaults = 0 at power up.
30. When in DC motor mode.
31. When in step motor mode, outputs are A, $\overline{A}$, B, and $\overline{B}$; when in DC motor mode, outputs B and $\overline{B}$ have no function.

CONFIG MODE:

Configuration mode is the mode in which the IC is programmed or configured by the external digital subsystem via the serial interface (i.e., MOSI, MISO, SCLK, CE).

Table 12. CONFIG Mode Input Frame Programming Model

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mtest1	Mtest0	cal4 (MSB)	cal3	cal2	cal1	cal0 (LSB)	ANALOG_TEST MODE	caladdr 1	caladdr 0	Filter	DC SS	A/D Speed	sleep	IREQ	config

Table 13. CONFIG Input Frame Bit Allocation [32]

Bit	Bit Name	Bit Description
15–14	Mtest[1:0]	Reserved for Freescale test. Set to [10].
13–9	cal[4:0]	Data for various calibration registers.
8	ANALOG_TEST MODE	Routes A and B output of analog encoder interface to AN0 and AN1, respectively. Used only for user development and verification. Do not use in normal operation.
7–6	caladdr[1:0]	Determines the calibration register, as identified in Table 14 below, the calibration data in the cal[4:0] (Bits 13–9) bits is latched in.
5	Filter	Determines the number of SCLK edges used to filter the DENCA and DENCB signals coming from the Digital Signal Generation stage of the analog encoder interface. This digital filter filters the DENCA and DENCB signals made available to the serial output frame.
4	DC SS	Determines if Motor Driver C operates in DC motor or step motor mode. Implicitly determines whether HSOUTx or LSOUTx are available. In DC motor mode, LSOUTx are available; in step motor mode, HSOUTx are available.
3	A/D Speed	Determines how many SCLK edges are required for conversion. This allows the use of a faster SCLK but still maintains A/D conversion accuracy.
2	sleep	When asserted, causes the 34921 to enter a power-down state, and minimize power consumption.
1	IREQ	Causes the next output frame sent to the host to contain internal information from the 34921.
0	config	The input frame can be either a configuration frame or a normal frame. Bit 0 determines the type of frame being received. Bit 0 = 1 is a configuration mode input frame.

Notes
32. All defaults = 0 at power up.

Table 14. Calibration Register Addressing

caladdr0	caladdr1	Register
0	0	Channel A gain
1	0	Channel A offset
0	1	Channel B gain
1	1	Channel B offset

Table 15. NORMAL Mode Output Frame Programming Model

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A/Dd7	A/Dd6	A/Dd5	A/Dd4	A/Dd3	A/Dd2	A/Dd1	A/Dd0	Info	A/Dr2	A/Dr1	A/Dr0	DENCB	DENCA	A/Ddone2	A/Ddone1

Table 16. NORMAL Mode Output Frame Bit Allocation Model

Bit	Bit Name	Bit Description
15–8	A/Dd[7:0]	ADC data from last conversion.
7	Info	Identifies the output frame as a normal or information frame. The type of output frame is determined by the IREQ bit (Bit 1) in the Configuration mode input frame.
6–4	A/Dr[2:0]	Report the input to the ADC that is represented in the A/Dd[7:0] (Bits 15–8).
3–2	DENCB, DENCA	Analog encoder interface digital signals. These signals are used to drive a quadrature encoder on the MCU.
1–0	A/Ddone2, A/Ddone1	Flag completion of the ADC for corresponding conversion. If ADC in single conversion mode, only A/Ddone1 is asserted. If in double conversion mode, A/Ddone1 is asserted for first conversion and A/Ddone2 is asserted for second conversion

NFO (IREQ) MODE:

NFO (IREQ) Mode is the mode in which the MC34921 IC reports status and error information via the serial interface.

Table 17. NFO (IREQ) Mode Output Frame Programming Model I

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	1	1	0	EXT	B+UV	Info	V5VUV	3.3UV	CoreUV	DENCB	DENCA	TSD	TW

Table 18. INFO (IREQ) Mode Output Frame Bit Allocation

Bit	Bit Name	Bit Description
15–10	Reserved	These bits will report [011000].
9	EXT	This flag will report if the last generated reset was due to an external signal driving $\overline{RST}$.
8	B+UV	Undervoltage flag for the B+ input voltage. If the input voltage drops below that necessary for the 34921 to operate, this flag will be asserted.
7	Info	Identifies the output frame as a normal or information frame. The type of output frame is determined by the IREQ bit (Bit 1) in the Configuration mode input frame.
6	V5VUV	Undervoltage warning for the 5.0 V regulator. This will be asserted when a fault on the 5.0 V causes the voltage to droop.
5	3.3UV	Undervoltage warning for the 3.3 V regulator. This will be asserted when a fault on the 3.3 V causes the voltage to droop.
4	CoreUV	Undervoltage warning for the VCORE linear regulator. This will be asserted when a fault on the VCORE voltage causes the voltage to droop.
3–2	DENCB, DENCA	Analog encoder interface digital signals. These signals are used to drive a quadrature encoder on the MCU.
1	TSD	Thermal shutdown flag. This flag will report if the last generated reset was due to a TSD. Thermal shutdown occurs when the junction temperature reaches approximately 140ºC.
0	TW	Thermal warning flag. This bit is asserted when the junction temperature on the die reaches approximately 110ºC.

LOGIC COMMANDS AND REGISTERS

Truth Tables use the following notations:

For inputs, I_{LIMIT} = 0 means TSD, I_{LIMIT} condition *not* encountered. I_{LIMIT} = 1 means TSD, I_{LIMIT} condition encountered.

For outputs XDCMA and XDCMB, 0 means low-side ON, 1 means high-side ON, Z means both OFF.

Table 19. DC Motors Truth Table

Inputs							Outputs	
Xdca	**Xdcb**	**XDCPWM**	**$\overline{RST}$**	**I_{LIMIT} Top**	**I_{LIMIT} Bottom**	**Thermal Shutdown (TSD)**	**XDCMA**	**XDCMB**
X	X	X	X	X	X	1	Z	Z
X	X	X	X	0	1	0	1	1
X	X	X	X	1	0	0	0	0
X	X	X	X	1	1	0	0	0
X	X	X	0	0	0	0	0	0
0	0	X	1	0	0	0	0	0
0	1	0	1	0	0	0	1	1
0	1	1	1	0	0	0	0	1
1	0	0	1	0	0	0	1	1
1	0	1	1	0	0	0	1	0
1	1	X	1	0	0	0	1	1

Table 20. Low-Side Out (LSOUT) Drivers Truth Table (Motor Driver Configured for H-bridge DC Motor)

Note The LSOUT terminals are controlled by the OUT1 and OUT2 signals (Bit 14 and Bit 15 in the NORMAL input frame). LSOUT is only available when Motor Driver C is configured as DC motor. (Set Bit 4 = 1 in CONFIG frame.)

Inputs							Output
Xdca	**Xdcb**	**XDCPWM**	**OUTx**	**$\overline{RST}$**	**I_{LIMIT} Output**	**TSD**	**LSOUTx**
X	X	X	X	X	X	1	OFF
X	X	X	X	0	X	0	OFF
X	X	X	0	1	0	0	OFF
X	X	X	1	1	0	0	ON
X	X	X	1	1	1	0	Limited

Table 21. High-Side Out (HSOUT) Drivers Truth Table (Motor Driver Configured for H-bridge DC Motor)

Note: The HSOUT terminals are controlled by the OUT1 and OUT2 signals (Bit 14 and Bit 15 in the NORMAL input frame). HSOUT is only available when DC motor is configured as Motor Driver C. (Set Bit 4 = 0 in CONFIG frame.)

Inputs							Output
Xdca	**Xdcb**	**XPWM**	**OUTx**	**$\overline{RST}$**	**I_{LIMIT} Output**	**TSD**	**HSOUTx**
X	X	X	X	X	X	1	OFF
X	X	X	X	0	X	0	OFF
X	X	X	0	1	0	0	OFF
X	X	X	1	1	0	0	ON
X	X	X	1	1	1	0	Limited

Table 22. Step Motor Driver Truth Table [33]

A or B Bit	$\overline{A}$ or $\overline{B}$ Bit	SPWMx Input	I_{LIMIT}	$\overline{RST}$	TSD	Output x	Output $\overline{x}$
X	X	X	X	X	1	OFF	OFF
X	X	X	X	0	0	OFF	OFF
X	X	X	1 [34]	1	0	Limited or OFF	Limited or OFF
0	0	X	0	1	0	OFF	OFF
0	1	0	0	1	0	ON	OFF
0	1	1	0	1	0	OFF	ON
1	0	0	0	1	0	OFF	ON
1	0	1	0	1	0	ON	OFF
1	1	X	0	1	0	OFF	OFF

Notes

33. To reduce parasitic dissipation associated with the body diode, the counterphase is turned on for synchronous rectification.
34. The current limit sense function may be disabled when the outputs are disabled. Hence, the output will oscillate between the requested state from the Truth Table and this state.

TYPICAL APPLICATIONS

In typical applications such as a personal computer printer, the MC34921 would supply the motor drive and control for two bi-directional dc motors, two unidirectional dc motors, and one unipolar stepper motor. In addition, the MC34921 would supply the power management for the printer including: the system MCU core voltage, the 3.3V logic supply, and the 5V logic supply. The MC34921 also would supply the system with the means to read and pre-process the carriage position information from an analog optical encoder.

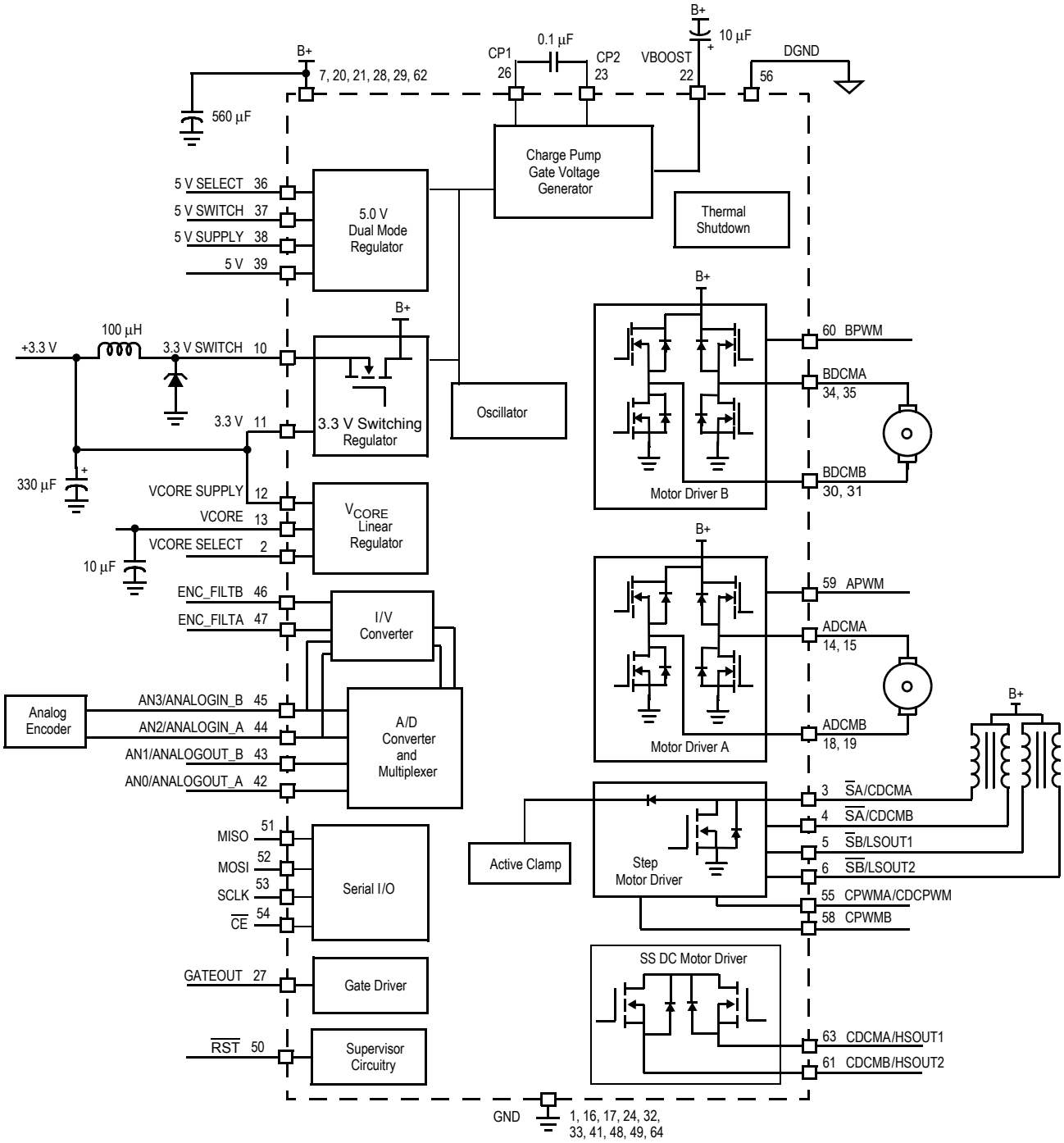
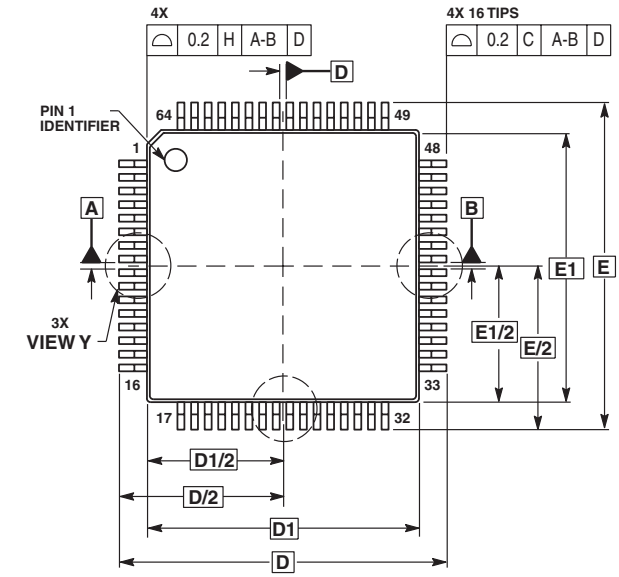
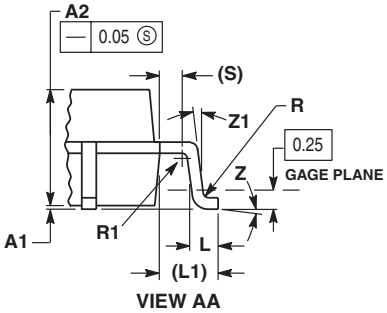


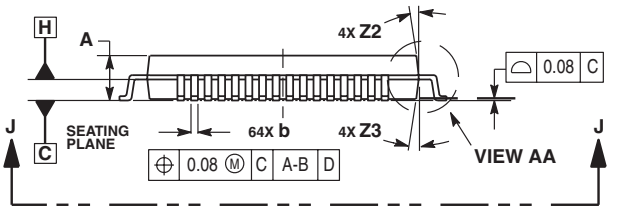
Figure 14. TYPICAL APPLICATION DIAGRAM

PACKAGE DIMENSIONS

For the most current revision of the package, visit www.freescale.com and do a keyword search using the 98A number for the specific device related to the data sheet.

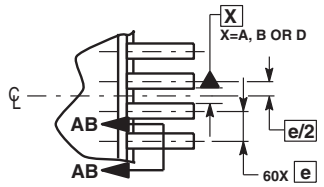




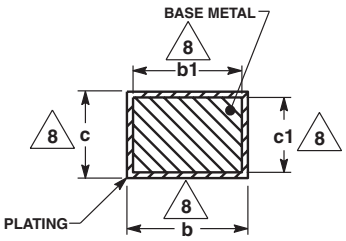


NOTES:
1. DIMENSIONS ARE IN INCHES.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUMS A, B AND D TO BE DETERMINED AT SEATING PLANE C.
4. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 mm.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZED DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.

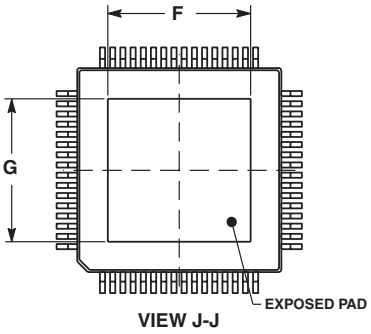
	MILLIMETERS	
DIM	MIN	MAX
A	---	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.17	0.27
b1	0.17	0.23
c	0.09	0.20
c1	0.09	0.16
D	12.00 BSC	
D1	10.00 BSC	
e	0.50 BSC	
E	12.00 BSC	
E1	10.00 BSC	
L	0.45	0.75
L1	1.00 REF	
R1	0.08	---
R2	0.08	---
S	0.20	---
F	6.00	7.00
G	6.00	7.00
Z	0°	7°
Z1	0°	---
Z2	11°	13°
Z3	11°	13°



VIEW Y



SECTION AB-AB
ROTATED 90° CLOCKWISE



VIEW J-J

AE SUFFIX (Pb FREE)
64-TERMINAL LQFP EXPOSED PAD
PLASTIC PACKAGE
98ARH98426A
ISSUE 0

NOTES

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