agere systems

Data Sheet, Rev. 1
August 2001

NetLight ® 2417J4A 1300 nm Laser Gigabit Transceiver

Available in a small form-factor, RJ-45 size, plastic package, the 2417J4A Transceiver is a high-performance, cost-effective optical transceiver for Gigabit Ethernet 1000Base-LX applications.

Features

- Gigabit Ethernet 1000Base-LX compliant
- Small form factor (SFF), RJ-45 size, multisourced 10-pin package
- LC duplex receptacle
- Uncooled 1300 nm laser transmitter with automatic output power control
- Transmitter disable input
- Wide dynamic range receiver with InGaAs PIN photodetector
- TTL signal-detect output
- Low power dissipation
- Single 3.3 V power supply
- Raised ECL (LVPECL) logic data interfaces
- Operating temperature range: 0 °C to 70 °C
- Agere Systems Inc. Reliability and Qualification Program for built-in quality and reliability

Description

The 2417J4A transceiver is a high-speed, cost-effective optical transceiver that is compliant with the *IEEE*® 802.3z Gigabit Ethernet Physical Medium Dependent (PMD) 1000Base-LX specifications using a long-wavelength laser. The transceiver features the latest generation of Agere Systems optics and is packaged in a narrow-width plastic housing with an LC duplex receptacle. This receptacle fits into an RJ-45 form-factor outline. The 10-pin package and pinout conform to a multisource transceiver agreement.

The transmitter features differential LVPECL logic level data inputs and an LVTTL logic level disable input. The receiver features differential LVPECL logic level data outputs and an LVTTL logic level signal-detect output.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	0	3.6	V
Operating Temperature Range	T_C	0	70	°C
Storage Case Temperature Range	T_{stg}	–40	85	°C
Lead Soldering Temperature/Time	—	—	250/10	°C/s
Operating Wavelength Range	λ	1.1	1.6	µm

Pin Information

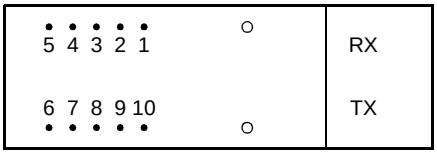

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Figure 1. 2417J4A Transceiver, 10-Pin Configuration, Top View

Table 1. Transceiver Pin Descriptions

Pin Number	Symbol	Name/Description	Logic Family
Receiver			
MS	MS	**Mounting Studs.** The mounting studs are provided for transceiver mechanical attachment to the circuit board. They may also provide an optional connection of the transceiver to the equipment chassis ground.	NA
1	V_{EER}	**Receiver Signal Ground**.	NA
2	V_{CCR}	**Receiver Power Supply.**	NA
3	SD	**Signal Detect.** Normal operation: logic one output. Fault condition: logic zero output.	LVTTL
4	RD–	**Received $\overline{\text{DATA}}$ Out.**	LVPECL
5	RD+	**Received DATA Out.**	LVPECL
Transmitter			
6	V_{CCT}	**Transmitter Power Supply.**	NA
7	V_{EET}	**Transmitter Signal Ground**.	NA
8	T_{DIS}	**Transmitter Disable.**	LVTTL
9	TD+	**Transmitter DATA In.** An internal termination is provided, consisting of a 100 Ω resistor between the TD+ and TD– pins.	LVPECL
10	TD–	**Transmitter $\overline{\text{DATA}}$ In.** See TD+ pin for terminations.	LVPECL

Electrostatic Discharge

Caution: This device is susceptible to damage as a result of electrostatic discharge (ESD). Take proper precautions during both handling and testing. Follow *EIA*® Standard *EIA*-625.

Although protection circuitry is designed into the device, take proper precautions to avoid exposure to ESD.

Agere Systems employs a human-body model (HBM) for ESD susceptibility testing and protection-design evaluation. ESD voltage thresholds are dependent on the critical parameters used to define the model. A standard HBM (resistance = 1.5 kΩ, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes. The HBM ESD threshold established for the 2417J4A is ±1500 V.

Application Information

The 2417 receiver section is a highly sensitive fiber-optic receiver. Although the data outputs are digital logic levels (PECL), the device should be thought of as an analog component. When laying out system application boards, the 2417 transceiver should receive the same type of consideration one would give to a sensitive analog component.

Printed-Wiring Board Layout Considerations

A fiber-optic receiver employs a very high gain, wide bandwidth transimpedance amplifier. This amplifier detects and amplifies signals that are only tens of nA in amplitude when the receiver is operating near its sensitivity limit. Any unwanted signal currents that couple into the receiver circuitry cause a decrease in the receiver's sensitivity and can also degrade the performance of the receiver's signal detect (SD) circuit. To minimize the coupling of unwanted noise into the receiver, careful attention must be given to the printed-wiring board layout.

At a minimum, a double-sided printed-wiring board (PWB) with a large component-side ground plane beneath the transceiver must be used. In applications that include many other high-speed devices, a multilayer PWB is highly recommended. This permits the placement of power and ground on separate layers, which allows them to be isolated from the signal lines. Multilayer construction also permits the routing of sensitive signal traces away from high-level, high-speed signal lines. To minimize the possibility of coupling noise into the receiver section, high-level, high-speed signals such as transmitter inputs and clock lines should be routed as far away as possible from the receiver pins.

Noise that couples into the receiver through the power supply pins can also degrade performance. It is recommended that the pi filter, shown in Figure 2, be used for both the transmitter and receiver power supplies.

Data and Signal Detect Outputs

The data and signal detect outputs of the 2417 transceiver are driven by open-emitter NPN transistors, which have an output impedance of approximately 7 Ω. Each output can provide approximately 50 mA maximum current to a 50 Ω load terminated to V_{CC} – 2.0 V.

Due to the high switching speeds of ECL outputs, transmission line design must be used to interconnect components. To ensure optimum signal fidelity, both data outputs (RD+/RD–) should be terminated identically. The signal lines connecting the data outputs to the next device should be equal in length and have matched impedances. Controlled impedance stripline or microstrip construction must be used to preserve the quality of the signal into the next component and to minimize reflections back into the receiver, which could degrade its performance. Excessive ringing due to reflections caused by improperly terminated signal lines makes it difficult for the component receiving these signals to decipher the proper logic levels and can cause transitions to occur where none were intended. Also, by minimizing high-frequency ringing, possible EMI problems can be avoided.

The signal-detect output is positive LVTTL logic. A logic low at this output indicates that the optical signal into the receiver has been interrupted or that the light level has fallen below the minimum signal detect threshold. This output should not be used as an error rate indicator since its switching threshold is determined only by the magnitude of the incoming optical signal.

Application Information (continued)

Transceiver Processing

When the process plug is placed in the transceiver's optical port, the transceiver and plug can withstand normal wave soldering and aqueous spray cleaning processes. However, the transceiver is not hermetic, and should not be subjected to immersion in cleaning solvents. The transceiver case should not be exposed to temperatures in excess of 125 °C. The transceiver pins can be wave soldered at 250 °C for up to 10 seconds. The process plug should only be used once. After removing the process plug from the transceiver, it must not be used again as a process plug; however, if it has not been contaminated, it can be reused as a dust cover.

Transceiver Optical and Electrical Characteristics

Table 2. Transmitter Optical and Electrical Characteristics (T_A = 0 °C to 70 °C; V_{CC} = 3.135 V—3.465 V)

Parameter	Symbol	Min	Max	Unit
Average Optical Output Power (EOL): Single-mode Fiber (10 μm)	P_O	 –11.0	 –3.0	 dBm
Optical Wavelength	λ_C	1270	1355	nm
Spectral Width	$\Delta\lambda_{RMS}$	—	4	nm
Dynamic Extinction Ratio	EXT	9	—	dB
Rise/Fall Time,20%—80%	t_R,t_F	—	260	ps
Output Optical Eye	Compliant with *IEEE* 802.3Z Eye Mask requirements			
Power Supply Current	I_{CCT}	—	150	mA
Input Data Voltage: Low High	 V_{IL} V_{IH}	 V_{CC} – 2.0 V_{CC} – 1.2	 V_{CC} – 1.6 V_{CC} – 0.8	 V V
Transmit Disable Voltage	V_D	V_{CC} – 1.3	V_{CC}	V
Transmit Enable Voltage	V_{EN}	V_{EE}	V_{EE} + 0.8	V

Table 3. Receiver Optical and Electrical Characteristics (T_A = 0 °C to 70 °C; V_{CC} = 3.135 V—3.465 V)

Parameter	Symbol	Min	Max	Unit
Average Sensitivity*	P_I	–19	—	dBm
Maximum Input Power*	P_{MAX}	—	–3	dBm
Return Loss	—	12	—	dB
Link Status Switching Threshold: Decreasing Light Increasing Light	 LST_D LST_I	 — —	 –20.5 –20.0	 dBm dBm
Link Status Hysteresis	HYS	0.5	—	dB
Power Supply Current	I_{CCR}	—	100	mA
Output Data Voltage/Clock Voltage: Low High	 V_{OL} V_{OH}	 V_{CC} – 1.81 V_{CC} – 1.025	 V_{CC} – 1.62 V_{CC} – 0.88	 V V
Signal-detect Voltage: Low High	 V_{OL} V_{OH}	 0.0 2.4	 0.8 V_{CC}	 V V

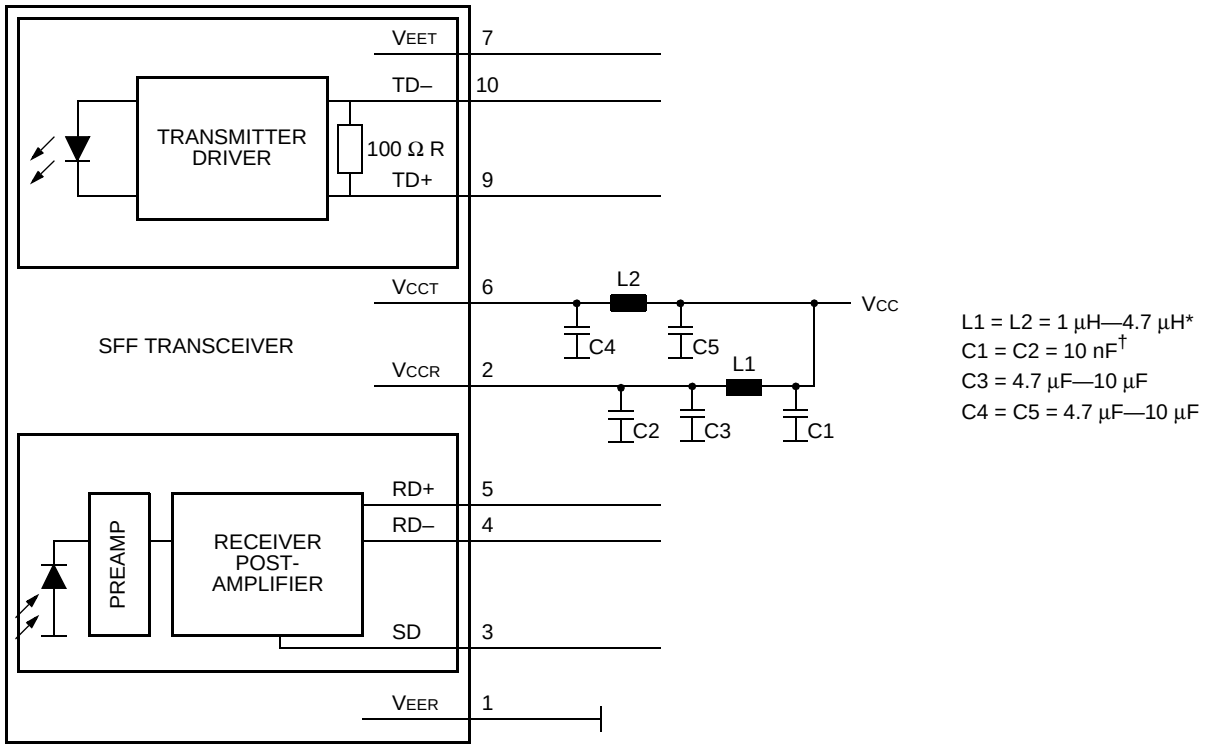
* For 1 x 10^{-10} BER with an optical input using 2^{23} – 1 PRBS.

Qualification and Reliability

To help ensure high product reliability and customer satisfaction, Agere Systems is committed to an intensive quality program that starts in the design phase and proceeds through the manufacturing process. Optoelectronic modules are qualified to Agere Systems internal standards using MIL-STD-883 test methods and procedures and using sampling techniques consistent with *Telcordia Technologies*® requirements. The 2417 transceiver is required to pass an extensive and rigorous set of qualification tests.

In addition, the design, development, and manufacturing facilities ofthe Agere Systems Optoelectronics unit have been certified to be in full compliance with the latest *ISO*® 9001 quality system standards.

Electrical Schematic



* Ferrite beads can be used as an option.
† For all capacitors, MLC caps are recommended.

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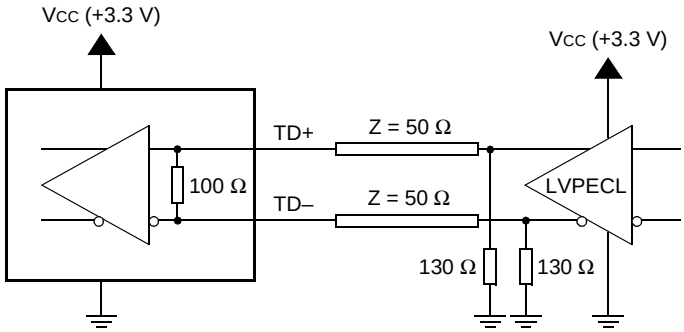
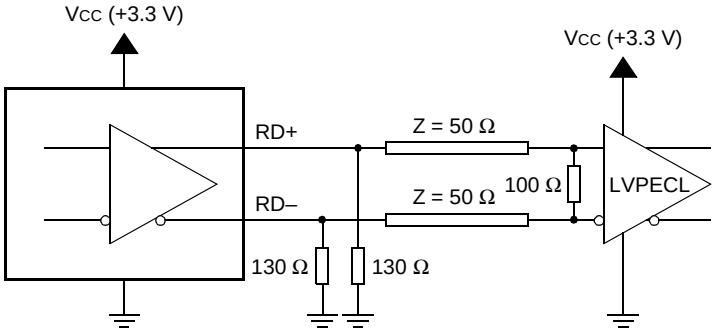
Figure 2. Power Supply Filtering for the Small Form Factor Transceiver

Application Schematics



(A) TRANSMITTER INTERFACE (LVPECL TO LVPECL)



(B) RECEIVER INTERFACE (LVPECL TO LVPECL)

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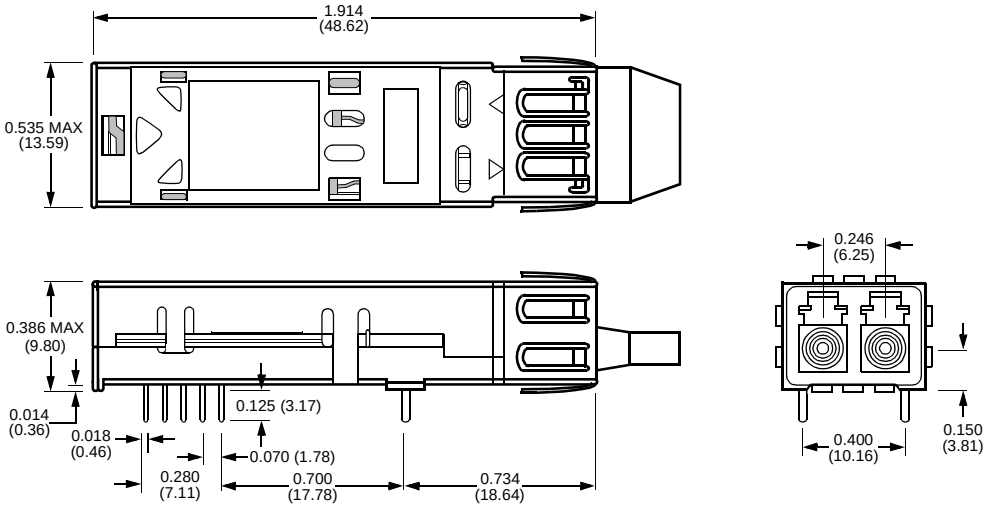
Figure 3. 3.3 V Transceiver Interface with 3.3 V ICs

Outline Diagrams

Dimensions are in inches and (millimeters).

Package Outline



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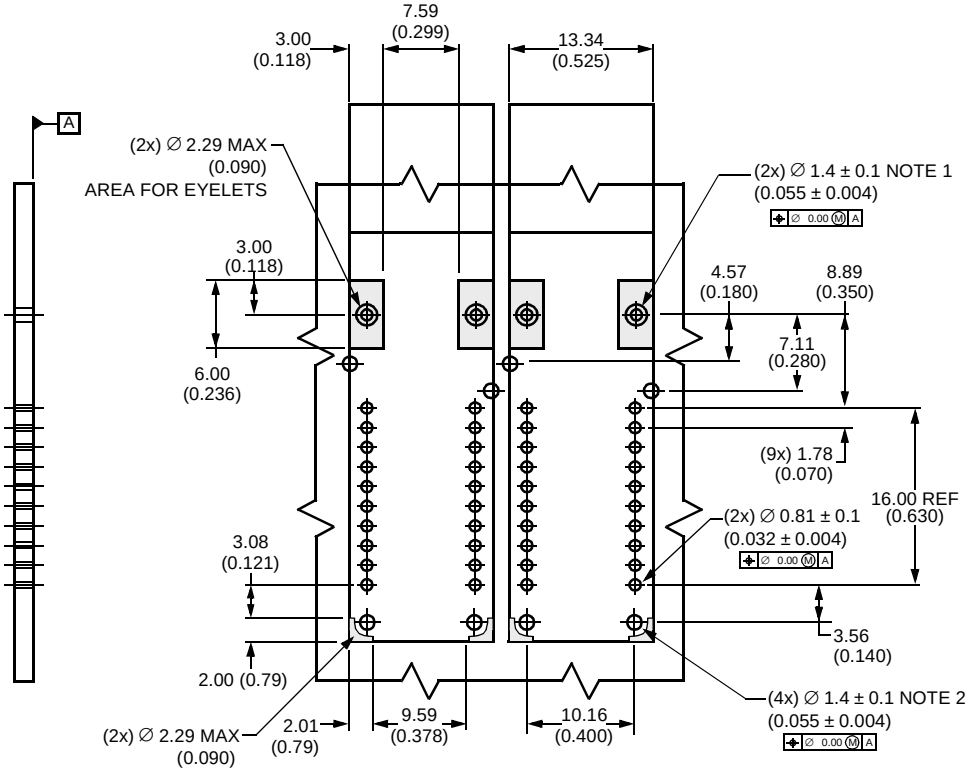
Outline Diagrams (continued)

Printed-Wiring Board Layout *, †

Dimensions are in inches and (millimeters).



NOTES:
1. HOLES FOR MOUNTING STUDS MUST BE TIED TO CHASSIS GROUND.
2. HOLES FOR HOUSING LEADS MUST BE TIED TO SIGNAL GROUND.

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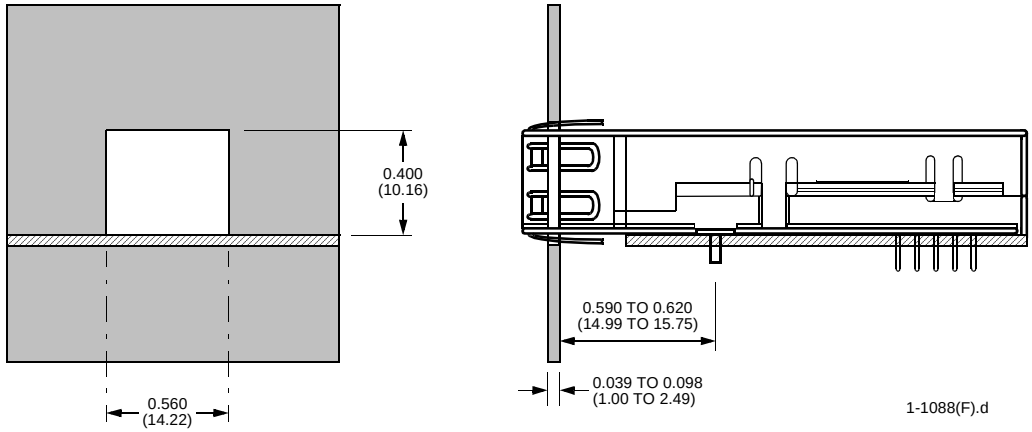
* The hatched areas are keep-out areas reserved for housing standoffs. No metal traces of ground connection in keep-out area.
† Twenty-pin module shown; 10-pin module requires only 16 PWB holes.

Outline Diagrams (continued)

Recommended Panel Opening

Dimensions are in inches and (millimeters).



Laser Safety Information

Class I Laser Product

FDA/CDRH Class 1 laser product. All versions of the transceiver are Class I laser products per CDRH, 21 CFR 1040 Laser Safety requirements. All versions are Class I laser products per *IEC*® 60825-1:1993. The transceiver has been certified with the FDA under accession number 9520668.

CAUTION: Use of controls, adjustments, and procedures other than those specified herein may result in hazardous laser radiation exposure.

This product complies with 21 CFR 1040.10 and 1040.11.
Wavelength = 1.3 µm
Maximum power = 1.0 mW

Because of size constraints, laser safety labeling is not affixed to the module but is attached to the outside of the shipping carton.

Product is not shipped with power supply.

NOTICE

Unterminated optical receptacles may emit laser radiation.

Do not view with optical instruments.

Ordering Information

Description	Device Code	Comcode
2 x 5 Single-mode SFF LC Receptacle Transceiver for 1000Base-LX Applications	2417J4A	108282229

For additional information, contact your Agere Systems Account Manager or the following:
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