2N7002L

Small Signal MOSFET

60 V, 115 mA, N−Channel SOT−23

ON Semiconductor®

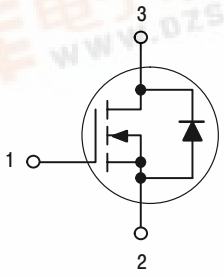
http://onsemi.com

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
60 V	7.5 Ω @ 10 V, 500 mA	115 mA

Features

- Pb−Free Packages are Available

N−Channel



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain−Source Voltage	V_{DSS}	60	Vdc
Drain−Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Drain Current − Continuous T_C = 25°C (Note 1) T_C = 100°C (Note 1) − Pulsed (Note 2)	I_D I_D I_{DM}	±115 ±75 ±800	mAdc
Gate−Source Voltage − Continuous − Non−repetitive ($t_p \le 50$ μs)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk

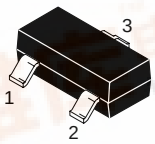
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

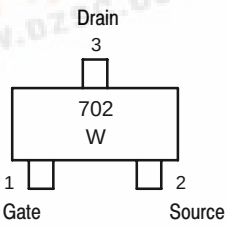
Characteristic	Symbol	Max	Unit
Total Device Dissipation FR−5 Board (Note 3) T_A = 25°C Derate above 25°C	P_D	225 1.8	mW mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	556	°C/W
Total Device Dissipation Alumina Substrate,(Note 4) T_A = 25°C Derate above 25°C	P_D	300 2.4	mW mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	417	°C/W
Junction and Storage Temperature	T_J, T_{stg}	−55 to +150	°C

1. The Power Dissipation of the package may result in a lower continuous drain current.
2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
3. FR−5 = 1.0 x 0.75 x 0.062 in.
4. Alumina = 0.4 x 0.3 x 0.025 in 99.5% alumina.

MARKING DIAGRAM & PIN ASSIGNMENT



SOT−23
CASE 318
STYLE 21



702 = Device Code
W = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
2N7002LT1	SOT−23	3000 Tape & Reel
2N7002LT3		10,000 Tape & Reel
2N7002LT1G	SOT−23 (Pb−free)	3000 Tape & Reel
2N7002LT3G		10,000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−Source Breakdown Voltage (V_{GS} = 0, I_D = 10 μAdc)		$V_{(BR)DSS}$	60	−	−	Vdc
Zero Gate Voltage Drain Current (V_{GS} = 0, V_{DS} = 60 Vdc)	T_J = 25°C T_J = 125°C	I_{DSS}	− −	− −	1.0 500	μAdc
Gate−Body Leakage Current, Forward (V_{GS} = 20 Vdc)		I_{GSSF}	−	−	100	nAdc
Gate−Body Leakage Current, Reverse (V_{GS} = −20 Vdc)		I_{GSSR}	−	−	−100	nAdc
ON CHARACTERISTICS (Note 5)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	1.0	−	2.5	Vdc
On−State Drain Current (V_{DS} ≥ 2.0 $V_{DS(on)}$, V_{GS} = 10 Vdc)		$I_{D(on)}$	500	−	−	mA
Static Drain−Source On−State Voltage (V_{GS} = 10 Vdc, I_D = 500 mAdc) (V_{GS} = 5.0 Vdc, I_D = 50 mAdc)		$V_{DS(on)}$	 − −	 − −	 3.75 0.375	Vdc
Static Drain−Source On−State Resistance (V_{GS} = 10 V, I_D = 500 mAdc) (V_{GS} = 5.0 Vdc, I_D = 50 mAdc)	 T_C = 25°C T_C = 125°C T_C = 25°C T_C = 125°C	$r_{DS(on)}$	 − − − −	 − − − −	 7.5 13.5 7.5 13.5	Ohms
Forward Transconductance (V_{DS} ≥ 2.0 $V_{DS(on)}$, I_D = 200 mAdc)		g_{FS}	80	−	−	mmhos
DYNAMIC CHARACTERISTICS						
Input Capacitance (V_{DS} = 25 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	−	−	50	pF
Output Capacitance (V_{DS} = 25 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{oss}	−	−	25	pF
Reverse Transfer Capacitance (V_{DS} = 25 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	−	−	5.0	pF
SWITCHING CHARACTERISTICS (Note 5)						
Turn−On Delay Time	(V_{DD} = 25 Vdc, I_D ≅ 500 mAdc, R_G = 25 Ω, R_L = 50 Ω, V_{gen} = 10 V)	$t_{d(on)}$	−	−	20	ns
Turn−Off Delay Time		$t_{d(off)}$	−	−	40	ns
BODY−DRAIN DIODE RATINGS						
Diode Forward On−Voltage (I_S = 11.5 mAdc, V_{GS} = 0 V)		V_{SD}	−	−	−1.5	Vdc
Source Current Continuous (Body Diode)		I_S	−	−	−115	mAdc
Source Current Pulsed		I_{SM}	−	−	−800	mAdc

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL ELECTRICAL CHARACTERISTICS

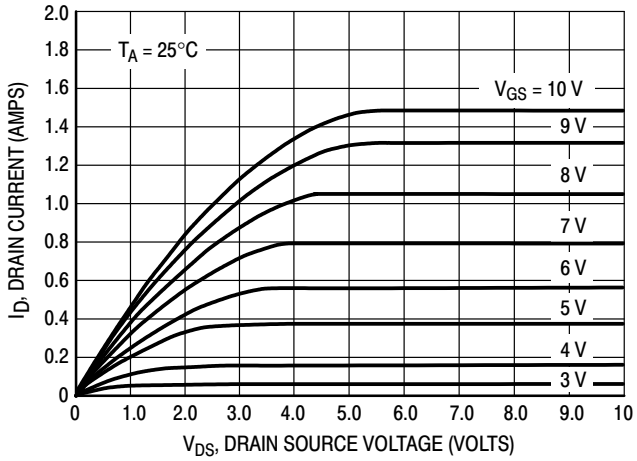


Figure 1. Ohmic Region

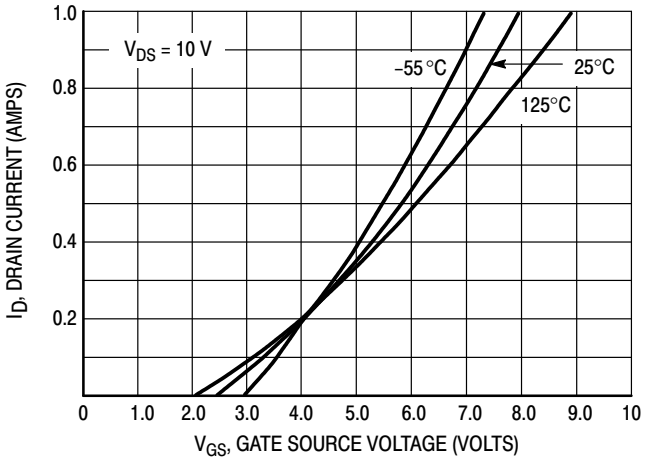


Figure 2. Transfer Characteristics

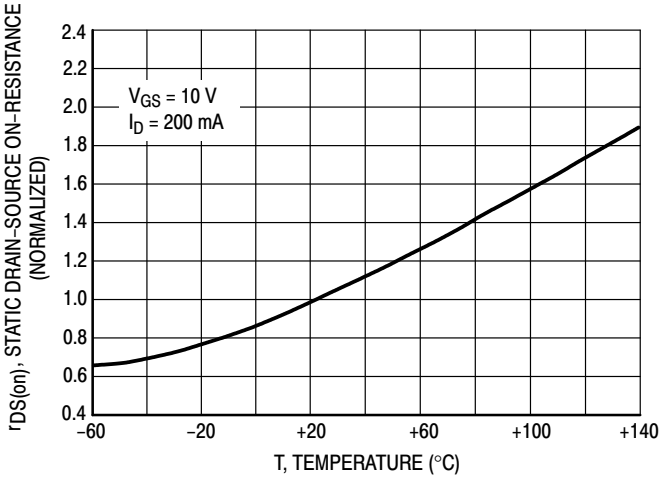


Figure 3. Temperature versus Static Drain−Source On−Resistance

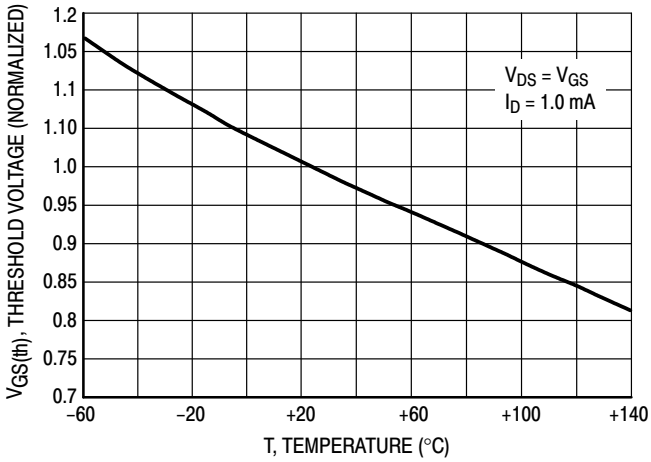
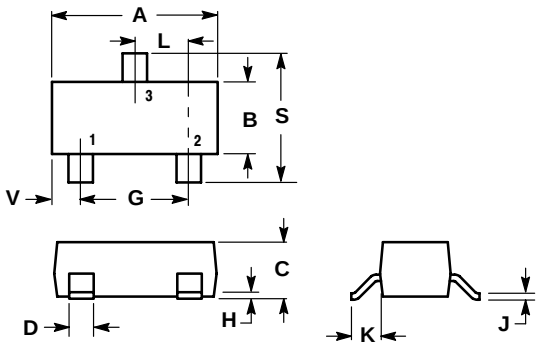


Figure 4. Temperature versus Gate Threshold Voltage

2N7002L

PACKAGE DIMENSIONS

SOT−23 (TO−236)
CASE 318−08
ISSUE AH

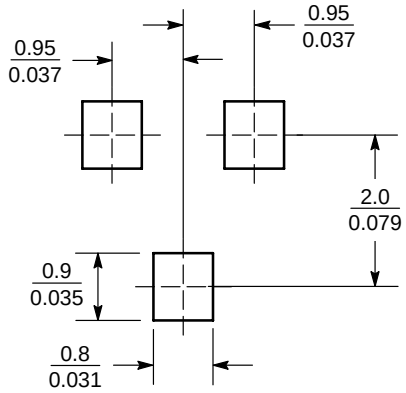


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318−03 AND −07 OBSOLETE, NEW STANDARD 318−08.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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