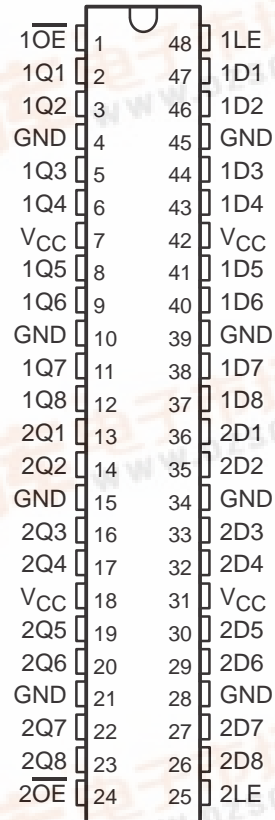


SN54ABT16373A, SN74ABT16373A 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS160C – DECEMBER 1992 – REVISED MAY 1997

- **Members of the Texas Instruments Widebus™ Family**
- **State-of-the-Art EPIC-II B™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 5 V, T_A = 25^\circ C$**
- **High-Impedance State During Power Up and Power Down**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs ($-32\text{-mA } I_{OH}, 64\text{-mA } I_{OL}$)**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54ABT16373A . . . WD PACKAGE
SN74ABT16373A . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'ABT16373A are 16-bit transparent D-type latches with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

\overline{OE} does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16373A is characterized for operation over the full military temperature range of $-55^\circ C$ to $125^\circ C$. The SN74ABT16373A is characterized for operation from $-40^\circ C$ to $85^\circ C$.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus and EPIC-II B are trademarks of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1997, Texas Instruments Incorporated



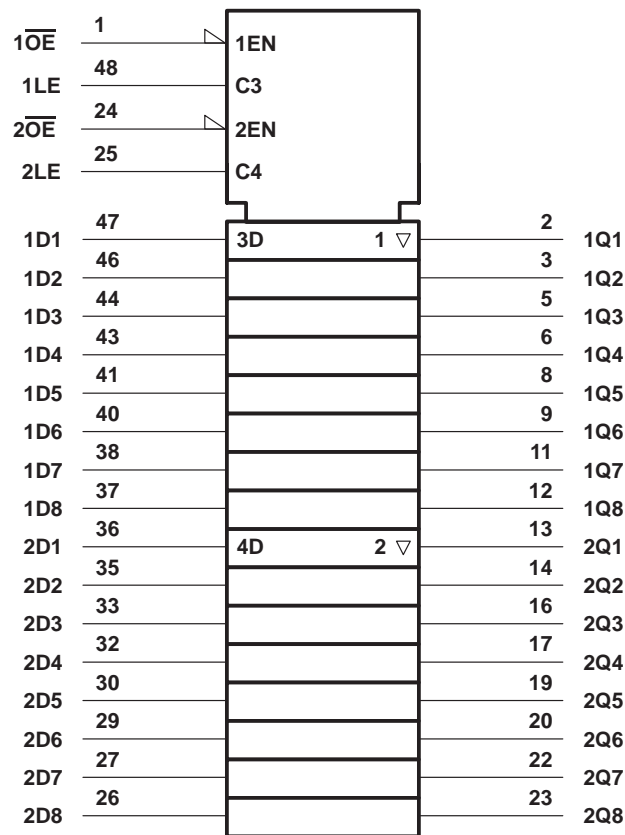
SN54ABT16373A, SN74ABT16373A 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS160C – DECEMBER 1992 – REVISED MAY 1997

FUNCTION TABLE
(each 8-bit section)

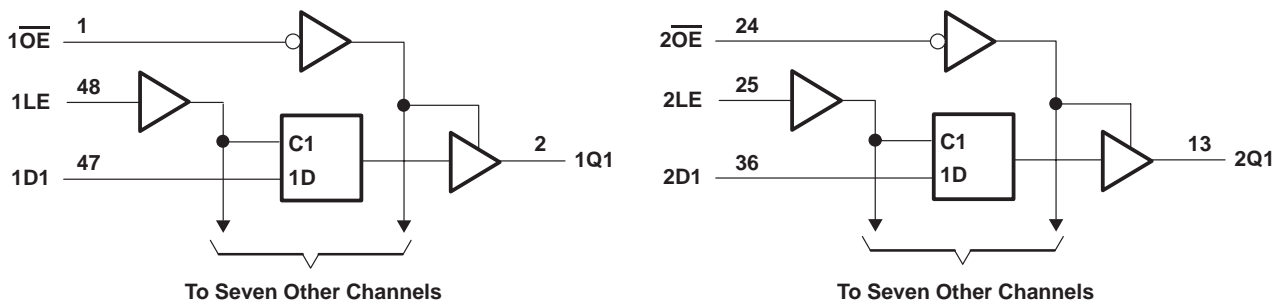
INPUTS			OUTPUT
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54ABT16373A, SN74ABT16373A 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS160C – DECEMBER 1992 – REVISED MAY 1997

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT16373A	96 mA
SN74ABT16373A	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

		SN54ABT16373A		SN74ABT16373A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
	Outputs enabled					
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μ s/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

SN54ABT16373A, SN74ABT16373A 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS160C – DECEMBER 1992 – REVISED MAY 1997

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54ABT16373A		SN74ABT16373A		UNIT	
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2		-1.2		-1.2	V	
V_{OH}	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -3\text{ mA}$	2.5			2.5		2.5		V	
	$V_{CC} = 5\text{ V}$, $I_{OH} = -3\text{ mA}$	3			3		3			
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -24\text{ mA}$	2			2				
		$I_{OH} = -32\text{ mA}$	2*					2		
V_{OL}	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 48\text{ mA}$		0.55		0.55			V	
		$I_{OL} = 64\text{ mA}$		0.55*				0.55		
V_{hys}			100						mV	
I_I	$V_{CC} = 0\text{ to }5.5\text{ V}$, $V_I = V_{CC}\text{ or GND}$			± 1		± 1		± 1	μA	
I_{OZPU}^\ddagger	$V_{CC} = 0\text{ to }2.1\text{ V}$, $V_O = 0.5\text{ V to }2.7\text{ V}$, $\overline{OE} = X$			± 50		± 50		± 50	μA	
I_{OZPD}^\ddagger	$V_{CC} = 2.1\text{ V to }0$, $V_O = 0.5\text{ V to }2.7\text{ V}$, $\overline{OE} = X$			± 50		± 50		± 50	μA	
I_{OZH}	$V_{CC} = 2.1\text{ V to }5.5\text{ V}$, $V_O = 2.7\text{ V}$, $\overline{OE} \geq 2\text{ V}$			10		10		10	μA	
I_{OZL}	$V_{CC} = 2.1\text{ V to }5.5\text{ V}$, $V_O = 0.5\text{ V}$, $\overline{OE} \geq 2\text{ V}$			-10		-10		-10	μA	
I_{off}	$V_{CC} = 0$, V_I or $V_O \leq 4.5\text{ V}$			± 100				± 100	μA	
I_{CEX}	Outputs high $V_{CC} = 5.5\text{ V}$, $V_O = 5.5\text{ V}$			50		50		50	μA	
I_O^\S	Outputs low $V_{CC} = 5.5\text{ V}$, $V_O = 2.5\text{ V}$	-50	-100	-180	-50	-180	-50	-180	mA	
I_{CC}	Outputs high			2		2		2	mA	
	Outputs low			85		85		85		
	Outputs disabled			2		2		2		
ΔI_{CC}^\parallel	$V_{CC} = 5.5\text{ V}$, One input at 3.4 V, Other inputs at V_{CC} or GND			1.5		1.5		1.5	mA	
C_i	$V_I = 2.5\text{ V or }0.5\text{ V}$			3.5					pF	
C_o	$V_O = 2.5\text{ V or }0.5\text{ V}$			9.5					pF	

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at $V_{CC} = 5\text{ V}$.

‡ This parameter is characterized, but not production tested.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}^\#$		SN54ABT16373A		SN74ABT16373A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	3.3		3.3		3.3		ns
t_{su}	Setup time, data before LE↓	1.5		2.4		1.5		ns
t_h	Hold time, data after LE↓	1		2.2		1		ns

These values apply only to the SN74ABT16373A.

SN54ABT16373A, SN74ABT16373A
16-BIT TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

SCBS160C – DECEMBER 1992 – REVISED MAY 1997

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT16373A					UNIT
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN	MAX	
			MIN	TYP	MAX			
t_{PLH}	D	Q	1.4	3.7	5.3	1.4	6.5	ns
t_{PHL}			2	4	5.4	2	6.5	
t_{PLH}	LE	Q	1.7	4.1	5.7	1.7	7	ns
t_{PHL}			2.3	4.3	5.6	2.3	6.3	
t_{PZH}	\overline{OE}	Q	1.1	3.4	5	1.1	6.4	ns
t_{PZL}			1.5	3.5	4.9	1.5	5.8	
t_{PHZ}	\overline{OE}	Q	2.4	5.1	7.1	2.4	8.3	ns
t_{PLZ}			1.6	4.4	6.3	1.6	8	

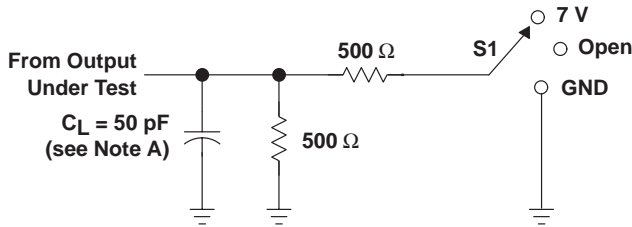
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT16373A					UNIT
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN	MAX	
			MIN	TYP	MAX			
t_{PLH}	D	Q	1.4	3.7	5.3	1.4	6.3	ns
t_{PHL}			2	4	5.4	2	6.2	
t_{PLH}	LE	Q	1.7	4.1	5.7	1.7	6.7	ns
t_{PHL}			2.3	4.3	5.6	2.3	6.1	
t_{PZH}	\overline{OE}	Q	1.1	3.4	5	1.1	6.1	ns
t_{PZL}			1.5	3.5	4.9	1.5	5.6	
t_{PHZ}	\overline{OE}	Q	2.4	5.1	7.1	2.4	8.1	ns
t_{PLZ}			1.6	4.4	5.8	1.6	6.5	

SN54ABT16373A, SN74ABT16373A 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

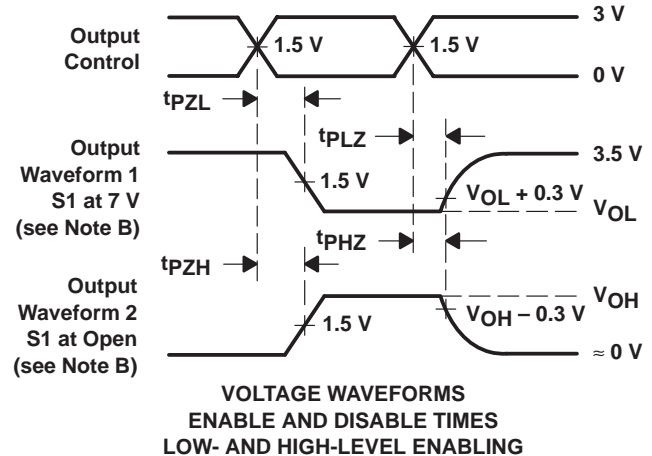
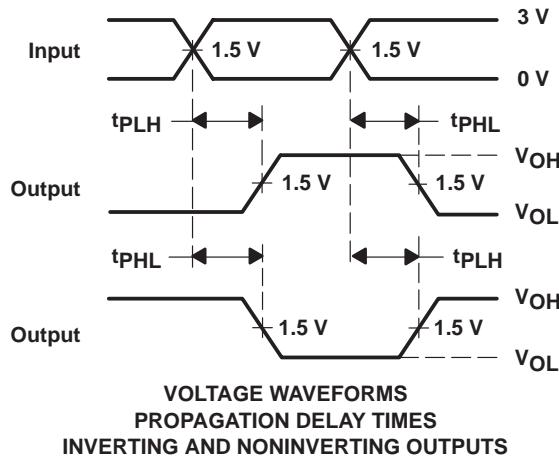
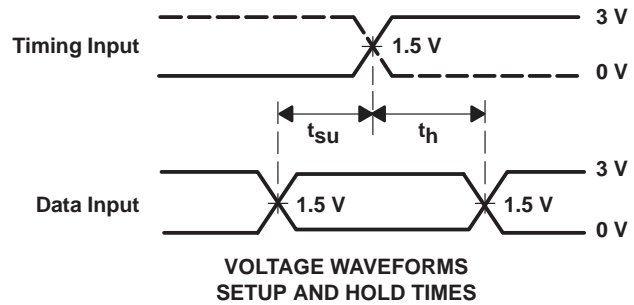
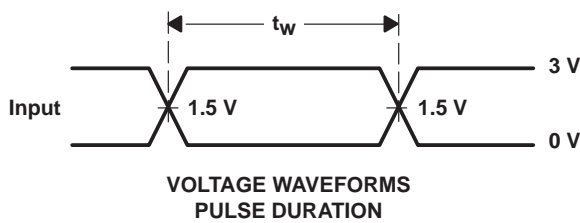
SCBS160C – DECEMBER 1992 – REVISED MAY 1997

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9320001QXA	ACTIVE	CFP	WD	48	1	TBD	Call TI	Level-NC-NC-NC
74ABT16373ADGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16373ADGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16373ADL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16373ADLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16373ADLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54ABT16373AWD	ACTIVE	CFP	WD	48	1	TBD	Call TI	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

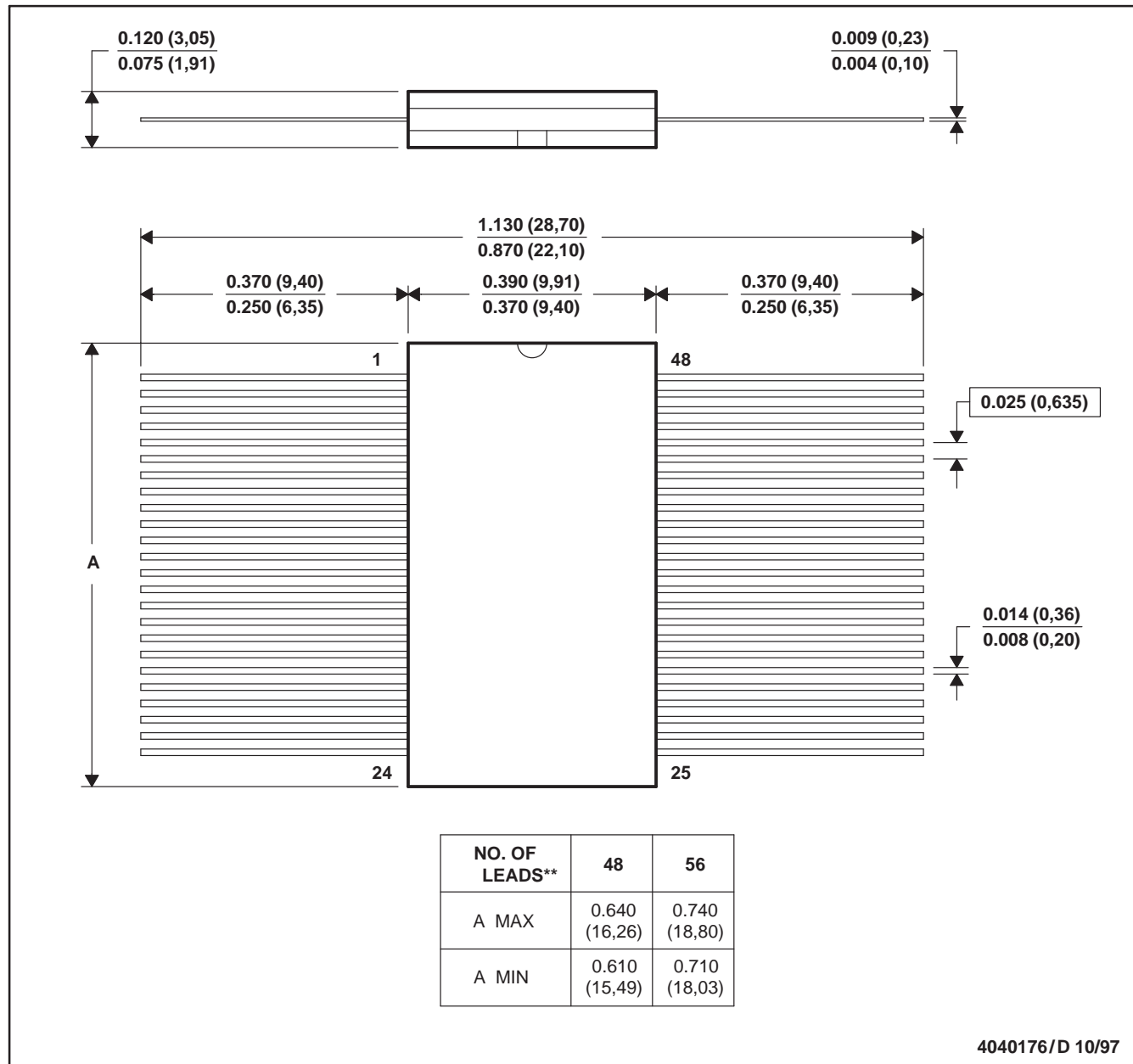
MECHANICAL DATA

MCFP010B – JANUARY 1995 – REVISED NOVEMBER 1997

WD (R-GDFP-F)**

CERAMIC DUAL FLATPACK

48 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA
 GDFP1-F56 and JEDEC MO-146AB

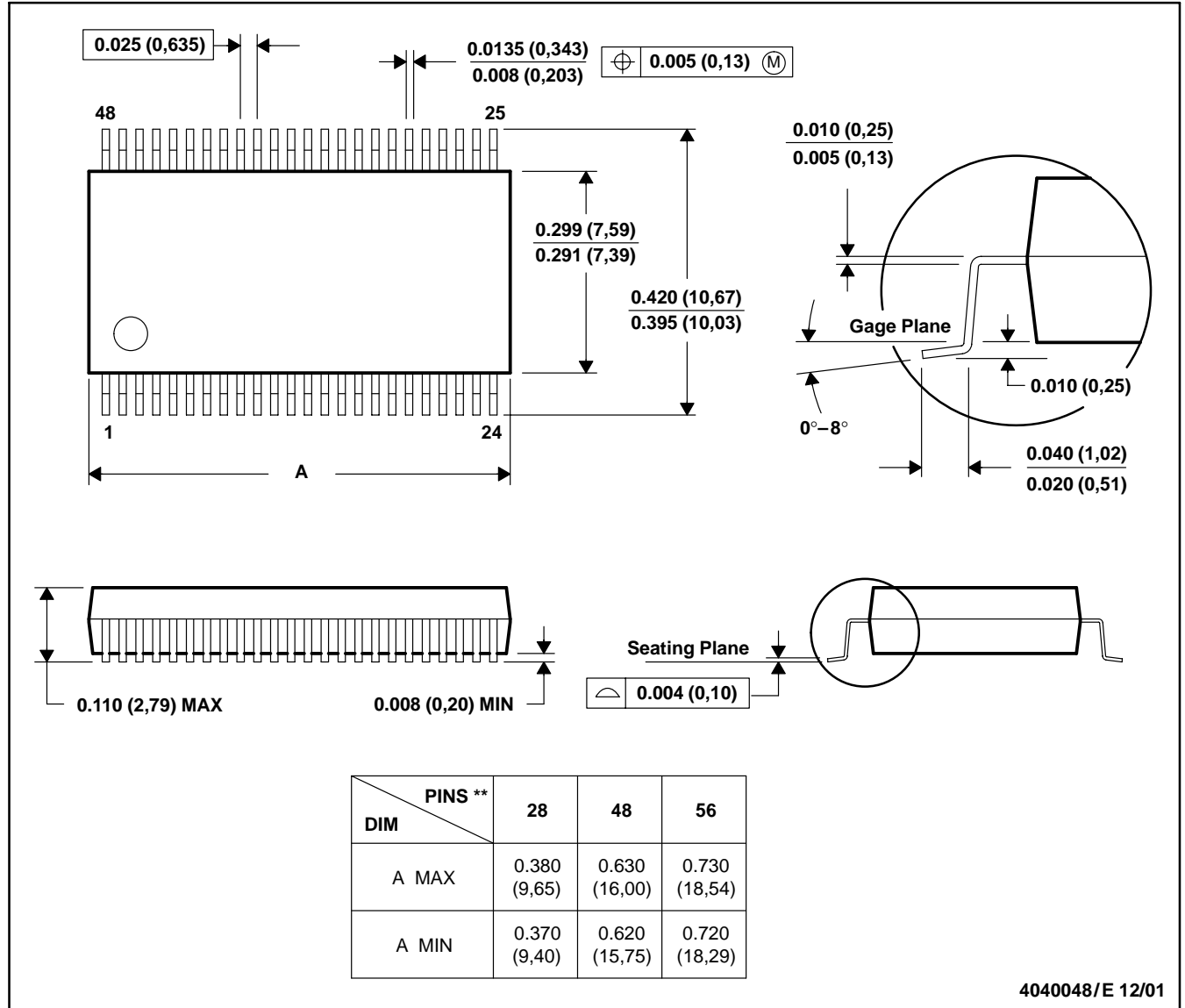
MECHANICAL DATA

MSS0001C – JANUARY 1995 – REVISED DECEMBER 2001

DL (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

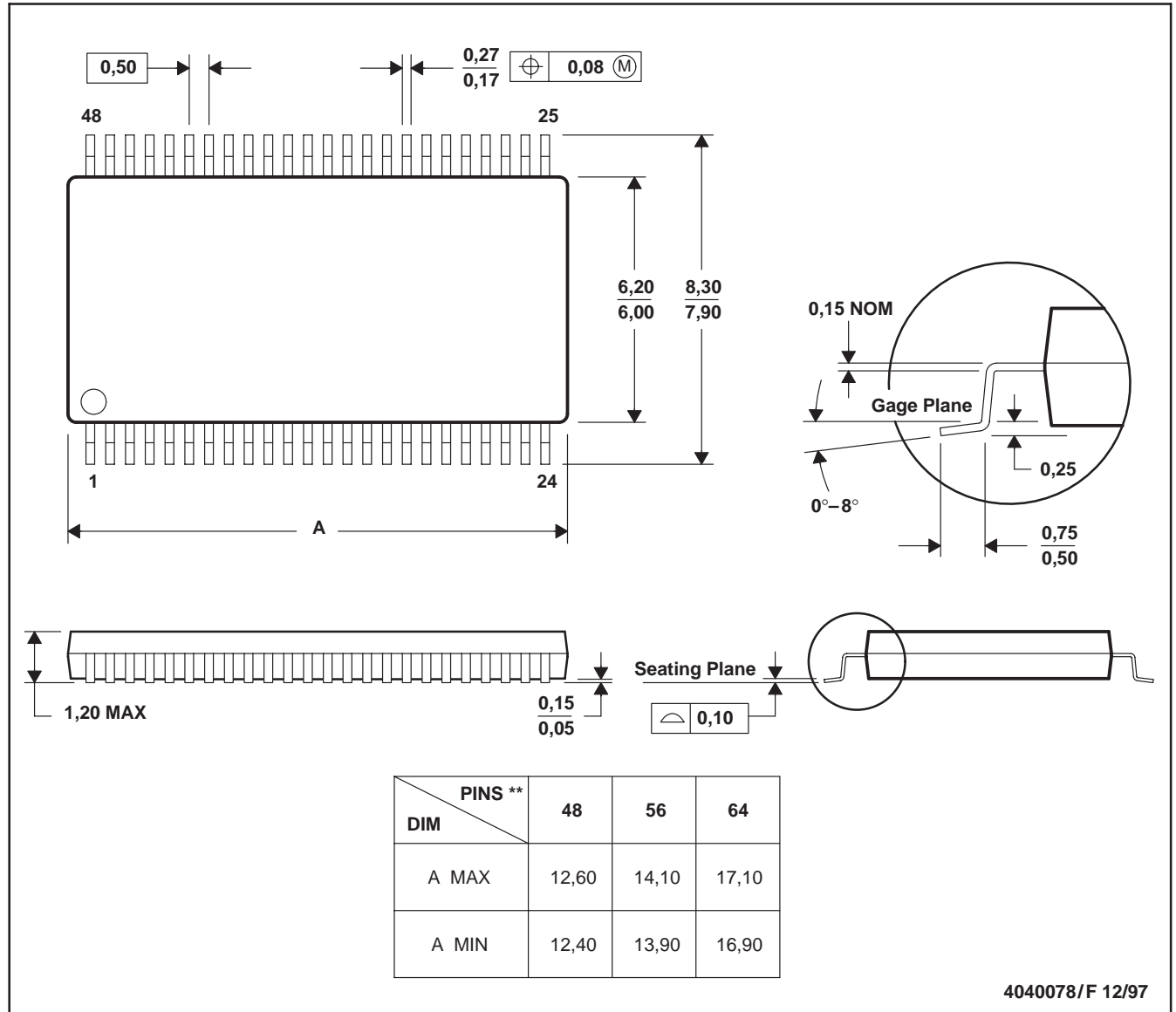
MECHANICAL DATA

MTSS003D – JANUARY 1995 – REVISED JANUARY 1998

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold protrusion not to exceed 0,15.
 - Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265