

TOSHIBA

TC74VHCT573AF/AFW/AFT

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VHCT573AF, TC74VHCT573AFW, TC74VHCT573AFT

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

The TC74VHCT573A is an advanced high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This 8-bit D-type latch is controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$).

When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

The input voltage are compatible with TTL output voltage. This device may be used as a level converter for interfacing 3.3V to 5V system.

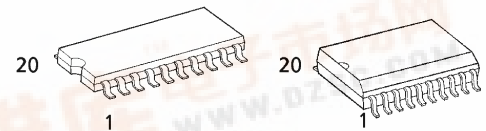
Input protection and output circuit ensure that 0 to 5.5V can be applied to the input and output*1 pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input/output voltages such as battery back up, hot board insertion, etc.

*1: output in off-state

FEATURES:

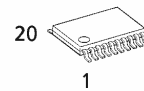
- High Speed..... $t_{pd} = 7.7\text{ns}(\text{typ.})$ at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs.... $V_{IL} = 0.8\text{V}(\text{Max.})$
 $V_{IH} = 2.0\text{V}(\text{Min.})$
- Power Down Protection is provided on all inputs and outputs.
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Low Noise..... $V_{OLP} = 1.6\text{V}(\text{Max.})$
- Pin and Function Compatible with the 74 series (74AC/HC / F/ALS/LS etc.) 573 type.

(Note) The JEDEC SOP (FW) is not available in Japan.



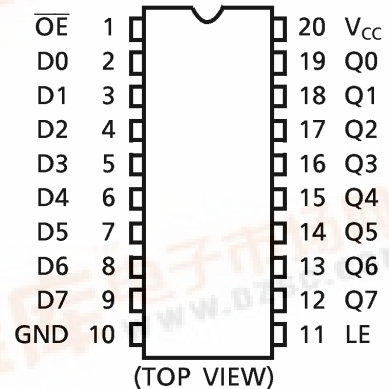
F (SOP20-P-300-1.27)
Weight : 0.22g (Typ.)

FW (SOL20-P-300-1.27)
Weight : 0.46g (Typ.)



FT (TSSOP20-P-0044-0.65)
Weight : 0.08g (Typ.)

PIN ASSIGNMENT



TRUTH TABLE

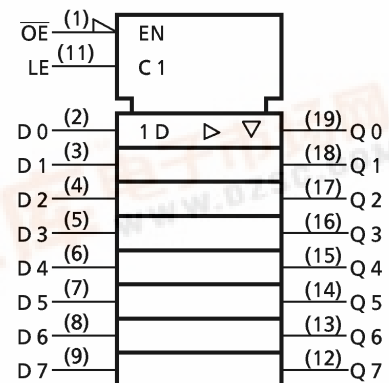
INPUTS			OUTPUT
$\overline{OE}$	LE	D	
H	X	X	Z
L	L	X	Q_n
L	H	L	L
L	H	H	H

X : Don't Care

Z : High Impedance

Q_n : Q outputs are latched at the time when the LE input is taken to a low logic level.

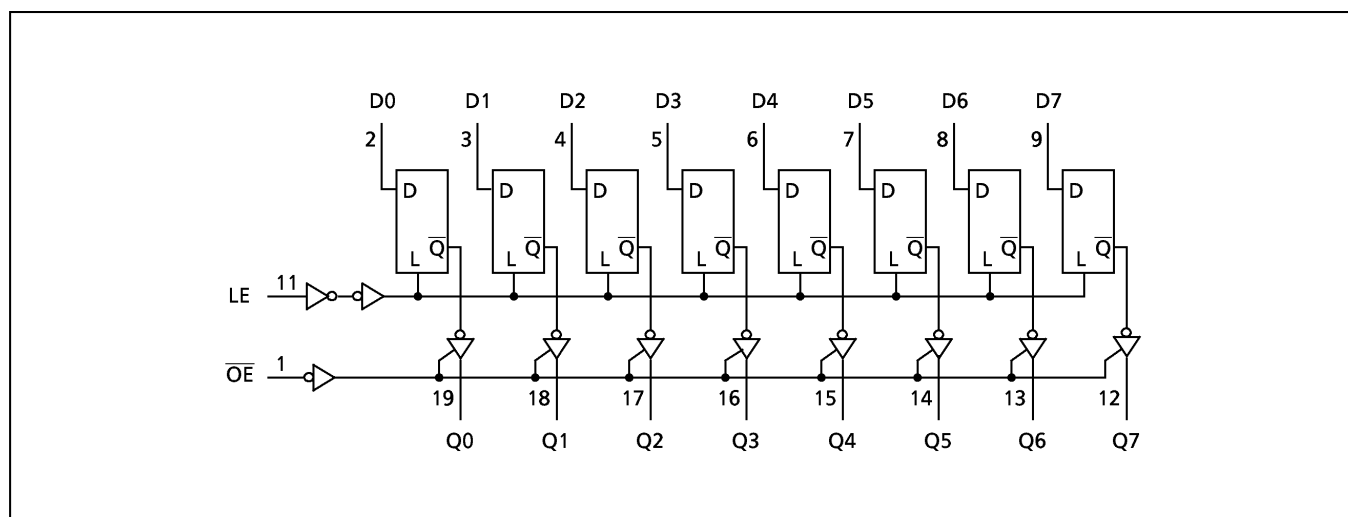
IEC LOGIC SYMBOL



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SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7.0$	V
DC Input Voltage	V_{IN}	$-0.5 \sim 7.0$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim 7.0$ (Note 1)	V
		$-0.5 \sim V_{CC} + 0.5$ (Note 2)	
Input Diode Current	I_{IK}	-20	mA
Output Diode Current	I_{OK}	± 20 (Note 3)	mA
DC Output Current	I_{OUT}	± 25	mA
DC Vcc/Ground Current	I_{CC}	± 75	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	$^{\circ}\text{C}$

(Note 1) Output in Off-State

(Note 2) High or Low State. I_{OUT} absolute maximum rating must be observed.(Note 3) $V_{OUT} < \text{GND}$, $V_{OUT} > V_{CC}$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~5.5 (Note 4)	V
		0~ V_{CC} (Note 5)	
Operating Temperature	T_{opr}	$-40 \sim 85$	$^{\circ}\text{C}$
Input Rise and Fall Time	dt/dV	0~20	ns/V

(Note 4) Output in Off-State

(Note 5) High or Low State

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DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITON		Ta = 25°C			Ta = -40~85°C		UNIT	
				V _{CC} (V)	MIN.	TYP.	MAX.	MIN.		MAX.
High - Level Input Voltage	V _{IH}			4.5~5.5	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V _{IL}			4.5~5.5	—	—	0.8	—	0.8	V
High - Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = - 50μA	4.5	4.40	4.50	—	4.40	—	V
			I _{OH} = - 8mA	4.5	3.94	—	—	3.80	—	
Low - Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50μA	4.5	—	0.0	0.1	—	0.1	V
			I _{OL} = 8mA	4.5	—	—	0.36	—	0.44	
3 - State Output Off - State Current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		5.5	—	—	± 0.25	—	± 2.50	μA
Input Leakage Current	I _{IN}	V _{IN} = 5.5V or GND		0~5.5	—	—	± 0.1	—	± 1.0	
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND		5.5	—	—	4.0	—	40.0	
	I _{CCT}	PER INPUT : V _{IN} = 3.4V OTHER INPUT : V _{CC} or GND		5.5	—	—	1.35	—	1.50	mA
Output Leakage Current	I _{OPD}	V _{OUT} = 5.5V		0	—	—	0.5	—	5.0	μA

TIMING REQUIREMENTS (Input t_r = t_f = 3ns)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C		Ta = -40~85°C	UNIT
				TYP .	LIMIT	LIMIT	
Minimum Pulse Width (LE)	t _W (H)		5.0 ± 0.5	—	6.5	8.5	ns
Minimum Set - up Time	t _s		5.0 ± 0.5	—	1.5	1.5	
Minimum Hold Time	t _h		5.0 ± 0.5	—	3.5	3.5	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = − 40~85°C		UNIT
			V _{CC} (V)	CL (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (LE-Q)	t _{pLH}		5.0 ± 0.5	15	—	7.7	12.3	1.0	13.5	ns
	t _{pHL}			50	—	8.5	13.3	1.0	14.5	
Propagation Delay Time (D-Q)	t _{pLH}		5.0 ± 0.5	15	—	5.1	8.5	1.0	9.5	
	t _{pHL}			50	—	5.9	9.5	1.0	10.5	
3-State Output Enable Time	t _{pZL}	RL = 1kΩ	5.0 ± 0.5	15	—	6.3	10.9	1.0	12.5	
	t _{pZH}			50	—	7.1	11.9	1.0	13.5	
3-State Output Disable Time	t _{pLZ} t _{pHZ}	RL = 1kΩ	5.0 ± 0.5	50	—	8.8	11.2	1.0	12.0	
Output to Output Skew	t _{osLH} t _{osHL}	(Note 6)	5.0 ± 0.5	50	—	—	1.0	—	1.0	
Input Capacitance	C _{IN}				—	4	10	—	10	pF
Output Capacitance	C _{OUT}				—	6	—	—	—	
Power Dissipation Capacitance	C _{PD}	(Note 7)			—	25	—	—	—	

(Note 6) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

(Note 7) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per latch)}$$

And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation :

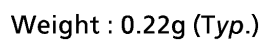
$$C_{PD} \text{ (total)} = 14 + 11 \cdot n$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			UNIT
			V _{CC} (V)	TYP.	MAX.	
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}	C _L = 50pF	5.0	1.1 (1.2)	1.5 (1.6)	V
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}	C _L = 50pF	5.0	− 1.1 (− 1.2)	− 1.5 (− 1.6)	V
Minimum High Level Dynamic Input Voltage	V _{IHD}	C _L = 50pF	5.0	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V _{ILD}	C _L = 50pF	5.0	—	0.8	V

(Note) The value in () only applies to JEDEC SOP (FW) devices.

Unit in mm



Unit in mm

Weight : 0.46g (Typ.)

TSSOP 20PIN OUTLINE DRAWING (TSSOP20-P-0044-0.65)

Unit in mm

