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# TS823/824/825

## Microprocessor Supervisory Circuit with Watchdog Timer & Manual Reset

SOT-25


**7 Voltage Threshold Voltage Option From 2.19V ~ 4.63V**

## General Description

The TS823/824/825 family allows the user to customize the CPU monitoring function without any external components. The user has a large choice of reset voltage thresholds and output driver configurations, all of which are present ant the factory. Each wafer is trimmed to the customer's specifications.

These circuits will ignore fast negative going transients on Vdd. The state of the reset output is guaranteed to be correct down to 1V. After Vdd crosses above a factory present threshold, the TS823/824/825 assert a reset signal. After a predetermined time (the "reset" interval) the reset is deasserted. If Vdd ever drops below the threshold voltage a reset is asserted immediately. In addition to a supply monitoring function the TS823/824/825 also monitor transitions at the watchdog (WDI) input. If a logic transition does not occur at the WDI pin within a certain time interval (the "watchdog" interval) then a reset is asserted. The reset deasserts after the reset interval, as explained earlier.

The TS823/824/825 can both assert a reset manually by pulling the MR input to ground, and the micro-power quiescent current make this family a natural for portable battery powered equipment.

The TS823/824/825 is available in a 5-pin SOT-25 package.

## Features

- ✧ Precision monitoring of +3V, +3.3V and +5V power supply voltage
- ✧ Tight voltage threshold tolerance +/-1.5%
- ✧ Fully specified over temperature
- ✧ 210mS min. power-on reset pulse width
- ✧ 3uA(typ) supply current
- ✧ Guaranteed reset valid to Vdd = +1V
- ✧ Power supply transient immunity
- ✧ No external components

## Ordering Information

| Part No. | Operating Temp. | Package |
|---|---|---|
| TS823CX5 x | - 40 ~ +85 °C | SOT-25 |
| TS824CX5 x | | |
| TS825CX5 x | | |

Note: x is the threshold voltage type, option as

A: 4.63V
B: 4.38V
D: 3.08V
E: 2.93V
F: 2.63V
G: 2.32V
H: 2.19V

## Applications

- ✧ Computers and Controllers
- ✧ Embedded Controllers
- ✧ Intelligent instruments
- ✧ Critical uP monitoring
- ✧ Portable / Battery powered equipment
- ✧ Automotive Systems

## Pin Assignment

| Function | TS823 | TS824 | TS825 |
|---|---|---|---|
| RESET (Active-Low) | 1 | 1 | 1 |
| Ground | 2 | 2 | 2 |
| Manual Reset | 3 | - | 4 |
| (RESET) (Active-High) | - | 3 | 3 |
| Watchdog Input | 4 | 4 | - |
| Supply Voltage (Vdd) | 5 | 5 | 5 |

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## Absolute Maximum Rating

| | | | |
|---|---|---|---|
| Supply Voltage | Vdd | 6.0 | V |
| Supply Voltage - Recommended | Vdd | 0.9 ~ 5 | V |
| Operating Junction Temperature Range | $T_{OP}$ | -40 ~ +125 | °C |
| Storage Temperature Range | $T_{STG}$ | -65 ~ +150 | °C |
| Caution: stress above the listed absolute rating may cause permanent damage to the device | | | |

## Thermal Information

| | | | |
|---|---|---|---|
| Thermal Resistance | Θjc | 256 | °C/W |
| Maximum Junction Temperature | Tj | 150 | V |
| Maximum Lead Temperature (300 °C) | $T_{LEAD}$ | 10 | S |

## Electrical Characteristics

Ta = 25 °C, unless otherwise specified.

| Parameter | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Supply Voltage | | Vdd | 1.0 | -- | 5.5 | V |
| Supply Current | WDI and MRB unconnected | Idd | -- | 3 | 10 | uA |
| Reset Threshold | TS823/824/825CX5A | $V_{TH}$ | 4.56 | 4.63 | 4.7 | V |
| | TS823/824/825CX5B | | 4.31 | 4.38 | 4.45 | |
| | TS823/824/825CX5D | | 3.03 | 3.08 | 3.13 | |
| | TS823/824/825CX5E | | 2.89 | 2.93 | 2.97 | |
| | TS823/824/825CX5F | | 2.59 | 2.63 | 2.67 | |
| | TS823/824/825CX5G | | 2.28 | 2.32 | 2.36 | |
| | TS823/824/825CX5H | | 2.15 | 2.19 | 2.23 | |
| RESET Output Voltage Low | Vdd < $V_{TH(MIN)}$, $I_{SINK}$ =1.2mA, | $V_{OL}$ | -- | -- | 0.5 | V |
| (RESET) Output Voltage High | Vdd > $V_{TH(MAX)}$, $I_{SOURCE}$=0.5mA | $V_{OH}$ | 0.8 Vdd | -- | -- | V |
| Vdd to Reset Delay | Vdd = $V_{TH}$ - 100mV | $T_{D1}$ | -- | 40 | -- | uS |
| Reset Active Timeout Period | Ta = -40 °C ~ +85 °C | $T_{D2}$ | 140 | 210 | 280 | mS |
| Watchdog Timeout Period | | $T_{WD}$ | 1120 | 1760 | 2400 | mS |
| WDI Pulse Width | | $T_{WDI}$ | 50 | -- | -- | nS |
| WDI Input Threshold | Vdd = $V_{TH}$ x 1.2 | $WDI_{IL}$ | -- | -- | 0.7 | V |
| | | $WDI_{IH}$ | 0.8 Vdd | -- | -- | V |
| WDI Input Current | WDI = 0V | $I_{IL}$ | -15 | -8 | 0.7 | uA |
| | WDI = Vdd = 5V | $I_{IH}$ | -- | 8 | 15 | uA |
| MR Input Threshold | Vdd = $V_{TH}$ x 1.2 | $MR_{IL}$ | -- | -- | 0.7 | V |
| | | $MR_{IH}$ | 0.8 Vdd | -- | -- | V |
| MR Pulse Width | | $T_{WMR}$ | 1 | -- | -- | uS |
| MR Noise Immunity | Pulse width with no reset | | -- | 100 | -- | nS |
| MR to Reset Delay | Vdd = $V_{TH}$ - 100mV | $T_{DMR}$ | -- | 500 | -- | nS |
| MR Pull Up Resistance | | | 80 | -- | 120 | KΩ |

## Detail Description

### Pin Function

** RESET
RESET is active low.
** GND
Ground
** (RESET)
(RESET) is active high.
** MR
This pin is active low. Pulling this pin low to forces a reset. After a low to high transition reset remains asserted for exactly one reset timeout period. This pin is internally pulled high. If this function is unused then float this pin or tie it to Vdd.
** WDI
Watch Dog Input. Any transition on this pin will reset the Watch Dog timer. If this pin remains high or low for longer than the Watch Dog interval then a reset is asserted. Float or tri-state this pin to disable the Watch Dog feature.
** Vdd
Positive power supply. A reset is asserted after this voltage drops below a predetermined level. After Vdd rises above that level reset remains asserted until the end of the reset timeout period.

### Applications Information

The TS823/824/825 are designed to interface with the reset input of a microprocessor and to prevent CPU execution errors due to power up, power down, and other power supply errors. The TS823/824 also monitor the CPU health by checking for signal transitions form the CPU at the WDI input.

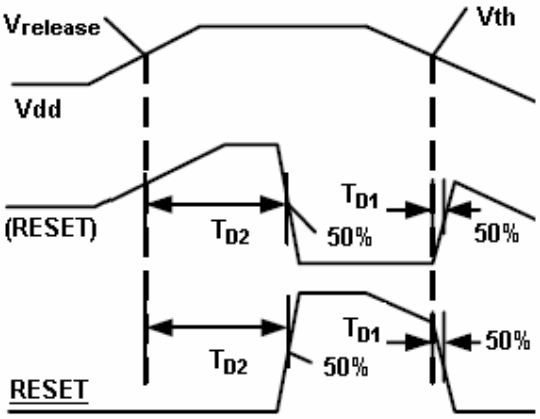
### Reset Output

Active low reset outputs are denoted as RESET, Active high reset output are denoted as (RESET),
A reset will be asserted if any of three things happen:

1) Vdd drops below the threshold (Vth)
2) The MR pin is pulled low.
3) The WDI pin does not detect a transition within the Watch Dog interval ($T_{WD}$)

The reset will remain asserted for the prescribed reset interval after:

1) Vdd rises above the threshold (Vth)
2) MR goes high
3) The Watch Dog timer have timed out causing the reset to assert.




**Reset Timing Diagram**

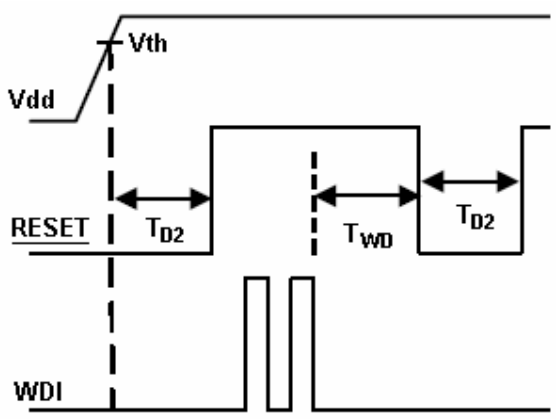
### Manual Reset Input

The TS823 and TS825 feature a manual reset feature (MR). A logic low on the MR pin asserts a reset. The reset remains asserted a long as the MR pin remains low. After the MR pin transitions to a high state the reset remains asserted for the prescribed reset interval ($T_{D2}$). The MR pin is internally pulled up to Vdd by a 100KΩ resistor. It is internally de-bounced to reject switching transients.
The MR pin is ESD protected by diodes connected to Vdd and Gnd. So the MR pin should never be driven higher than Vdd or lower than Gnd.

### Watchdog Input

The TS823 and TS824 are equipped with a watchdog input (WDI). If the microprocessor does not produce a valid logic edge at the watchdog input (WDI) within the prescribed watchdog interval ($T_{WD}$) then a reset asserts. The reset remains asserted for the required reset interval ($T_{D2}$). Ata the end of the reset interval the reset is deasserted and the watchdog interval timer starts again from zero.
If the watchdog input is left unconnected or is connected to a tri-stated buffer the watchdog function is disabled. As soon as the WDI input is driven either low or high the watchdog function resumes with the watchdog timer set to zero.

## Detail Description (continued)




**Watchdog Timing Diagram**

### Watchdog Input Current

The watchdog input pin (WDI) typically sources/sinks 8uA when driven high or low. So from a power dissipation point of view the duty cycle of the waveform at WDI is unimportant. When the WDI pin is floating or tri-stated the power supply current fall to less than 3uA.

### Glitch Rejection

The TS823/824/825 family will reject negative going transients on the Vdd line to some extent. The smaller the duration of the transient the larger its amplitude may be without triggering a reset. The “Glitch Rejection” chart in the graphs section of this datasheet shows the relation between glitch amplitude and allowable glitch duration to avoid unintended resets.

### Accurate Output State at Low Vdd

With Vdd voltage on the order of the MOS transistor threshold (<1V) the outputs of the TS823/824/825 may become undefined. For parts with active low output RESET a resistor placed between RESET and Gnd on the order of 100KΩ will ensure that the RESET output stays low when Vdd is lower than the threshold voltage of the part. In a like manner a resistor on the order of 100KΩ when placed between (RESET) and Vdd will ensure parts with active high output (RESET) will remain high when Vdd is lower than the threshold voltage of the parts.

## Electrical Characteristics Curve

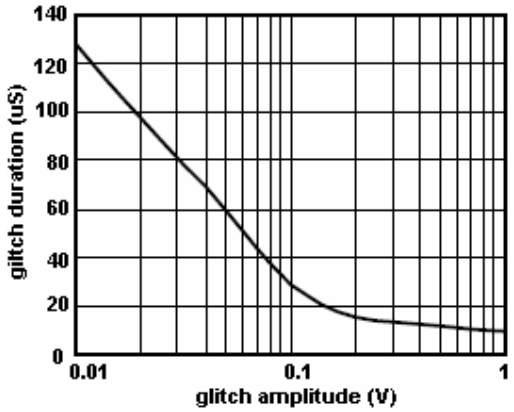


Fig 1. Glitch Rejection

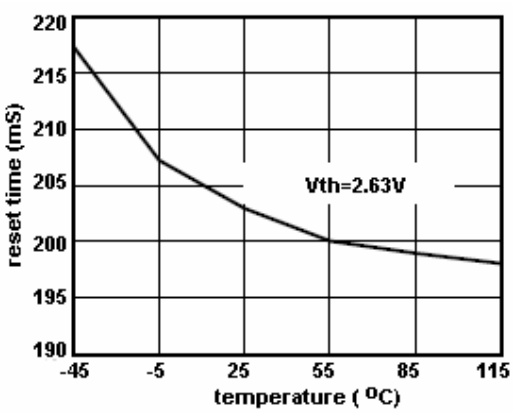


Fig 2. Reset time vs Temp.

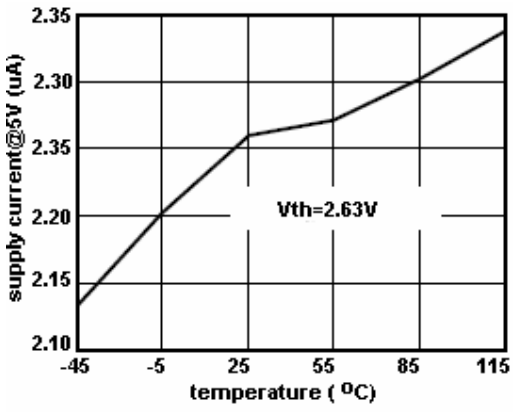


Fig 3. Idd vs Temp.

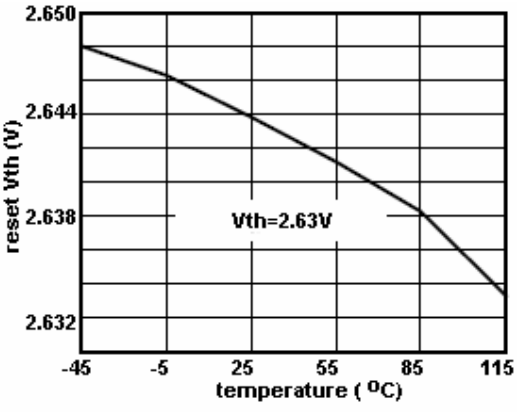


Fig 4. Reset Vth vs Temp.

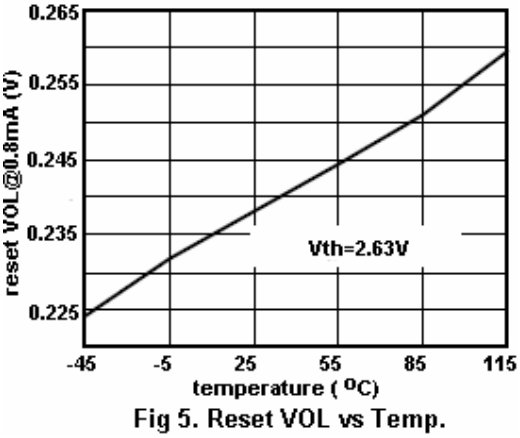
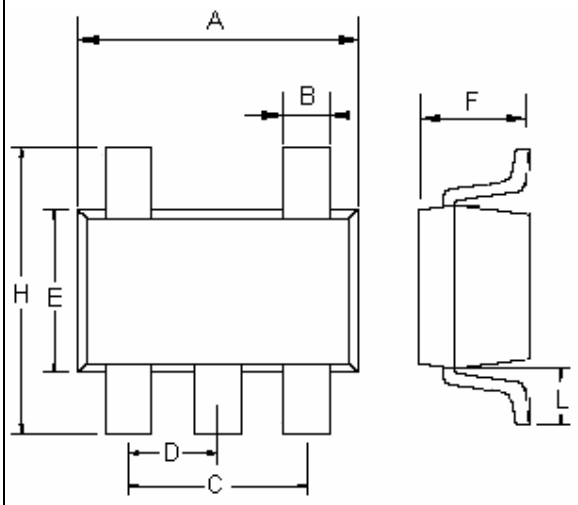


Fig 5. Reset VOL vs Temp.

# SOT-25 Mechanical Drawing




| SOT-25 DIMENSION | | | | |
|---|---|---|---|---|
| DIM | MILLIMETERS | | INCHES | |
| | MIN | MAX | MIN | MAX |
| A | 2.70 | 3.00 | 0.106 | 0.118 |
| B | 0.25 | 0.50 | 0.010 | 0.020 |
| C | 1.90(typ) | | 0.075(typ) | |
| D | 0.95(typ) | | 0.037(typ) | |
| E | 1.50 | 1.70 | 0.059 | 0.067 |
| F | 1.05 | 1.35 | 0.041 | 0.053 |
| H | 2.60 | 3.00 | 0.102 | 0.118 |
| L | 0.60(typ) | | 0.024(typ) | |