TEXAS INSTRUMENTS

CD74FCT543

Data sheet acquired from Harris Semiconductor
SCHS258

January 1997

NOT RECOMMENDED FOR NEW DESIGNS
Use CMOS Technology

BiCMOS FCT Interface Logic, Octal Register/Transceiver, Three-State

Features

- Buffered Inputs
- Typical Propagation Delay: 6.4ns at V_{CC} = 5V, T_A = 25°C, C_L = 50pF
- Noninverting
- Family Features
  - SCR Latchup Resistant BiCMOS Process and Circuit Design
  - Speed of Bipolar FAST™/AS/S
  - 64mA Output Sink Current
  - Output Voltage Swing Limited to 3.7V at V_{CC} = 5V
  - Controlled Output Edge Rates
  - Input/Output Isolation to V_{CC}
  - BiCMOS Technology with Low Quiescent Power

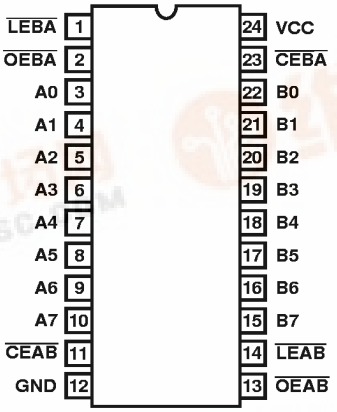
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT543EN	0 to 70	24 Ld PDIP	E24.3
CD74FCT543M	0 to 70	24 Ld SOIC	M24.3
CD74FCT543SM	0 to 70	24 Ld SSOP	M24.209

NOTE: When ordering the suffix M and SM packages, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinout

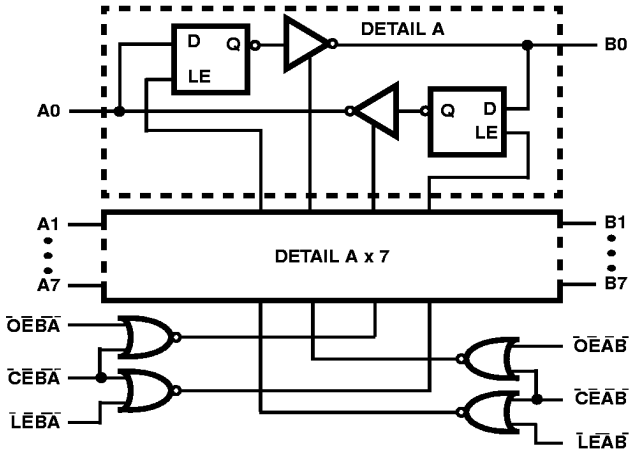
CD74FCT543
(PDIP, SOIC, SSOP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 2399.2

Functional Diagram



TRUTH TABLE For A to B (Symmetric with B to A)

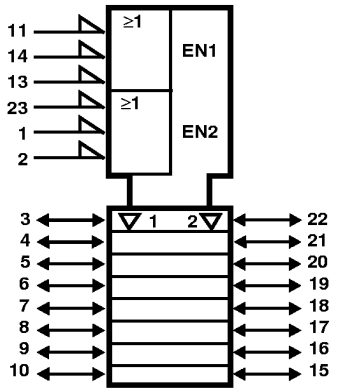
INPUTS			LATCH STATUS	OUTPUT BUFFERS
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A TO B	B0 THRU B7
H	X	X	Storing	High Z
X	H	–	Storing	-
X	-	H	-	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous A Inputs (Note 1)

NOTE:

1. Before $\overline{LEAB}$ LOW to HIGH Transition
   H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Immaterial
   A to B data flow shown; B to A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.

IEC Logic Symbol

CD74FCT543



Absolute Maximum Ratings

DC Supply Voltage (V_{CC}) . . . . . -0.5V to 6V
DC Input Diode Current, I_{IK} (For V_I < -0.5V) . . . . . -20mA
DC Output Diode Current, I_{OK} (for V_O < -0.5V) . . . . . -50mA
DC Output Sink Current per Output Pin, IO 70mA
DC Output Source Current per Output Pin, IO . . . . . -30mA
DC V_{CC} Current (I_{CC}) 140mA
DC Ground Current (I_{GND}) 528mA

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} ($^oC/W$)
PDIP Package 75
SOIC Package 75
SSOP Package 125
Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC and SSOP-Lead Tips Only)

Operating Conditions

Operating Temperature Range (T_A) . . . . . 0^oC to 70^oC
Supply Voltage Range, V_{CC} . . . . . 4.75V to 5.25V
DC Input Voltage, V_I . . . . . 0 to V_{CC}
DC Output Voltage, V_O . . . . . 0 to $\leq V_{CC}$
Input Rise and Fall Slew Rate, dt/dv . . . . . 0 to 10ns/V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications Commercial Temperature Range 0^oC to 70^oC, V_{CC} Max = 5.25V, V_{CC} Min = 4.75V

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A)				UNITS
					25^oC		0^oC TO 70^oC		
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	
High Level Input Voltage	V_{IH}			4.75 to 5.25	2	-	2	-	V
Low Level Input Voltage	V_{IL}			4.75 to 5.25	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	Min	2.4	-	2.4	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	64	Min	-	0.55	-	0.55	V
High Level Input Current	I_{IH}	V_{CC}		Max	-	0.1	-	1	µA
Low Level Input Current	I_{IL}	GND		Max	-	-0.1	-	-1	µA
Three-State Leakage Current	I_{OZH}	V_{CC}		Max	-	0.5	-	10	µA
	I_{OZL}	GND		Max	-	-0.5	-	-10	µA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	Min	-	-1.2	-	-1.2	V
Short Circuit Output Current (Note 3)	I_{OS}	V_O = 0 V_{CC} or GND		Max	-60	-	-60	-	mA
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	Max	-	8	-	80	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V (Note 4)		Max	-	1.6	-	1.6	mA

NOTES:

3. Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
4. Inputs that are not measured are at V_{CC} or GND.
5. FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Electrical Specifications table, e.g., 1.6mA Max. at 70^oC.

Switching Specifications Over Operating Range FCT Series t_r, t_f = 2.5ns, C_L = 50pF, R_L (Figure 4)

PARAMETER	SYMBOL	V_{CC} (V)	25°C	0°C TO 70°C			UNITS
			TYP	MIN	TYP	MAX	
Propagation Delays							
An ↔ Bn	t_{PLH}, t_{PHL}	5	6.4	2.5	-	8.5	ns
$\overline{LEBA}$ to An or $\overline{LEAB}$ to Bn	t_{PLH}, t_{PHL}	5	9.4	2.5	-	12.5	ns
$\overline{CEBA}$ or $\overline{CEAB}$ to An or Bn	t_{PLZ}, t_{PHZ}	5	6.8	2	-	9	ns
	t_{PZL}, t_{PZH}	5	9	2	-	12	ns
Power Dissipation Capacitance	C_{PD} (Note 6)	-	49	-	49	-	pF
Minimum (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV}	5	0.5	-	-	-	V
Maximum (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP}	5	1	-	-	-	V
Input Capacitance	C_I	-	-	-	-	10	pF
Input/Output Capacitance	$C_{I/O}$	-	-	-	-	15	pF

NOTE:

6. C_{PD}, measured per flip-flop, is used to determine the dynamic power consumption.
   P_D (per package) = V_{CC} I_{CC} + $\Sigma(V_{CC}^2$ f_I C_{PD} + V_O^2 f_O C_L + V_{CC} ΔI_{CC} D) where:
   V_{CC} = supply voltage
   ΔI_{CC} = flow through current x unit load
   C_L = output load capacitance
   D = duty cycle of input high
   f_O = output frequency
   f_I = input frequency

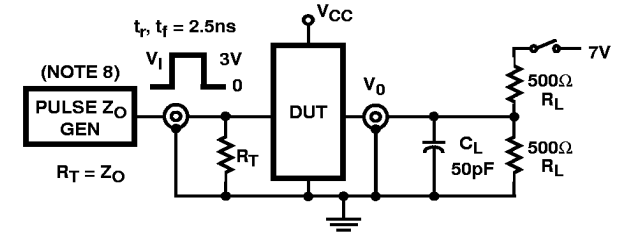
Prerequisite for Switching

PARAMETER	SYMBOL	V_{CC} (V)	25°C	0°C TO 70°C		UNITS
			TYP	MIN	MAX	
Data to Latch Enable Setup Time	t_{SU}	5 (Note 7)	-	3	-	ns
Data to Latch Enable Hold Time	t_H	5	-	2	-	ns
Latch Enable Pulse Width	t_W	5	-	9	-	ns

NOTE:

7. 5V: Minimum is at 4.75V for 0°C to 70°C, Typical is at 5V.

Test Circuits and Waveforms



NOTE:

8. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

V_{IN} = 0V to 3V.

Input: $t_r = t_f$ = 2.5ns (10% to 90%), unless otherwise specified

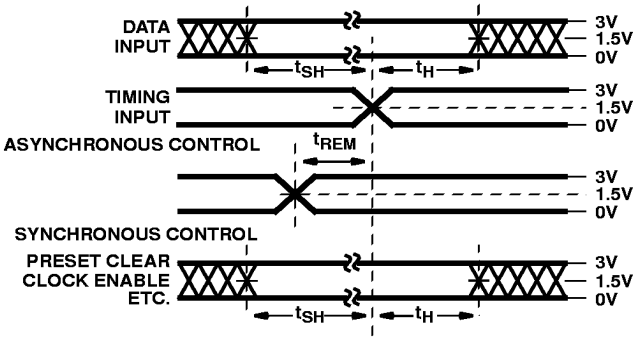


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

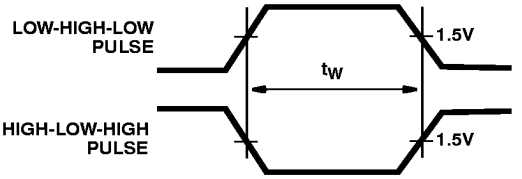


FIGURE 3. PULSE WIDTH

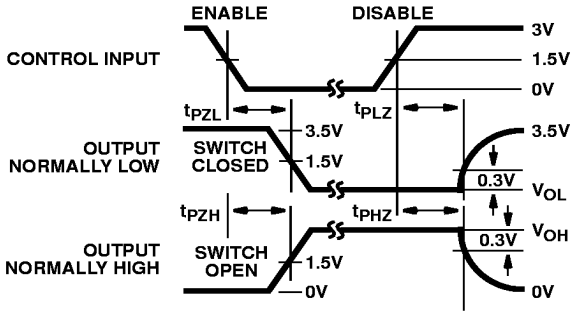


FIGURE 4. ENABLE AND DISABLE TIMING

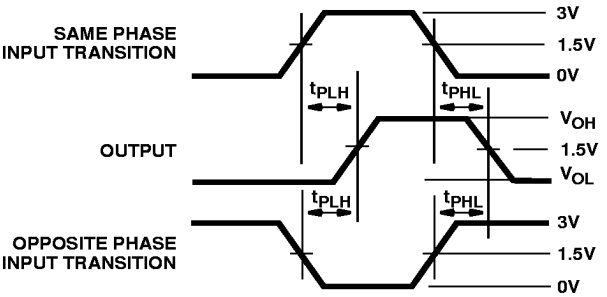
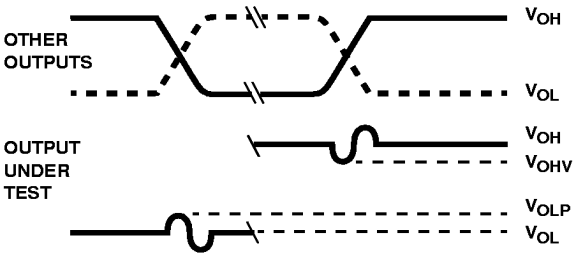


FIGURE 5. PROPAGATION DELAY



NOTES:

9. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH}.
10. Input pulses have the following characteristics: P_{RR} ≤ 1MHz, t_r = 2.5ns, t_f = 2.5ns, skew 1ns.
11. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with 0.1μF capacitor. Scope and probes require 700MHz bandwidth.

FIGURE 6. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS