查询ADS8343E/2K5供应商 捷多邦，专业PCB打样工厂，24小时加急出货

SBAS183A – JANUARY 2001 – REVISED OCTOBER 2002

16-Bit, 4-Channel Serial Output Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- BIPOLAR INPUT RANGE
- PIN-FOR-PIN COMPATIBLE WITH THE ADS7841 AND ADS8341
- SINGLE SUPPLY: 2.7V to 5V
- 4-CHANNEL SINGLE-ENDED OR 2-CHANNEL DIFFERENTIAL INPUT
- UP TO 100kHz CONVERSION RATE
- 86dB SINAD
- SERIAL INTERFACE
- SSOP-16 PACKAGE

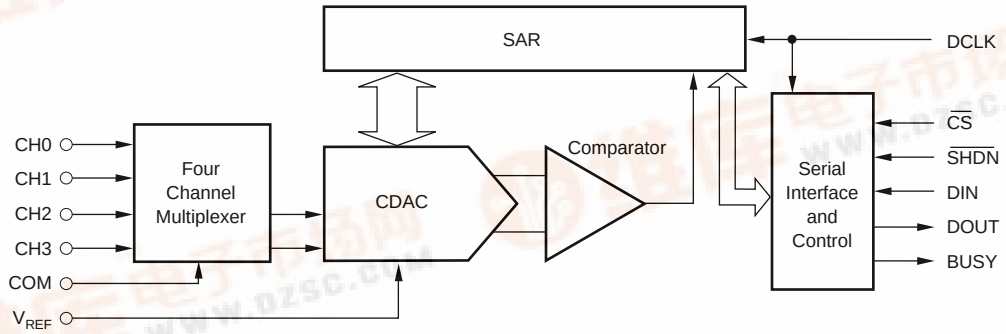
APPLICATIONS

- DATA ACQUISITION
- TEST AND MEASUREMENT
- INDUSTRIAL PROCESS CONTROL
- PERSONAL DIGITAL ASSISTANTS
- BATTERY-POWERED SYSTEMS

DESCRIPTION

The ADS8343 is a 4-channel, 16-bit sampling Analog-to-Digital (A/D) converter with a synchronous serial interface. Typical power dissipation is 8mW at a 100kHz throughput rate and a +5V supply. The reference voltage (V_{REF}) can be varied between 500mV and $V_{CC}/2$, providing a corresponding input voltage range of $\pm V_{REF}$. The device includes a shut-down mode which reduces power dissipation to under 15µW. The ADS8343 is ensured down to 2.7V operation.

Low power, high speed, and an onboard multiplexer make the ADS8343 ideal for battery-operated systems such as personal digital assistants, portable multi-channel data loggers, and measurement equipment. The serial interface also provides low-cost isolation for remote data acquisition. The ADS8343 is available in an SSOP-16 package and is ensured over the –40°C to +85°C temperature range.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include

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PACKAGE/ORDERING INFORMATION

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	NO MISSING CODES ERROR (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR[1]	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS8343E	8	14	SSOP-16	DBQ	–40°C to +85°C	ADS8343E	Rails, 100
"	"	"	"	"	"	ADS8343E/2K5	Tape and Reel, 2500
ADS8343EB	6	15	SSOP-16	DBQ	–40°C to +85°C	ADS8343EB	Rails, 100
"	"	"	"	"	"	ADS8343EB/2K5	Tape and Reel, 2500

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS[1]

$+V_{CC}$ to GND	–0.3V to +6V
Analog Inputs to GND	–0.3V to $+V_{CC}$ + 0.3V
Digital Inputs to GND	–0.3V to +6V
Power Dissipation	250mW
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

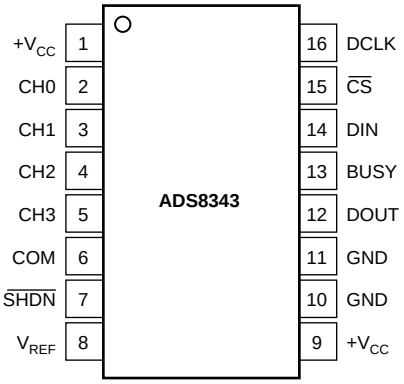
ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATIONS

Top View **SSOP**



PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	$+V_{CC}$	Power Supply, 2.7V to 5V
2	CH0	Analog Input Channel 0
3	CH1	Analog Input Channel 1
4	CH2	Analog Input Channel 2
5	CH3	Analog Input Channel 3
6	COM	Common reference for analog inputs. This pin is typically connected to V_{REF}.
7	$\overline{SHDN}$	Shutdown. When LOW, the device enters a very low power shutdown mode.
8	V_{REF}	Voltage Reference Input. See Electrical Characteristic Table for ranges.
9	$+V_{CC}$	Power Supply, 2.7V to 5V
10	GND	Ground
11	GND	Ground
12	DOUT	Serial Data Output. Data is shifted on the falling edge of DCLK. This output is high impedance when $\overline{CS}$ is HIGH.
13	BUSY	Busy Output. This output is high impedance when $\overline{CS}$ is HIGH.
14	DIN	Serial Data Input. If $\overline{CS}$ is LOW, data is latched on rising edge of DCLK.
15	$\overline{CS}$	Chip Select Input. Controls conversion timing and enables the serial input/output register.
16	DCLK	External Clock Input. This clock runs the SAR conversion process and synchronizes serial data I/O. Maximum input clock frequency equals 2.4MHz to achieve 100kHz sampling rate.

ELECTRICAL CHARACTERISTICS: +5V

At T_A = –40°C to +85°C, $+V_{CC}$ = +5V, V_{REF} = +2.5V, f_{SAMPLE} = 100kHz, and f_{CLK} = 24 • f_{SAMPLE} = 2.4MHz, unless otherwise noted.

PARAMETER	CONDITIONS	ADS8343E			ADS8343EB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				16			*	Bits
ANALOG INPUT								
Full-Scale Input Span	Positive Input-Negative Input	$–V_{REF}$		$+V_{REF}$	*		*	V
Absolute Input Range	Positive Input	–0.2		$+V_{CC}$ + 0.2	*		*	V
	Negative Input	–0.2		$+V_{CC}$ + 0.2	*		*	V
Capacitance			25			*		pF
Leakage Current			±1			*		µA
SYSTEM PERFORMANCE								
No Missing Codes		14			15			Bits
Integral Linearity Error				±8			±6	LSB
Bipolar Error				±2			±1	mV
Bipolar Error Match			2.3	8.0		*	*	LSB(1)
Gain Error				±0.05			±0.024	%
Gain Error Match			1.0	4.0		*	*	LSB
Noise			20			*		µVrms
Power-Supply Rejection	+4.75V < V_{CC} < 5.25V		3			*		LSB(1)
SAMPLING DYNAMICS								
Conversion Time				16			*	Clk Cycles
Acquisition Time		4.5			*			Clk Cycles
Throughput Rate				100			*	kHz
Multiplexer Settling Time			500			*		ns
Aperture Delay			30			*		ns
Aperture Jitter			100			*		ps
Internal Clock Frequency	$\overline{SHDN}$ = V_{DD}		2.4			*		MHz
External Clock Frequency		0.024		2.4	*		*	MHz
	Data Transfer Only	0		2.4	*		*	MHz
DYNAMIC CHARACTERISTICS								
Total Harmonic Distortion(2)	V_{IN} = 5Vp-p at 10kHz		–95			*		dB
Signal-to-(Noise + Distortion)	V_{IN} = 5Vp-p at 10kHz		86			*		dB
Spurious-Free Dynamic Range	V_{IN} = 5Vp-p at 10kHz		97			*		dB
Channel-to-Channel Isolation	V_{IN} = 5Vp-p at 50kHz		100			*		dB
REFERENCE INPUT								
Range		0.5		$+V_{CC}$/2	*		*	V
Resistance	DCLK Static		5			*		GΩ
Input Current			40	100		*	*	µA
	f_{SAMPLE} = 12.5kHz		2.5			*		µA
	DCLK Static		0.001	3		*	*	µA
DIGITAL INPUT/OUTPUT								
Logic Family			CMOS			*		
Logic Levels								
V_{IH}	| I_{IH} | ≤ +5µA	3.0		5.5	*		*	V
V_{IL}	| I_{IL} | ≤ +5µA	–0.3		+0.8	*		*	V
V_{OH}	I_{OH} = –250µA	3.5			*			V
V_{OL}	I_{OL} = 250µA			0.4			*	V
Data Format		Binary Two's Complement					*	
POWER-SUPPLY REQUIREMENTS								
$+V_{CC}$	Specified Performance	4.75		5.25	*		*	V
Quiescent Current			1.5	2.0			*	mA
	f_{SAMPLE} = 10kHz		150			*		µA
	Power-Down Mode(3, 4), $\overline{CS}$ = $+V_{CC}$			3			*	µA
Power Dissipation			7.5	10			*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

* Same specifications as ADS8343E.

NOTES: (1) LSB means Least Significant Bit. With V_{REF} equal to +2.5V, one LSB is 76µV. (2) First nine harmonics of the test frequency. (3) Auto power-down mode (PD1 = PD0 = 0) active or $\overline{SHDN}$ = GND. (4) Power-down after conversion mode with external clock gated 'HIGH'.

ELECTRICAL CHARACTERISTICS: +2.7V

At T_A = –40°C to +85°C, $+V_{CC}$ = +2.7V, V_{REF} = +1.25V, f_{SAMPLE} = 100kHz, and f_{CLK} = 24 • f_{SAMPLE} = 2.4MHz, unless otherwise noted.

PARAMETER	CONDITIONS	ADS8343E			ADS8343EB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				**16**			*	**BITS**
ANALOG INPUT								
Full-Scale Input Span	Positive Input-Negative Input	$–V_{REF}$		$+V_{REF}$	*		*	V
Absolute Input Range	Positive Input	–0.2		$+V_{CC}$ + 0.2	*		*	V
	Negative Input	–0.2		$+V_{CC}$ + 0.2	*		*	V
Capacitance			25			*		pF
Leakage Current			±1			*		µA
SYSTEM PERFORMANCE								
No Missing Codes		14			15			Bits
Integral Linearity Error				±12			±8	LSB
Bipolar Error				±1			±0.5	mV
Bipolar Error Match			1.2	4.0		*	*	LSB
Gain Error				±0.05			±0.0024	% of FSR
Gain Error Match			1.0	4.0		*	*	LSB
Noise			20			*		µVrms
Power-Supply Rejection	$+2.7 < V_{CC} < +3.3V$		3			*		LSB[1]
SAMPLING DYNAMICS								
Conversion Time				16			*	Clk Cycles
Acquisition Time		4.5			*			Clk Cycles
Throughput Rate				100			*	kHz
Multiplexer Settling Time			500			*		ns
Aperture Delay			30			*		ns
Aperture Jitter			100			*		ps
Internal Clock Frequency	$\overline{SHDN}$ = V_{DD}		2.4			*		MHz
External Clock Frequency		0.024		2.4	*		*	MHz
	When Used with Internal Clock	0.024		2.0	*		*	MHz
	Data Transfer Only	0		2.4	*		*	MHz
DYNAMIC CHARACTERISTICS								
Total Harmonic Distortion[2]	V_{IN} = 2.5Vp-p at 1kHz		–94			*		dB
Signal-to-(Noise + Distortion)	V_{IN} = 2.5Vp-p at 1kHz		81			*		dB
Spurious-Free Dynamic Range	V_{IN} = 2.5Vp-p at 1kHz		98			*		dB
Channel-to-Channel Isolation	V_{IN} = 2.5Vp-p at 10kHz		100			*		dB
REFERENCE INPUT								
Range		0.5		$+V_{CC}/2$	*		*	V
Resistance	DCLK Static		5			*		GΩ
Input Current			13	40		*	*	µA
	f_{SAMPLE} = 12.5kHz		2.5			*		µA
	DCLK Static		0.001	3		*	*	µA
DIGITAL INPUT/OUTPUT								
Logic Family			CMOS			*		
Logic Levels								
V_{IH}	$\lvert I_{IH} \rvert \leq +5\mu A$	$+V_{CC}$ • 0.7		5.5	*		*	V
V_{IL}	$\lvert I_{IL} \rvert \leq +5\mu A$	–0.3		+0.8	*		*	V
V_{OH}	I_{OH} = –250µA	$+V_{CC}$ • 0.8			*			V
V_{OL}	I_{OL} = 250µA			0.4			*	V
Data Format			Binary Two's Complement				*	
POWER-SUPPLY REQUIREMENTS								
$+V_{CC}$	Specified Performance	2.7		3.6	*		*	V
Quiescent Current			1.2	1.85		*	*	mA
	f_{SAMPLE} = 10kHz		105					µA
	Power-Down Mode[3, 4], $\overline{CS}$ = $+V_{CC}$			3			*	µA
Power Dissipation			3.2	5			*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

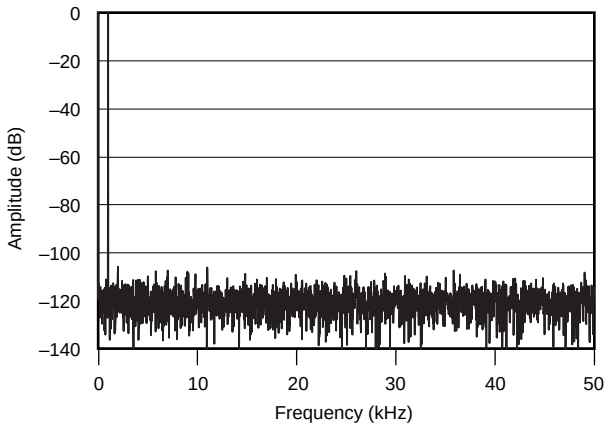
* Same specifications as ADS8343E.

NOTES: (1) LSB means Least Significant Bit. With V_{REF} equal to +1.25V, one LSB is 38µV. (2) First nine harmonics of the test frequency. (3) Auto power-down mode (PD1 = PD0 = 0) active or $\overline{SHDN}$ = GND. (4) Power-down after conversion mode with external clock gated 'HIGH'.

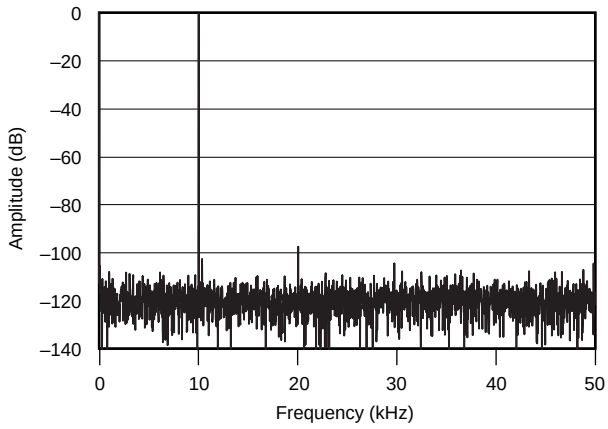
TYPICAL CHARACTERISTICS: +5V

At T_A = +25°C, $+V_{CC}$ = +5V, V_{REF} = +2.5V, f_{SAMPLE} = 100kHz, and f_{CLK} = 24 • f_{SAMPLE} = 2.4MHz, unless otherwise noted.

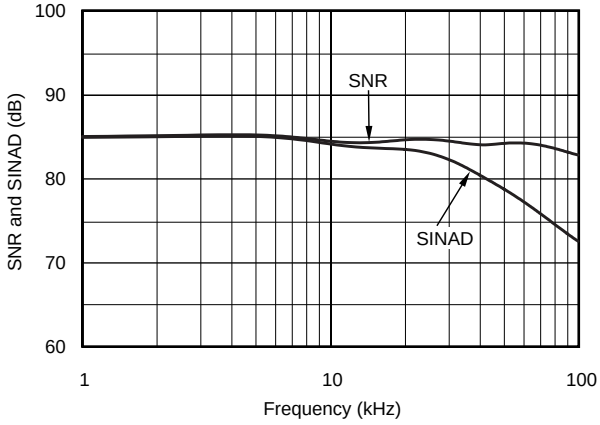
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 1.001kHz, –0.2dB)



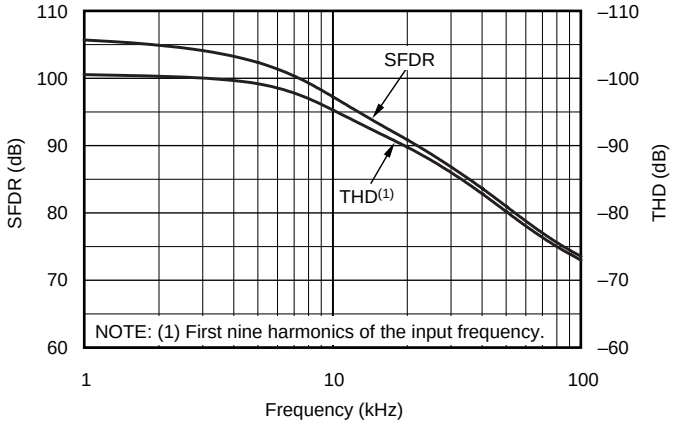
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 9.985kHz, –0.2dB)



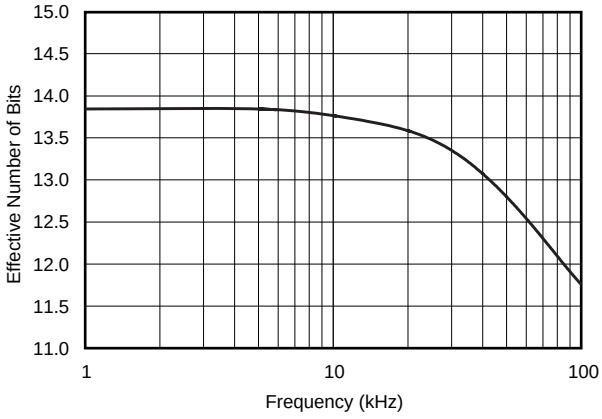
SIGNAL-TO-NOISE RATIO AND
SIGNAL-TO-(NOISE + DISTORTION)
vs INPUT FREQUENCY



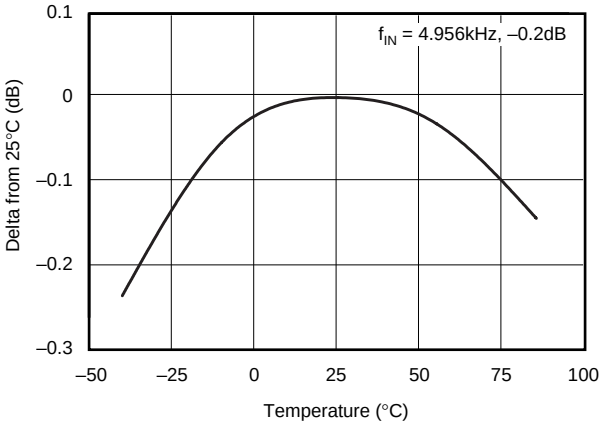
SPURIOUS-FREE DYNAMIC RANGE AND
TOTAL HARMONIC DISTORTION
vs INPUT FREQUENCY



EFFECTIVE NUMBER OF BITS
vs INPUT FREQUENCY



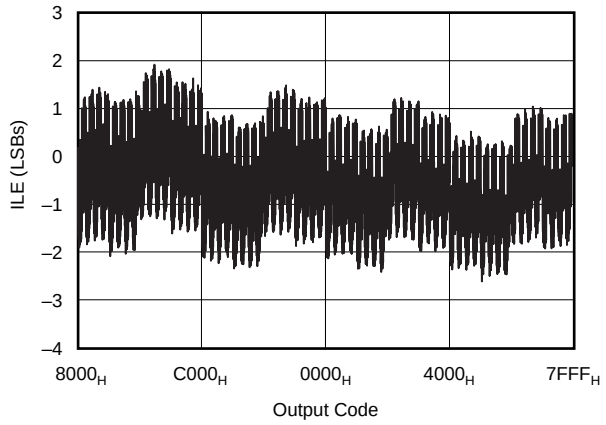
CHANGE IN SIGNAL-TO-(NOISE + DISTORTION)
vs TEMPERATURE



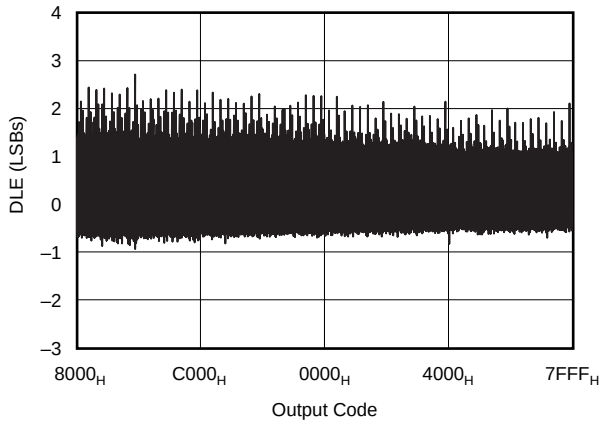
TYPICAL CHARACTERISTICS: +5V (Cont.)

At T_A = +25°C, $+V_{CC}$ = +5V, V_{REF} = +2.5V, f_{SAMPLE} = 100kHz, and f_{CLK} = 24 • f_{SAMPLE} = 2.4MHz, unless otherwise noted.

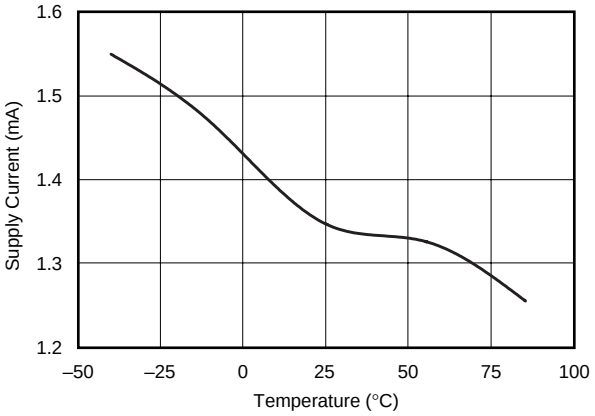
INTEGRAL LINEARITY ERROR vs CODE



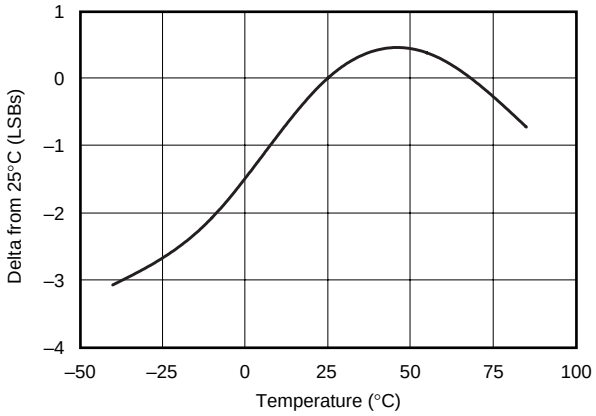
DIFFERENTIAL LINEARITY ERROR vs CODE



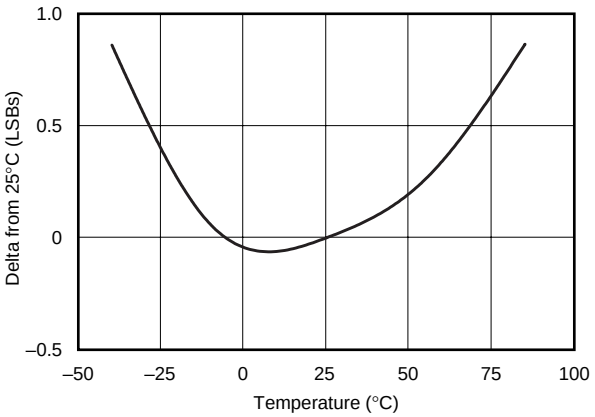
SUPPLY CURRENT vs TEMPERATURE



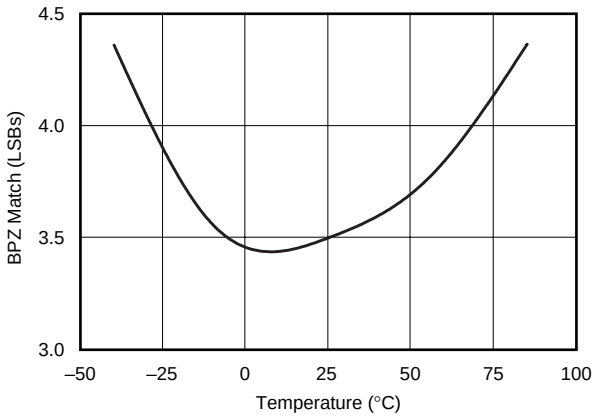
CHANGE IN BPZ vs TEMPERATURE



CHANGE IN GAIN vs TEMPERATURE



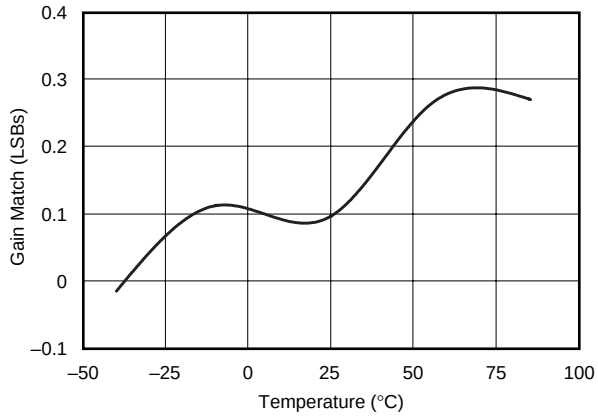
WORST-CASE CHANNEL-TO-CHANNEL
BPZ MATCH vs TEMPERATURE



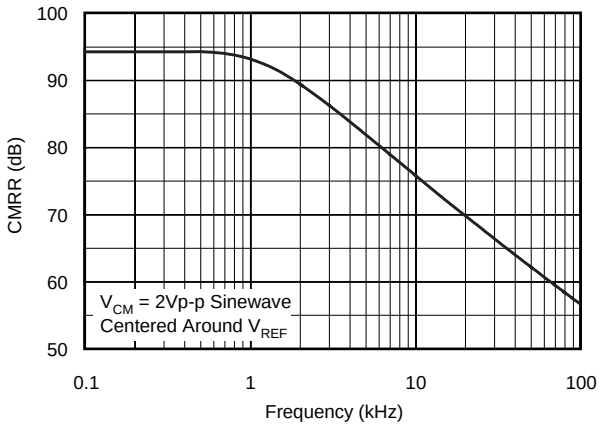
TYPICAL CHARACTERISTICS: +5V (Cont.)

At T_A = +25°C, $+V_{CC}$ = +5V, V_{REF} = +2.5V, f_{SAMPLE} = 100kHz, and f_{CLK} = 24 • f_{SAMPLE} = 2.4MHz, unless otherwise noted.

WORST CASE CHANNEL-TO-CHANNEL
GAIN MATCH vs TEMPERATURE



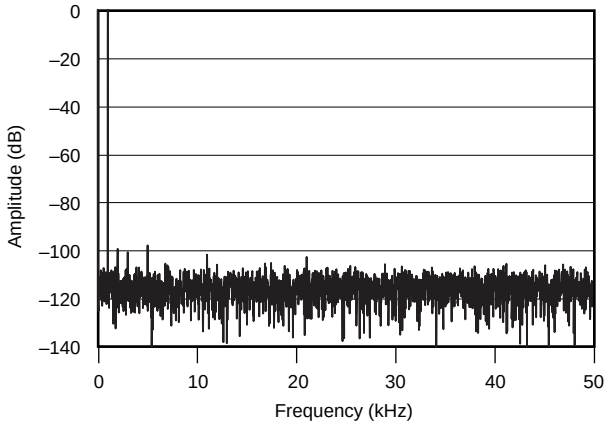
COMMON-MODE REJECTION vs FREQUENCY



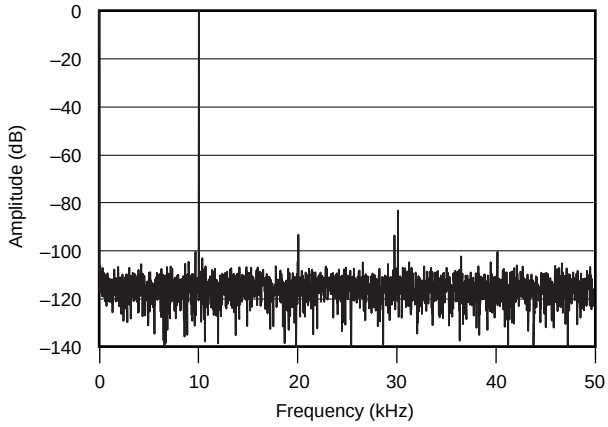
TYPICAL CHARACTERISTICS: +2.7V

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = +1.25V, f_{SAMPLE} = 100kHz, and f_{CLK} = 24 • f_{SAMPLE} = 2.4MHz, unless otherwise noted.

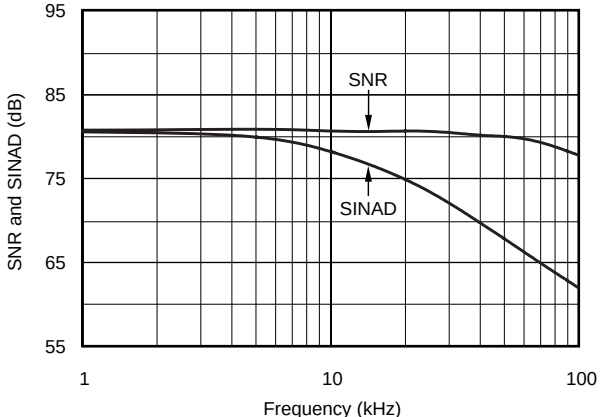
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 1.001kHz, –0.2dB)



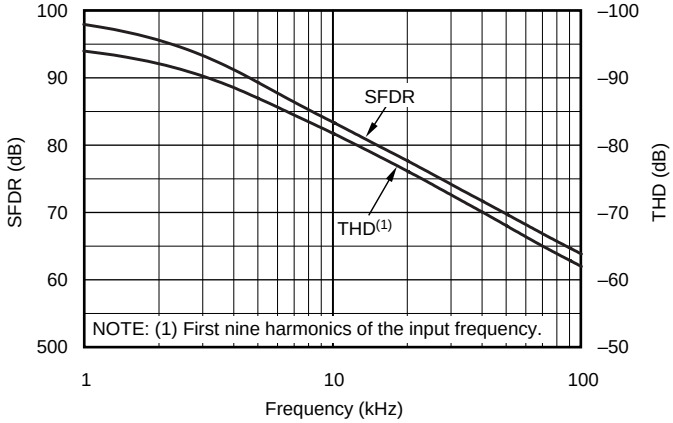
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 9.985kHz, –0.2dB)



SIGNAL-TO-NOISE RATIO AND
SIGNAL-TO-(NOISE + DISTORTION)
vs INPUT FREQUENCY



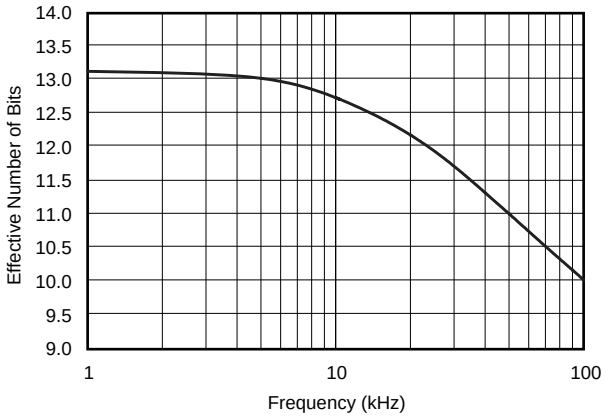
SPURIOUS-FREE DYNAMIC RANGE AND
TOTAL HARMONIC DISTORTION
vs INPUT FREQUENCY



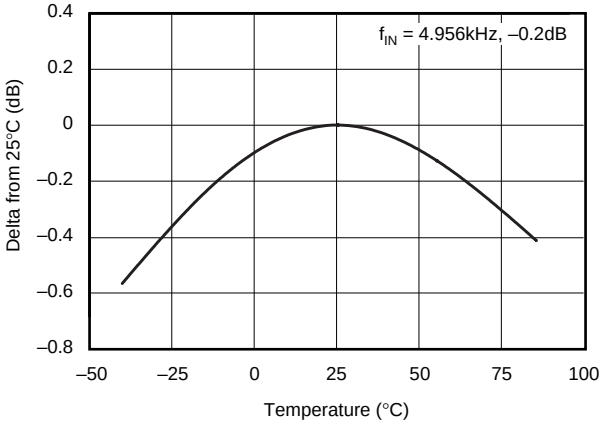
TYPICAL CHARACTERISTICS: +2.7V (Cont.)

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = +1.25V, f_{SAMPLE} = 100kHz, and f_{CLK} = 24 • f_{SAMPLE} = 2.4MHz, unless otherwise noted.

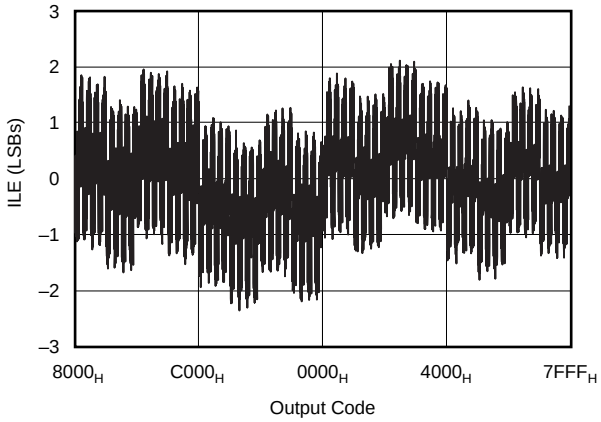
EFFECTIVE NUMBER OF BITS
vs INPUT FREQUENCY



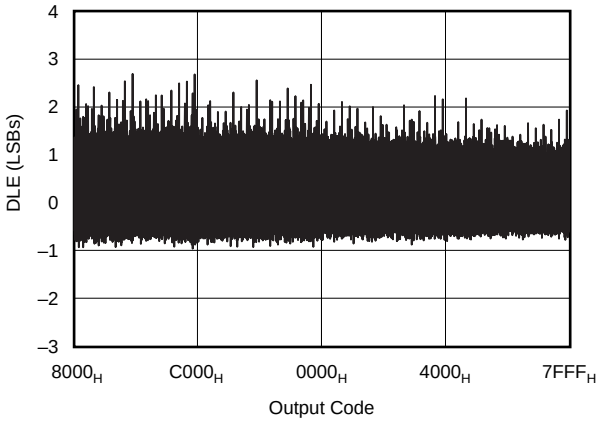
CHANGE IN SIGNAL-TO-(NOISE + DISTORTION)
vs TEMPERATURE



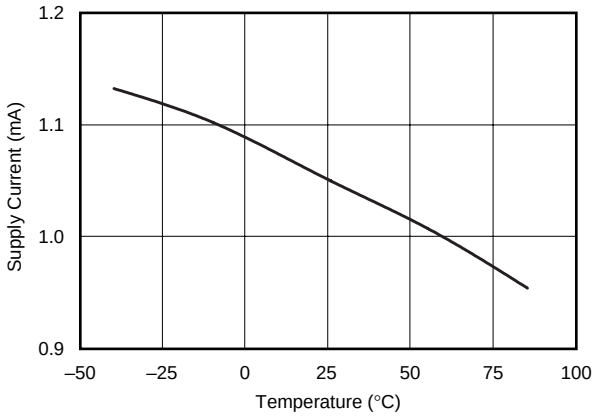
INTEGRAL LINEARITY ERROR vs CODE



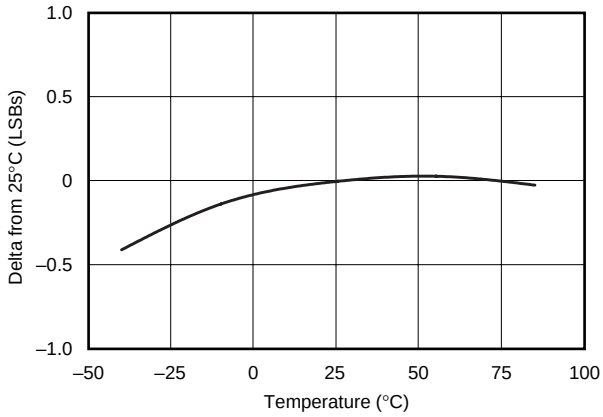
DIFFERENTIAL LINEARITY ERROR vs CODE



SUPPLY CURRENT vs TEMPERATURE



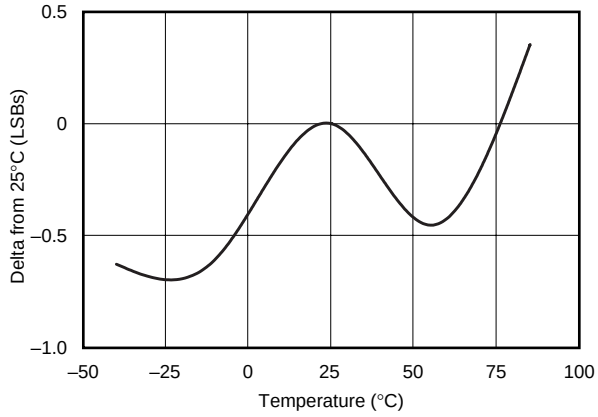
CHANGE IN BPZ vs TEMPERATURE



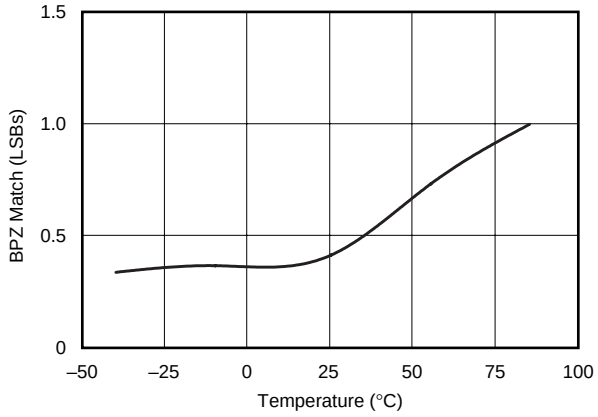
TYPICAL CHARACTERISTICS: +2.7V (Cont.)

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = +1.25V, f_{SAMPLE} = 100kHz, and f_{CLK} = 24 • f_{SAMPLE} = 2.4MHz, unless otherwise noted.

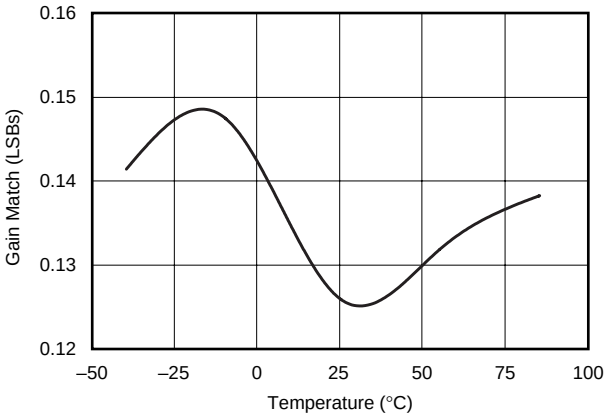
CHANGE IN GAIN vs TEMPERATURE



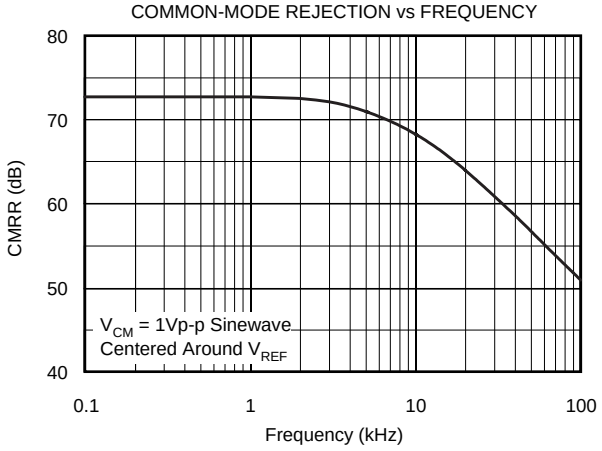
WORST-CASE CHANNEL-TO-CHANNEL BPZ MATCH vs TEMPERATURE



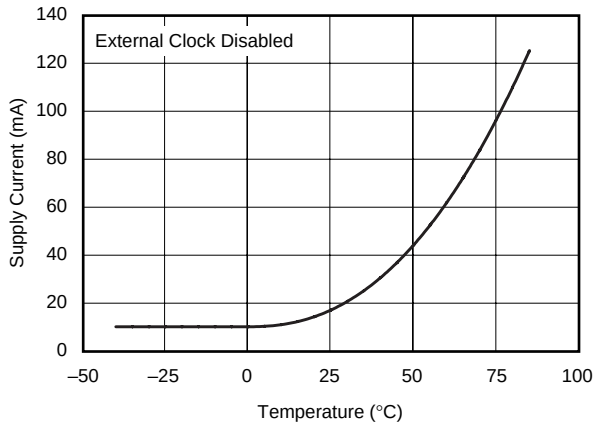
WORST-CASE CHANNEL-TO-CHANNEL GAIN MATCH vs TEMPERATURE



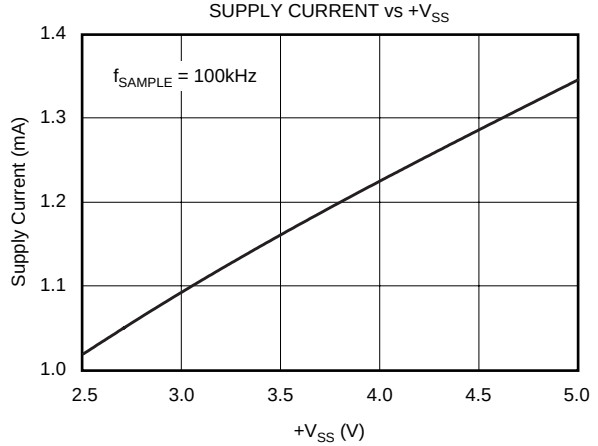
COMMON-MODE REJECTION vs FREQUENCY



POWER-DOWN SUPPLY CURRENT vs TEMPERATURE

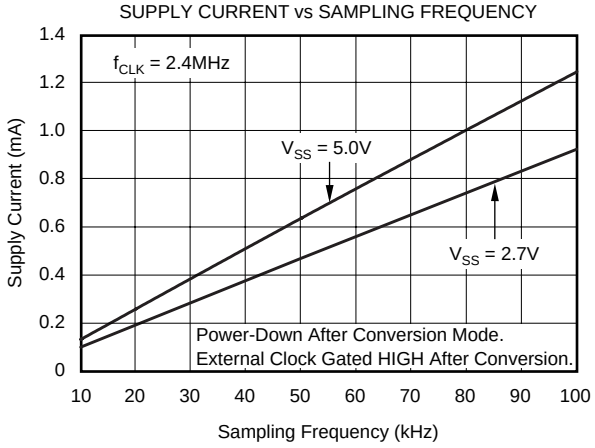


SUPPLY CURRENT vs $+V_{SS}$



TYPICAL CHARACTERISTICS: +2.7V (Cont.)

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = +1.25V, f_{SAMPLE} = 100kHz, and f_{CLK} = 24 • f_{SAMPLE} = 2.4MHz, unless otherwise noted.



THEORY OF OPERATION

The ADS8343 is a classic Successive Approximation Register (SAR) A/D converter. The architecture is based on capacitive redistribution which inherently includes a sample-and-hold function. The converter is fabricated on a 0.6µm CMOS process.

The basic operation of the ADS8343 is shown in Figure 1. The device requires an external reference and an external clock. It operates from a single supply of 2.7V to 5.25V. The external reference can be any voltage between 500mV and $+V_{CC}/2$. The value of the reference voltage directly sets the input range of the converter. The average reference input current depends on the conversion rate of the ADS8343.

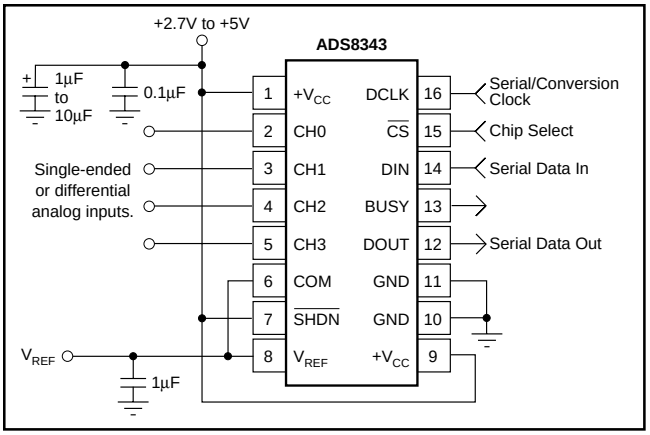


FIGURE 1. Basic Operation of the ADS8343.

The analog input to the converter is differential and is provided via a 4-channel multiplexer. The input can be provided in reference to a voltage on the COM pin (which is generally V_{REF}) or differentially by using two of the four input channels (CH0-CH3). The particular configuration is selectable via the digital interface.

ANALOG INPUT

The analog input is bipolar and fully differential. There are two general methods of driving the analog input of the ADS8343: single-ended or differential, as shown in Figure 2.

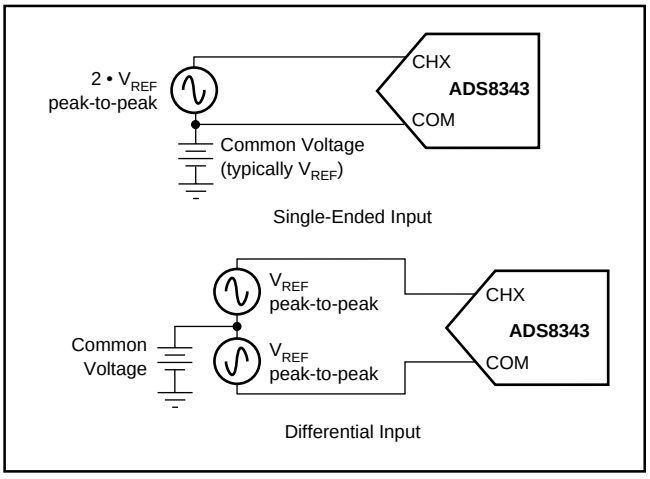


FIGURE 2. Methods of Driving the ADS8343—Single-Ended or Differential.

When the input is single-ended, the COM input is held at a fixed voltage. The CHX input swings around the same voltage and the peak-to-peak amplitude is 2 • V_{REF}. The value of V_{REF} determines the range over which the common voltage may vary, as shown in Figure 3.

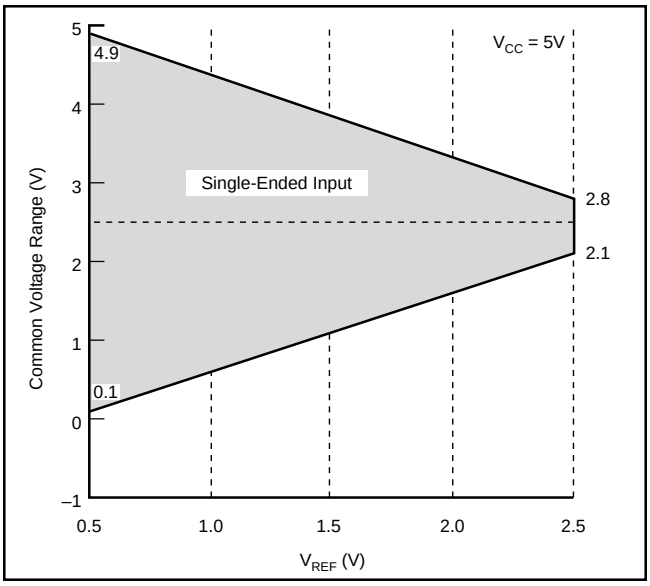


FIGURE 3. Single-Ended Input—Common Voltage Range vs V_{REF}.

When the input is differential, the amplitude of the input is the difference between the CHX and COM input. A voltage or signal is common to both of these inputs. The peak-to-peak amplitude of each input is V_{REF} about this common voltage. However, since the inputs are 180° out-of-phase, the peak-to-peak amplitude of the difference voltage is 2 • V_{REF}. The value of V_{REF} also determines the range of the voltage that may be common to both inputs, as shown in Figure 4.

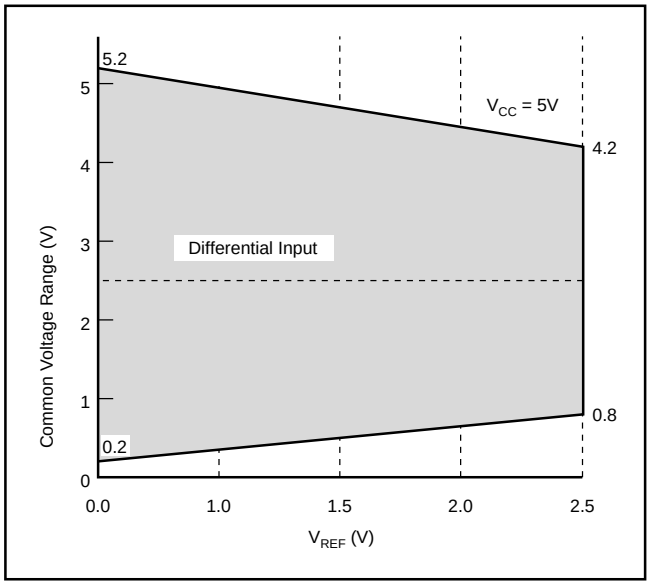


FIGURE 4. Differential Input—Common Voltage Range vs V_{REF}.

In each case, care should be taken to ensure that the output impedance of the sources driving the CHX and COM inputs are matched. If this is not observed, the two inputs could have different settling times. This may result in offset error, gain error, and linearity error which change with both temperature and input voltage. If the impedance cannot be matched, the errors can be lessened by giving the ADS8343 additional acquisition time.

The input current on the analog inputs depends on a number of factors: sample rate, input voltage, and source impedance. Essentially, the current into the ADS8343 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current.

Care must be taken regarding the absolute analog input voltage. Outside of these ranges, the converter's linearity may not meet specifications. Please refer to the electrical characteristics table for min/max ratings.

REFERENCE INPUT

The external reference sets the analog input range. The ADS8343 will operate with a reference in the range of 500mV to +V_{CC}/2. Keep in mind that the analog input is the difference between the CHX input and the COM input, as shown in Figure 5. For example, in the single-ended mode, a 1.25V reference, and with the COM pin at V_{REF}, the selected input channel (CH0-CH3) will properly digitize a signal in the range of 0V to 1.25V. If the COM pin is connected to 0.5V, the input range on the selected channel is 0.5V to 1.75V.

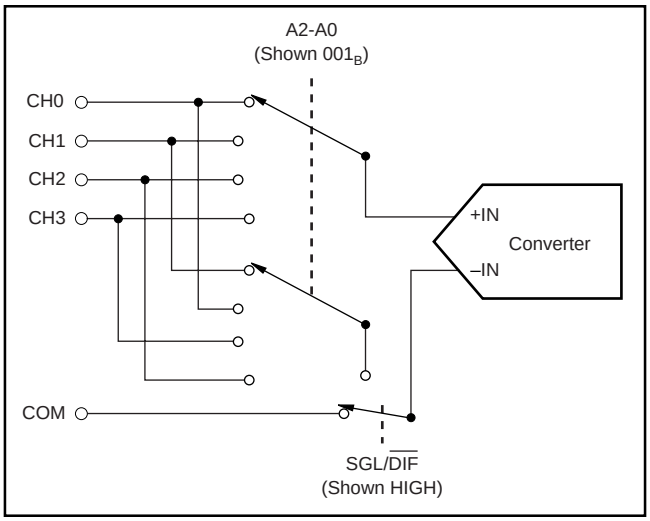


FIGURE 5. Simplified Diagram of the Analog Input.

There are several critical items concerning the reference input and its wide voltage range. As the reference voltage is reduced, the analog voltage weight of each digital output code is also reduced. This is often referred to as the LSB (Least Significant Bit) size and is equal to the reference voltage divided by 65,536. Any offset or gain error inherent in the A/D converter will appear to increase, in terms of LSB

size, as the reference voltage is reduced. For example, if the offset of a given converter is 2LSBs with a 2.5V reference, then it will typically be 10LSBs with a 0.5V reference. In each case, the actual offset of the device is the same, 76µV.

The noise or uncertainty of the digitized output will increase with lower LSB size. With a reference voltage of 500mV, the LSB size is 7.6µV. This level is below the internal noise of the device. As a result, the digital output code will not be stable and vary around a mean value by a number of LSBs. The distribution of output codes will be gaussian and the noise can be reduced by simply averaging consecutive conversion results or applying a digital filter.

With a lower reference voltage, care should be taken to provide a clean layout including adequate bypassing, a clean (low-noise, low-ripple) power supply, a low-noise reference, and a low-noise input signal. Because the LSB size is lower, the converter will also be more sensitive to nearby digital signals and electromagnetic interference.

The voltage into the V_{REF} input is not buffered and directly drives the Capacitor Digital-to-Analog Converter (CDAC) portion of the ADS8343. Typically, the input current is 13µA with a 2.5V reference. This value will vary by microamps depending on the result of the conversion. The reference current diminishes directly with both conversion rate and reference voltage. As the current from the reference is drawn on each bit decision, clocking the converter more quickly during a given conversion period will not reduce overall current drain from the reference.

DIGITAL INTERFACE

Figure 6 shows the typical operation of the ADS8343's digital interface. This diagram assumes that the source of the digital signals is a microcontroller or digital signal processor with a basic serial interface (note that the digital inputs are over-voltage tolerant up to 5.5V, regardless of $+V_{CC}$). Each communication between the processor and the converter consists of eight clock cycles. One complete conversion can be accomplished with three serial communications, for a total of 24 clock cycles on the DCLK input.

The first eight cycles are used to provide the control byte via the DIN pin. When the converter has enough information about the following conversion to set the input multiplexer appropriately, it enters the acquisition (sample) mode. After three more clock cycles, the control byte is complete and the converter enters the conversion mode. At this point, the input sample-and-hold goes into the hold mode. The next 16 clock cycles accomplish the actual A/D conversion.

Control Byte

Also shown in Figure 6 is the placement and order of the control bits within the control byte. Tables I and II give detailed information about these bits. The first bit, the 'S' bit, must always be HIGH and indicates the start of the control byte. The ADS8343 will ignore inputs on the DIN pin until the start bit is detected. The next three bits (A2-A0) select the active input channel or channels of the input multiplexer, as shown in Tables III and IV and Figure 5.

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
S	A2	A1	A0	—	SGL/$\overline{\text{DIF}}$	PD1	PD0

TABLE I. Order of the Control Bits in the Control Byte.

BIT	NAME	DESCRIPTION
7	S	Start Bit. Control byte starts with first HIGH bit on DIN.
6-4	A2-A0	Channel Select Bits. Along with the SGL/$\overline{\text{DIF}}$ bit, these bits control the setting of the multiplexer input.
2	SGL/$\overline{\text{DIF}}$	Single-Ended/Differential Select Bit. Along with bits A2-A0, this bit controls the setting of the multiplexer input.
1-0	PD1-PD0	Power-Down Mode Select Bits. See Table V for details.

TABLE II. Descriptions of the Control Bits within the Control Byte.

A2	A1	A0	CH0	CH1	CH2	CH3	COM
0	0	1	+IN				–IN
1	0	1		+IN			–IN
0	1	0			+IN		–IN
1	1	0				+IN	–IN

TABLE III. Single-Ended Channel Selection (SGL/$\overline{\text{DIF}}$ HIGH).

A2	A1	A0	CH0	CH1	CH2	CH3	COM
0	0	1	+IN	–IN			
1	0	1	–IN	+IN			
0	1	0			+IN	–IN	
1	1	0			–IN	+IN	

TABLE IV. Differential Channel Control (SGL/$\overline{\text{DIF}}$ LOW).

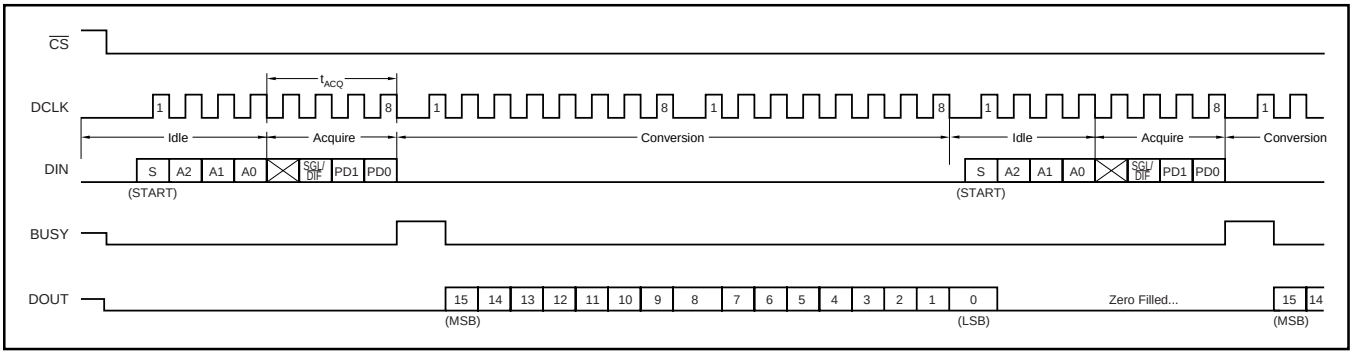


FIGURE 6. Conversion Timing, 24-Clocks per Conversion, 8-Bit Bus Interface. No DCLK delay required with dedicated serial port.

The SGL/$\overline{DIF}$ bit controls the multiplexer input mode: either single-ended (HIGH) or differential (LOW). In single-ended mode, the selected input channel is referenced to the COM pin. In differential mode, the two selected inputs provide a differential input. See Tables III and IV and Figure 5 for more information. The last two bits (PD1-PD0) select the power-down mode as shown in Table V. If both inputs are HIGH, the device is always powered up. If both inputs are LOW, the device enters a power-down mode between conversions. When a new conversion is initiated, the device will resume normal operation instantly—no delay is needed to allow the device to power up and the very first conversion will be valid.

PD1	PD0	DESCRIPTION
0	0	Power-down between conversions. When each conversion is finished, the converter enters a low-power mode. At the start of the next conversion, the device instantly powers up to full power. There is no need for additional delays to assure full operation and the very first conversion is valid.
1	0	Internal clock mode.
0	1	Reserved for future use.
1	1	No power-down between conversions, device always powered.

TABLE V. Power-Down Selection.

Clock Modes

The ADS8343 can be used with an external serial clock or an internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the device. Internal clock mode is selected when PD1 is HIGH and PD0 is LOW.

If the user decides to switch from one clock mode to the other, an extra conversion cycle will be required before the ADS8343 can switch to the new mode. The extra cycle is required because the PD0 and PD1 control bits need to be written to the ADS8343 prior to the change in clock modes.

NOTE: It is recommended that the customer write to the PD1 and PD0 registers prior to the first conversion in order to insure that the proper clock mode is selected.

External Clock Mode

In external clock mode, the external clock not only shifts data in and out of the ADS8343, it also controls the A/D conversion steps. BUSY will go HIGH for one clock period after the last bit of the control byte is shifted in. Successive-approximation bit decisions are made and appear at DOUT on each of the next 16 SCLK falling edges, see Figure 6. Figure 7 shows the BUSY timing in external clock mode.

Since one clock cycle of the serial clock is consumed with BUSY going HIGH (while the MSB decision is being made), 16 additional clocks must be given to clock out all 16 bits of data; thus, one conversion takes a minimum of 25 clock cycles to fully read the data. Since most microprocessors communicate in 8-bit transfers, this means that an additional transfer must be made to capture the LSB.

There are two ways of handling this requirement. One is presented in Figure 6, where the beginning of the next control byte appears at the same time the LSB is being clocked out of the ADS8343. This method allows for maximum throughput and 24 clock cycles per conversion.

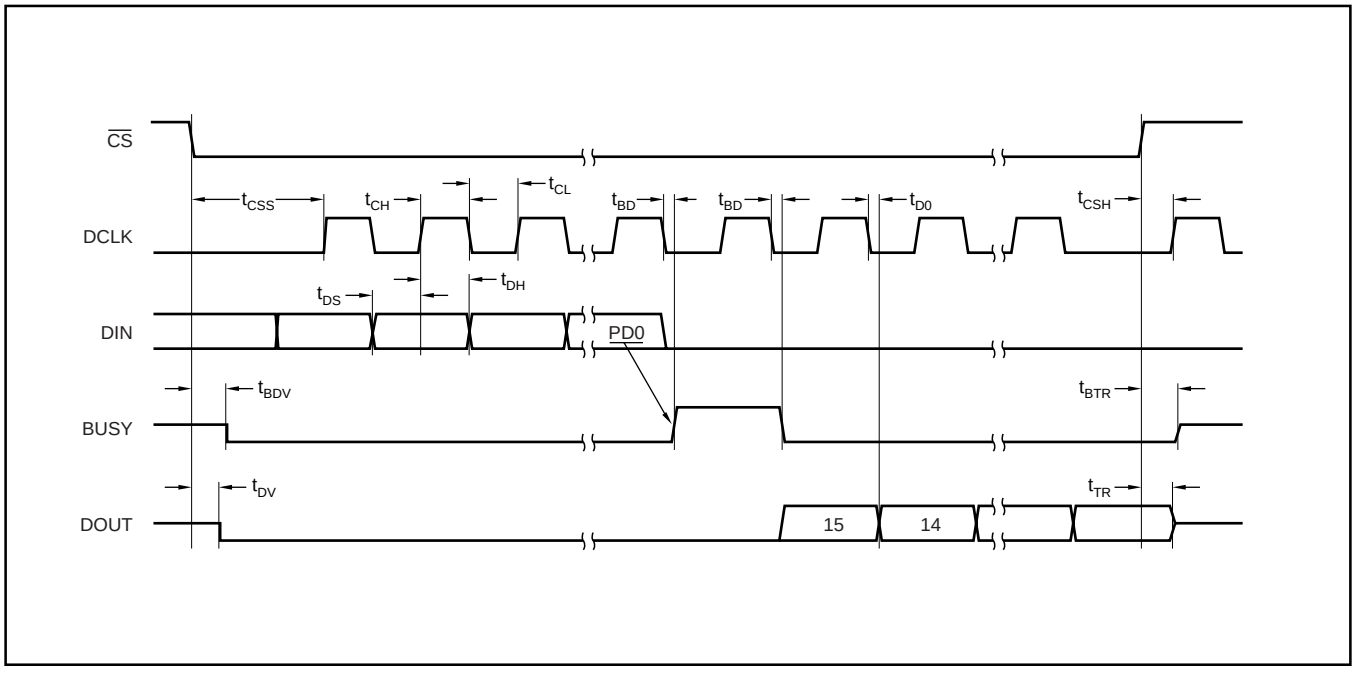


FIGURE 7. Detailed Timing Diagram.

The other method is shown in Figure 8, which uses 32 clock cycles per conversion; the last seven clock cycles simply shift out zeros on the DOUT line. BUSY and DOUT go into a high-impedance state when $\overline{CS}$ goes HIGH; after the next $\overline{CS}$ falling edge, BUSY will go LOW.

Internal Clock Mode

In internal clock mode, the ADS8343 generates its own conversion clock internally. This relieves the microprocessor from having to generate the SAR conversion clock and allows the conversion result to be read back at the processor's convenience, at any clock rate from 0MHz to 2.0MHz. BUSY goes LOW at the start of conversion and then returns HIGH when the conversion is complete. During the conversion, BUSY will remain LOW for a maximum of 8µs. Also, during the conversion, SCLK should remain LOW to achieve the best noise performance. The conversion result is stored in an internal register; the data may be clocked out of this register any time after the conversion is complete.

If $\overline{CS}$ is LOW when BUSY goes LOW following a conversion, the next falling edge of the external serial clock will write out the MSB on the DOUT line. The remaining bits (D14-D0) will be clocked out on each successive clock cycle following the MSB. If $\overline{CS}$ is HIGH when BUSY goes LOW then the DOUT line will remain in tri-state until $\overline{CS}$ goes LOW, as shown in Figure 9. $\overline{CS}$ does not need to remain LOW once a conversion has started. Note that BUSY is not tri-stated when $\overline{CS}$ goes HIGH in internal clock mode.

Data can be shifted in and out of the ADS8343 at clock rates exceeding 2.4MHz, provided that the minimum acquisition time t_{ACQ}, is kept above 1.7µs.

Digital Timing

Figure 4 and Tables VI and VII provide detailed timing for the digital interface of the ADS8343.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{ACQ}	Acquisition Time	1.5			µs
t_{DS}	DIN Valid Prior to DCLK Rising	100			ns
t_{DH}	DIN Hold After DCLK HIGH	10			ns
t_{DO}	DCLK Falling to DOUT Valid			200	ns
t_{DV}	$\overline{CS}$ Falling to DOUT Enabled			200	ns
t_{TR}	$\overline{CS}$ Rising to DOUT Disabled			200	ns
t_{CSS}	$\overline{CS}$ Falling to First DCLK Rising	100			ns
t_{CSH}	$\overline{CS}$ Rising to DCLK Ignored	0			ns
t_{CH}	DCLK HIGH	200			ns
t_{CL}	DCLK LOW	200			ns
t_{BD}	DCLK Falling to BUSY Rising			200	ns
t_{BDV}	$\overline{CS}$ Falling to BUSY Enabled			200	ns
t_{BTR}	$\overline{CS}$ Rising to BUSY Disabled			200	ns

TABLE VI. Timing Specifications ($+V_{CC}$ = +2.7V to 3.6V, T_A = –40°C to +85°C, C_{LOAD} = 50pF).

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{ACQ}	Acquisition Time	1.7			µs
t_{DS}	DIN Valid Prior to DCLK Rising	50			ns
t_{DH}	DIN Hold After DCLK HIGH	10			ns
t_{DO}	DCLK Falling to DOUT Valid			100	ns
t_{DV}	$\overline{CS}$ Falling to DOUT Enabled			70	ns
t_{TR}	$\overline{CS}$ Rising to DOUT Disabled			70	ns
t_{CSS}	$\overline{CS}$ Falling to First DCLK Rising	50			ns
t_{CSH}	$\overline{CS}$ Rising to DCLK Ignored	0			ns
t_{CH}	DCLK HIGH	150			ns
t_{CL}	DCLK LOW	150			ns
t_{BD}	DCLK Falling to BUSY Rising			100	ns
t_{BDV}	$\overline{CS}$ Falling to BUSY Enabled			70	ns
t_{BTR}	$\overline{CS}$ Rising to BUSY Disabled			70	ns

TABLE VII. Timing Specifications ($+V_{CC}$ = +4.75V to +5.25V, T_A = –40°C to +85°C, C_{LOAD} = 50pF).

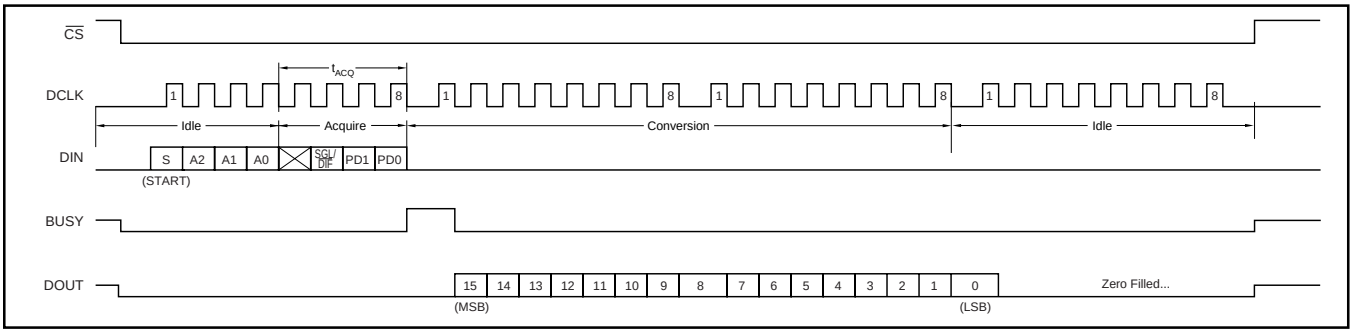


FIGURE 8. External Clock Mode 32 Clocks Per Conversion.

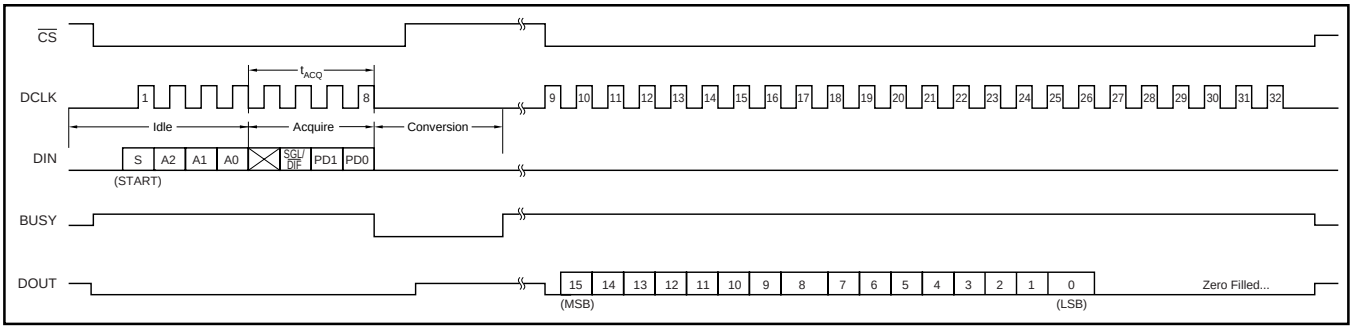


FIGURE 9. Internal Clock Mode Timing.

DATA FORMAT

The output data from the ADS8343 is in Binary Two's Complement format, as shown in Table VIII. This table represents the ideal output code for the given input voltage and does not include the effects of offset, gain, or noise.

DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT BINARY TWO'S COMPLEMENT	
Full-Scale Range	$2 \cdot V_{REF}$		
Least Significant Bit (LSB)	$2 \cdot V_{REF}/65536$	BINARY CODE	HEX CODE
+Full-Scale	$+V_{REF} - 1LSB$	0111 1111 1111 1111	7FFF
Midscale	0V	0000 0000 0000 0000	0000
Midscale – 1LSB	0V – 1LSB	1111 1111 1111 1111	FFFF
–Full-Scale	$-V_{REF}$	1000 0000 0000 0000	8000

TABLE VIII. Ideal Input Voltages and Output Codes.

POWER DISSIPATION

There are three power modes for the ADS8343: full-power (PD1 = PD0 = 1_B), auto power-down (PD1 = PD0 = 0_B), and shutdown ($\overline{SHDN}$ LOW). The affects of these modes varies depending on how the ADS8343 is being operated. For example, at full conversion rate and 24-clocks per conversion, there is very little difference between full-power mode and auto power-down, a shutdown ($\overline{SHDN}$ LOW) will not lower power dissipation.

When operating at full-speed and 24 clocks per conversion (see Figure 6), the ADS8343 spends most of its time acquiring or converting. There is little time for auto power-down, assuming that this mode is active. Thus, the difference between full-power mode and auto power-down is negligible. If the conversion rate is decreased by simply slowing the frequency of the DCLK input, the two modes remain approximately equal. However, if the DCLK frequency is kept at the maximum rate during a conversion, but conversion are simply done less often, then the difference between the two modes is dramatic. Figure 10 shows the difference between reducing the DCLK frequency ("scaling" DCLK to match the conversion rate) or maintaining DCLK at the highest frequency and reducing the number of conversion per second. In the later case, the converter spends an increasing percentage of its time in power-down mode (assuming the auto power-down mode is active).

If DCLK is active and $\overline{CS}$ is LOW while the ADS8343 is in auto power-down mode, the device will continue to dissipate some power in the digital logic. The power can be reduced to a minimum by keeping $\overline{CS}$ HIGH. The differences in supply current for these two cases are shown in Figure 11.

Operating the ADS8343 in auto power-down mode will result in the lowest power dissipation, and there is no conversion time "penalty" on power-up. The very first conversion will be valid. $\overline{SHDN}$ can be used to force an immediate power-down.

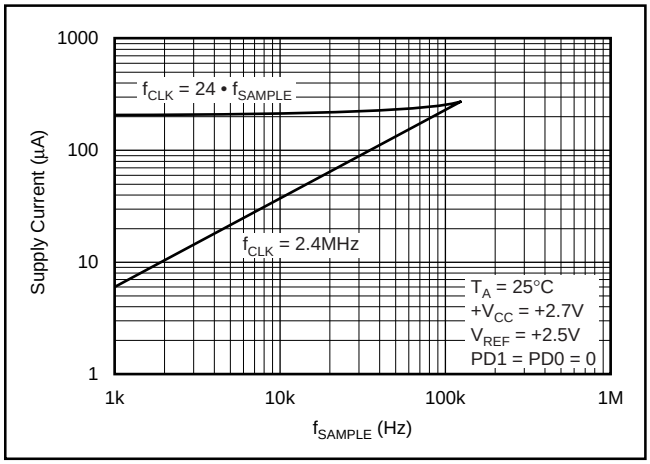


FIGURE 10. Supply Current versus Directly Scaling the Frequency of DCLK with Sample Rate or Keeping DCLK at the Maximum Possible Frequency.

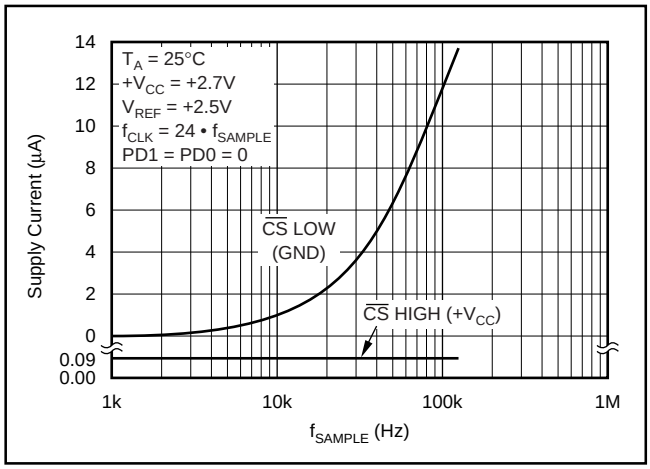


FIGURE 11. Supply Current vs State of $\overline{CS}$.

NOISE

The noise floor of the ADS8343 itself is extremely low, as can be seen from Figures 12 and 13, and is much lower than competing A/D converters. The ADS8343 was tested at both 5V and 2.7V and in both the internal and external clock modes. A low-level DC input was applied to the analog input pins and the converter was put through 5000 conversions. The digital output of the A/D converter will vary in output code due to the internal noise of the ADS8343. This is true for all 16-bit, SAR-type, A/D converters. Using a histogram to plot the output codes, the distribution should appear bell-shaped with the peak of the bell curve representing the nominal code for the input value. The ±1σ, ±2σ, and ±3σ distributions will represent the 68.3%, 95.5%, and 99.7%, respectively, of all codes. The transition noise can be calculated by dividing the number of codes measured by 6 and this will yield the ±3σ distribution or 99.7% of all codes. Statistically, up to 3 codes could fall outside the distribution when executing 1000 conversions. The ADS8343, with < 3 output codes for the ±3σ distribution, will yield a < ±0.5LSB transition noise at 5V operation. Remember, to achieve this low noise performance, the peak-to-peak noise of the input signal and reference must be < 50µV.

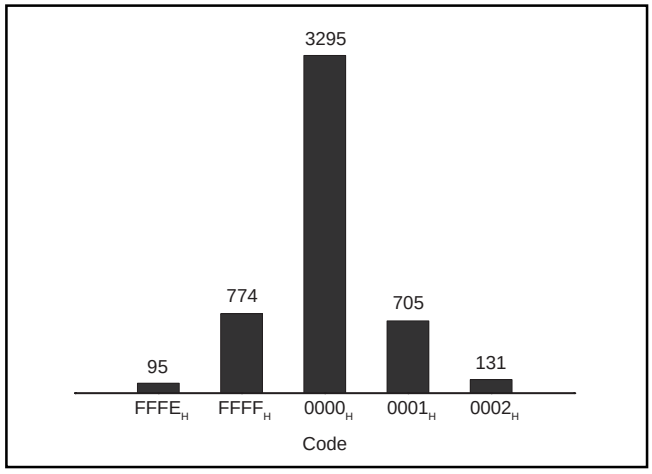


FIGURE 12. Histogram of 5000 Conversions of a DC Input at the Code Transition, 5V Operation External Clock Mode.

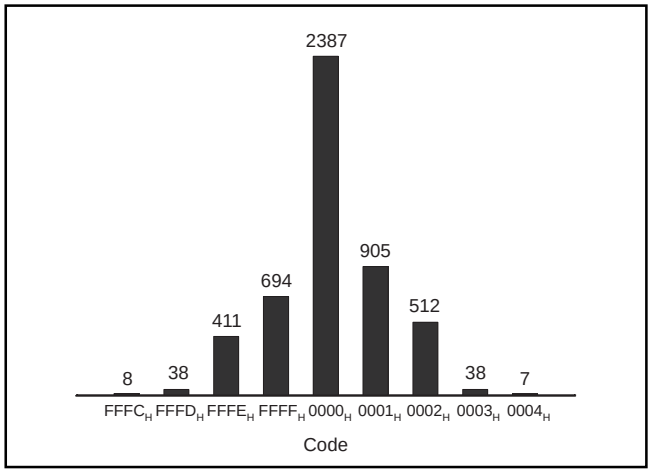


FIGURE 13. Histogram of 5000 Conversions of a DC Input at the Code Center, 2.7V Operation Internal Clock Mode.

AVERAGING

The noise of the A/D converter can be compensated by averaging the digital codes. By averaging conversion results, transition noise will be reduced by a factor of $1/\sqrt{n}$, where n is the number of averages. For example, averaging 4 conversion results will reduce the transition noise by 1/2 to ±0.25LSBs. Averaging should only be used for input signals with frequencies near DC.

For AC signals, a digital filter can be used to low-pass filter and decimate the output codes. This works in a similar manner to averaging; for every decimation by 2, the signal-to-noise ratio will improve 3dB.

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS8343 circuitry. This is particularly true if the reference voltage is low and/or the conversion rate is high.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Thus, during any single conversion for an n-bit SAR converter, there are n "windows" in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high-power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the DCLK input.

With this in mind, power to the ADS8343 should be clean and well bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1µF to 10µF capacitor and a 5Ω or 10Ω series resistor may be used to low-pass filter a noisy supply.

The reference should be similarly bypassed with a 1µF capacitor. Again, a series resistor and large capacitor can be used to low-pass filter the reference voltage. If the reference voltage originates from an op amp, make sure that it can drive the bypass capacitor without oscillation (the series resistor can help in this case). The ADS8343 draws very little current from the reference on average, but it does place larger demands on the reference circuitry over short periods of time (on each rising edge of DCLK during a conversion).

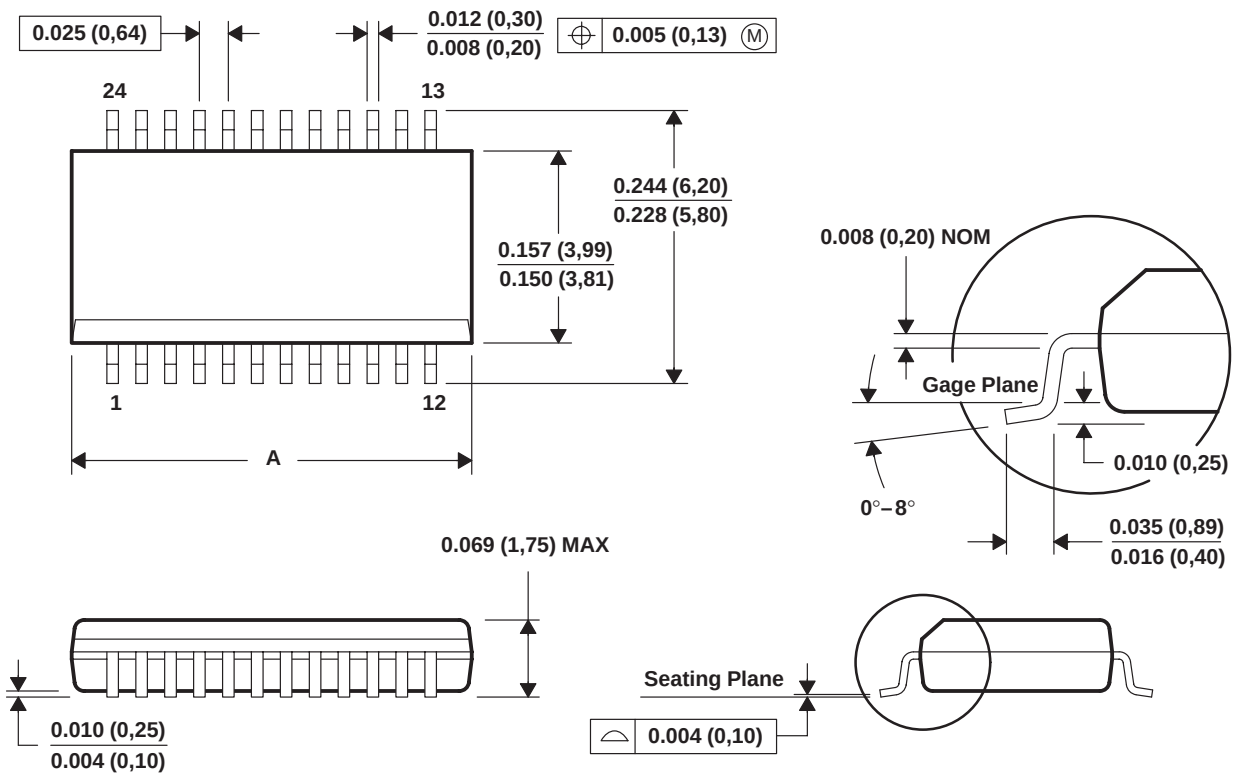
The ADS8343 architecture offers no inherent rejection of noise or voltage variation in regards to the reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results. While high-frequency noise can be filtered out as discussed in the previous paragraph, voltage variation due to line frequency (50Hz or 60Hz) can be difficult to remove.

The GND pin should be connected to a clean ground point. In many cases, this will be the "analog" ground. Avoid connections which are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power-supply entry point. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

PACKAGE DRAWING

DBQ (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.197 (5,00)	0.344 (8,74)	0.344 (8,74)	0.394 (10,01)
A MIN	0.188 (4,78)	0.337 (8,56)	0.337 (8,56)	0.386 (9,80)

4073301/E 10/00

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-137

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