

ARX4810 & 4810FP Universal Dual Transceivers for MIL-STD-1553 & MACAIR A3818, A5690, A5232 & A4905

Features

- World's smallest dual "Universal Transceiver" 0.3" X 1.2" Package
- Dual transceiver meets military data bus requirements, MIL-STD-1553 and Macair specs
- Low power dissipation at full output power
- +5 / -15 Volt Power Supply Operation
- Voltage source output for higher bus drive power
- Monolithic construction using linear ASICs
- Processed and screened to MIL-STD-883 specs
- MIL-PRF-38534 Compliant Devices Available
- DESC SMD (Standard Military Drawing)



General Description

The Aeroflex Circuit Technology Models ARX4810 and ARX4810FP are new generation monolithic transceivers which provide full compliance with MIL-STD-1553 and Macair data bus requirements in the smallest packages with low power consumption and two power supply operation.

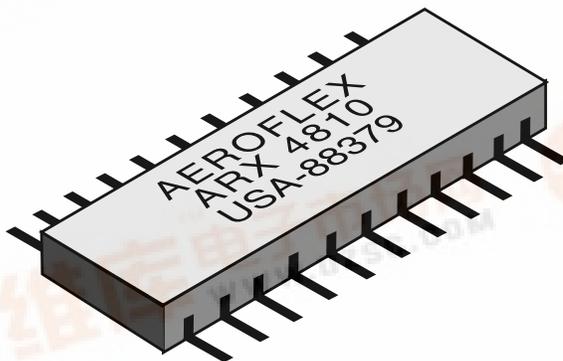
The dual channel Model ARX4810 and Model ARX4810FP perform the front-end analog function of inputting and outputting data through a transformer to a MIL-STD-1553 or Macair data bus.

Design of these transceivers reflects particular attention to active filter performance. This results in low bit and word error rate with superior waveform purity and minimal zero crossover distortion. Efficient transmitter electrical and thermal design provides low internal power dissipation and heat rise at high as well as low duty cycles.

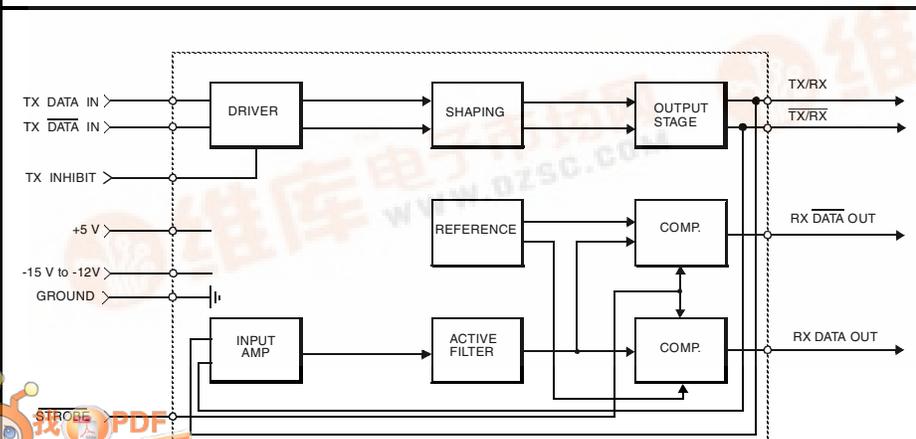
Each channel of the dual transceiver is completely separate from the other and fully independent. This includes power leads as well as signal lines. Hence, each channel may be connected to a different data bus with no interaction.

Transmitter

The Transmitter section accepts bi-phase TTL data at the input and when coupled to the data bus with a 1:1 transformer, isolated on the data bus side with two 52.5 Ohm fault isolation resistors, and loaded by two



ARX4810 Dual Universal Transceiver



Block Diagram (without transformer), 1/2 of unit shown

70 Ohm terminations plus additional receivers, the data bus signal produced is 7.5 volts nominal P-P at A-A'. (See Figure 5) When both DATA and $\overline{\text{DATA}}$ inputs are held low or high, the transmitter output becomes a high impedance and is "removed" from the line. In addition, an overriding "INHIBIT" input provides for the removal of the transmitter output from the line. A logic "1" applied to the "INHIBIT" takes priority over the condition of the data inputs and disables the transmitter. (See Transmitter Logic Waveform, Figure 1.)

The transceiver utilizes an active filter to suppress harmonics above

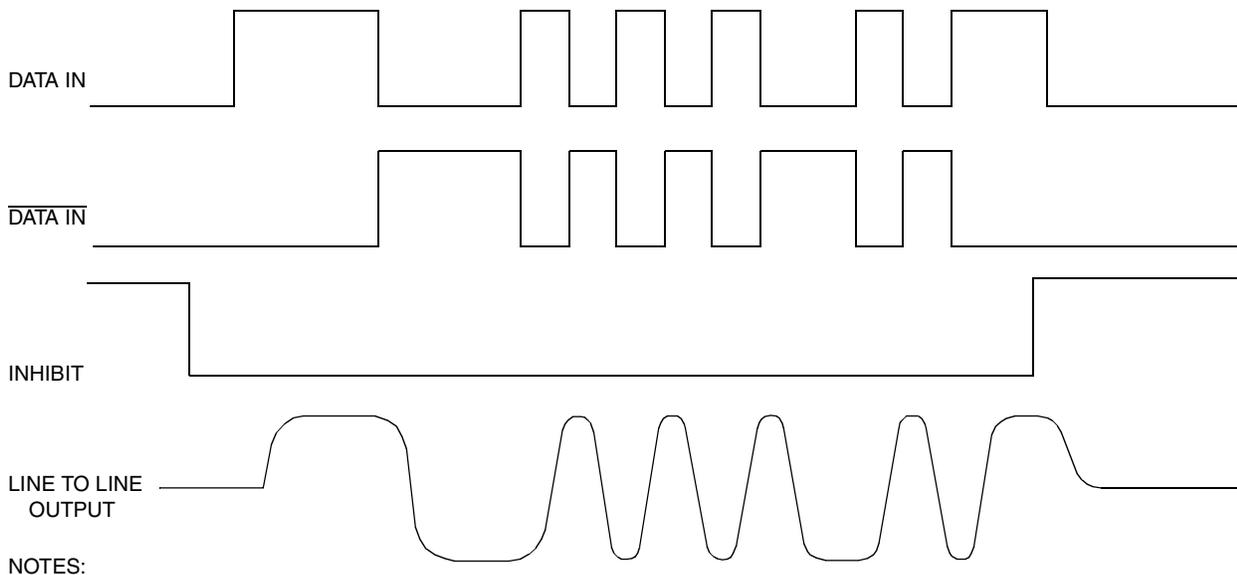
1 MHz to meet Macair specifications A-3818, A-4905, A-5232 and A-5690. The Transmitter may be safely operated at 100% duty cycle for an indefinite period into a short circuited, the 1553 or Macair bus.

Receiver

The Receiver section accepts bi-phase differential data at the input and produces two TTL signals at the output. The outputs are DATA and $\overline{\text{DATA}}$, and represent positive and negative excursions of the input beyond a pre-determined threshold. (See Receiver Logic Waveform Figure 2).

The pre-set internal thresholds will detect data bus signals exceeding 1.150 Volts P-P and reject signals less than 0.6 volts P-P when used with a 1:1 turns ratio transformer. (See Figure 5 for transformer data and typical connection.)

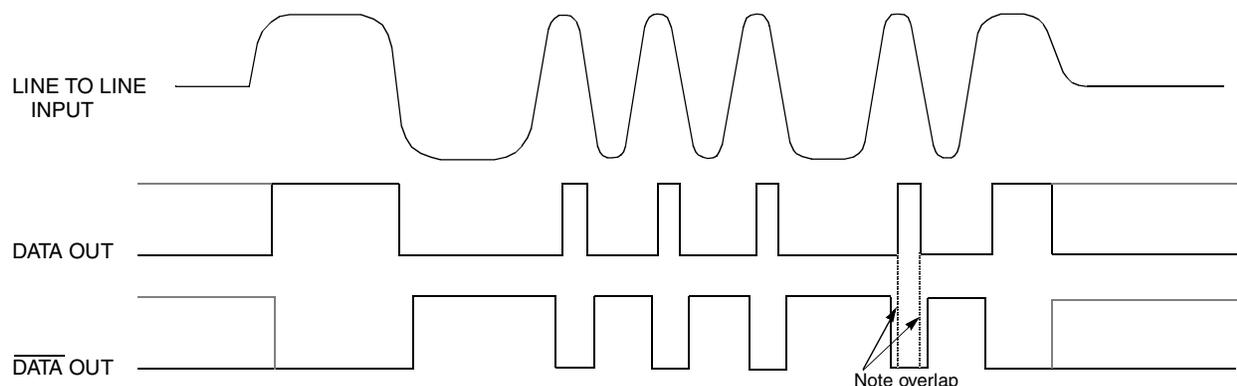
Figure 1 – Transmitter Logic Waveforms



NOTES:

1. DATA and $\overline{\text{DATA}}$ inputs must be complementary waveforms or 50% duty cycle average, with no delays between them.
2. DATA and $\overline{\text{DATA}}$ must be in the same state during off time (both high or low).

Figure 2 – Receiver Logic Waveforms



NOTE: Waveforms shown are for normally low devices. For normally high receiver output level devices, the receiver outputs are swapped as shown by the dashed lines.

Absolute Maximum Ratings

Operating case temperature	-55°C to +125°C
Storage case temperature	-65°C to +150 °C
Negative Power supply Voltage	-15 V P.S. to -18V MAX
Positive Power Supply Voltage	-0.3 V to +5.5 V
Receiver differential input	±10 V
Receiver input voltage (common mode)	±5 V
Driver peak output current	300 mA
Total package power dissipation over the full operating case temperature rise	4 Watts (Note. Normal operation conditions require one transmitter on and the other off at any given time, with a maximum dissipation of 3.2 watts.)
Maximum junction to case temperature rise for the hottest device	6° C
Thermal resistance for the hottest device, junction to bottom of case	3° C/W

Electrical Characteristics, Driver Section

Input Characteristics, TX DATA in or TX DATA in

Parameter	Condition	Symbol	Min	Typ	Max	Unit
"0" Input Current	V _{IN} = 0.4 V	I _{ILD}		-0.25	-0.4	mA
"1" Input Current	V _{IN} = 2.7 V	I _{IHD}		1	40	μA
"0" Input Voltage		V _{IHD}			0.7	V
"1" Input Voltage		V _{IHD}	2.0			V

Inhibit Characteristics

"0" Input Current	V _{IN} = 0.4V	I _{ILI}		-0.25	-0.4	mA
"1" Input Current	V _{IN} = 2.7V	I _{IHI}		1.0	40	μA
"0" Input Voltage		V _{ILI}			0.7	V
"1" Input Voltage		V _{IHI}	2			V
Delay from TX inhibit,(0→1) to inhibited output	Note 1	t _{DXOFF}		240	350	nS
Delay from TX inhibit, (1→0) to active output	Note 1	t _{DXON}		210	350	nS
Differential output noise, inhibit mode		V _{NOI}		2	10	mV p-p
Differential output impedance (inhibited)	Note 2	Z _{OI}	7K			Ω

Note 1. Characteristics guaranteed by design, not production tested .

Output Characteristics

Differential output level	R _L = 35Ω	V _O	6	6.8	7.7	V p-p
Rise and fall times (10% to 90% of p-p output)		t _R	200	240	300	nS
Output offset at point A-A' on Fig 5., 2.5 μS after midpoint crossing of the parity bit of the last word of a 660μS message	R _L = 35Ω	V _{OS}			±90	mV peak
Delay from 50% point of TX DATA or TX DATA input to zero crossing of differential signal	Note 1	t _{DTX}		260	350	nS

Note 2. Measured at 1MHz from bus side of transformer after contribution from transformer is accounted for.

Electrical Characteristics, Receiver Section

Parameter	Condition	Sym	Min	Typ	Max	Unit
Differential Input Impedance	f = 1MHz	Z _{IN}	20K			Ω
Differential Voltage Range		VIDR			±4	V peak
Input Common Mode Voltage Range	Note 1	V _{ICR}	±2.5			V peak
Common Mode Rejection Ratio Note 3	Note 1	CMRR	40			dB

Strobe Characteristics (Logic "0" inhibits output) if not used, a 1K pullup to 5 V is recommended

"0" Input Current	V _s = 0.4 V	I _{IL}		-0.25	-0.4	mA
"1" Input Current	V _s = 2.7V	I _{IH}		1	+40	μA
"0" Input Voltage		V _{IL}			0.7	V
"1" Input Voltage		V _{IH}	2.0			V
Strobe Delay (turn-on or turn-off)	Note 1	t _{SD}		10	78	nS

Threshold Characteristics (Sinewave input)

Input Threshold Voltage (referred to the bus)	100KHz-1MHz	V _{TH}	0.60	0.8	1.15	V _{P-P}
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Output Characteristics, RX DATA and RX DATA

"1" State	I _{OH} = -0.4 mA	V _{OH}	2.5	3.4		V
"0" State	I _{OL} = 4 mA	V _{OL}		0.3	0.5	V
Delay, (average) from differential input zero crossings to RX DATA and RX DATA output 50% points		t _{DRX}		280	450	nS

Power Data

Maximum Currents, per channel (Power supplies used are -15V, and +5V)

Duty Cycle	-V	+V and Logic
Transmitter Standby	42 mA	48 mA
25% duty cycle, Note 1	85mA	90 mA
50% duty cycle	105 mA	110 mA
100% duty cycle, Note 1	140 mA	145 mA

Power supply Voltages

-V	-14.25 Volts to -15.75 Volts
Logic and +V	4.5 Volts to 5.5 Volts

Note 3. Measured at the bus side of the transformer, including the contribution from the transformer.

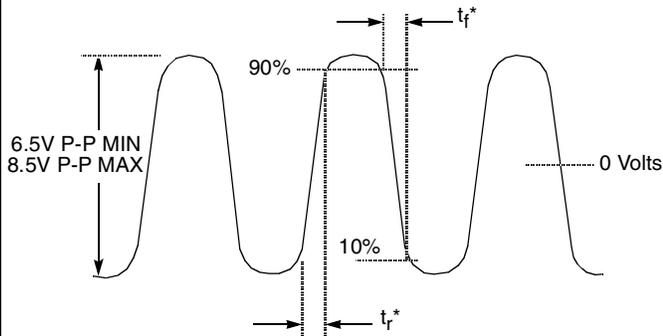
Note 4. V_{cc} = 5 Volts ±0.1 V, for all measurements unless otherwise specified.

Note 5. Specifications apply over the case temperature range of -55°C to +125°C unless otherwise specified.

Note 6. All typical values are measured at +25°C

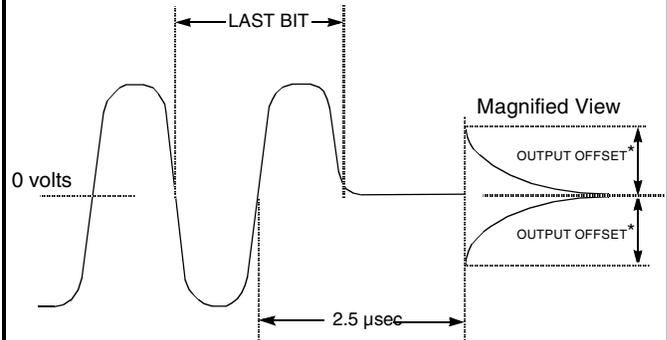
Note 7. A 1uf, 10 Volt capacitor is required on the TX/RX terminal for each transceiver as shown in Figure 5. A Sprague 194D type (.05" W x .10" L x .05" H) is suggested.

Figure 3 – Transmitter (TX) Output Wave form



* Rise and fall times measured at point A-A' in Fig 5

Figure 4 – Transmitter (TX) Output offset



*Offset measured at point A-A' in Fig 5

Figure 5 – Typical Transformer connection

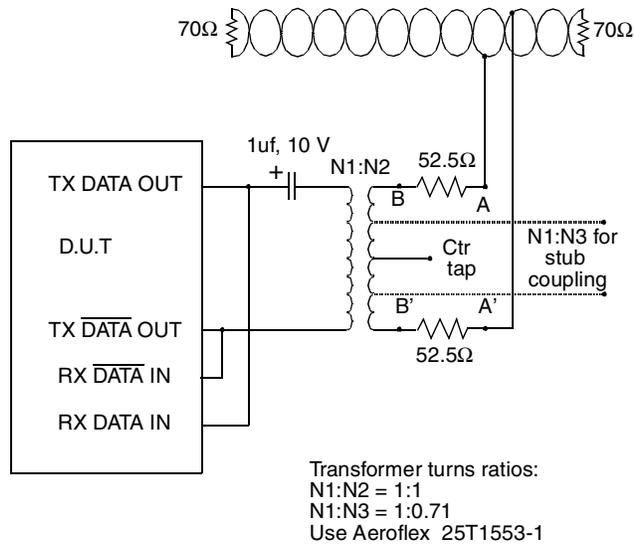
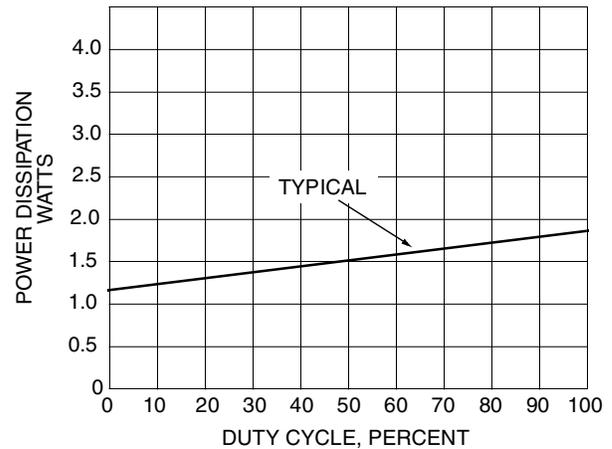


Figure 6 – Power Dissipation vs. Duty Cycle (per channel)

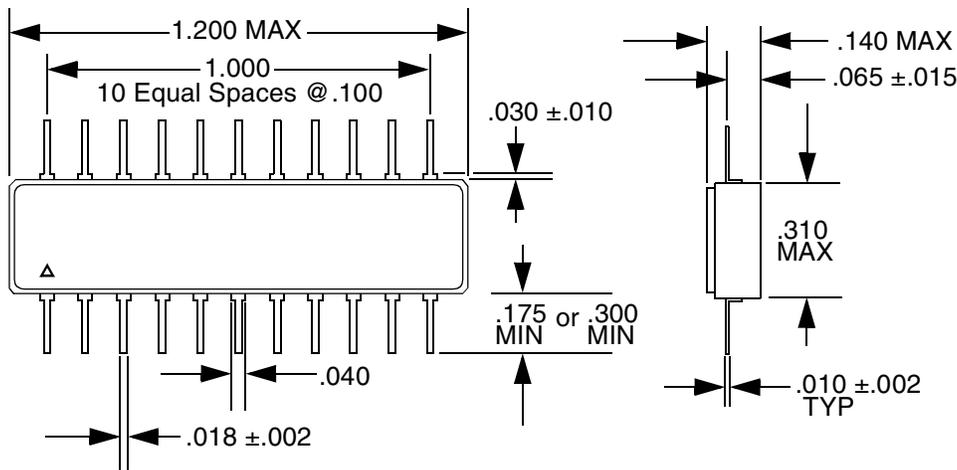


Configurations and Ordering Information

Model No.	DESC No.	Receiver Data level	Case	Configuration
ARX4810	5962-TBA	Normally High	Plug-In	Dual
ARX4810-201-1	5962-9550501HXC	Normally High	Flat Pkg (.175 Lead)	Dual
ARX4810-201-2	5962-9550501HXA	Normally High	Flat Pkg (.175 Lead)	Dual
ARX4810-201-3	5962-9550501HXA or C	Normally High	Flat Pkg (.175 Lead)	Dual
ARX4810-203-1	5962-9550501HYC	Normally High	Flat Pkg (.300 Lead)	Dual
ARX4810-203-2	5962-9550501HYA	Normally High	Flat Pkg (.300 Lead)	Dual
ARX4810-203-3	5962-9550501HYA or C	Normally High	Flat Pkg (.300 Lead)	Dual
ARX4811	5962-TBA	Normally Low	Plug-In	Dual
ARX4811-2	5962-TBA	Normally Low	Flat Package	Dual

Package Dimensions and Pin Outs

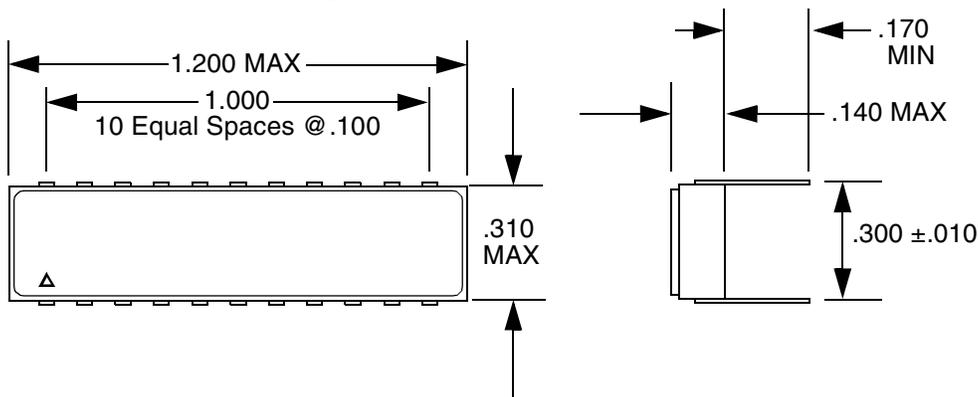
Flat Package



Pin Numbers & Functions

Pin #	Function	Channel
1	INHIBIT	A
2	TX DATA IN	A
3	TX DATA IN	A
4	STROBE	A
5	GROUND	A
6	RX DATA OUT	B
7	RX DATA OUT	B
8	TX / RX	B
9	TX / RX	B
10	-15V	B
11	+5V	B
12	INHIBIT	B
13	TX DATA IN	B
14	TX DATA IN	B
15	STROBE	B
16	GROUND	B
17	RX DATA OUT	A
18	RX DATA OUT	A
19	TX / RX	A
20	TX / RX	A
21	-15V	A
22	+5V	A

DIP Package



Notes
1. Dimensions shown are in inches

Specifications subject to change without notice.