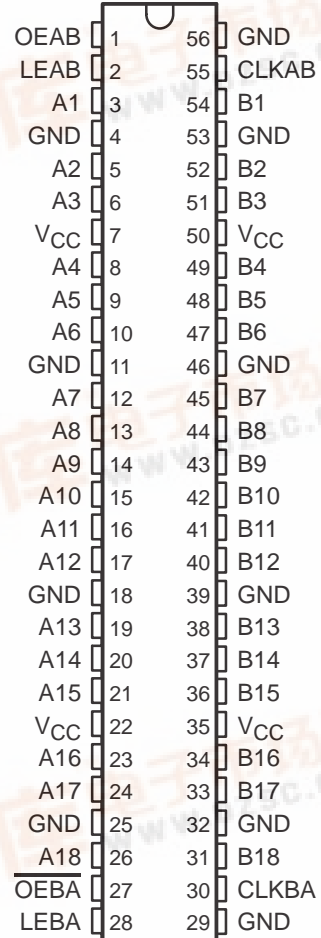


SN54ABT162501/SN74ABT162501 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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- **Members of the Texas Instruments *Widebus*™ Family**
- **B-Port Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art *EPIC-II B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$**
- **High-Impedance State During Power Up and Power Down**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54ABT162501 . . . WD PACKAGE
SN74ABT162501 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

These 18-bit universal bus transceivers consist of storage elements that can operate either as D-type latches or D-type flip-flops to allow data flow in transparent or clocked modes.

Data flow in each direction is controlled by output-enable ($\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA. The output enables are complementary (OEAB is active high and $\overline{\text{OEBA}}$ is active low).

The B-port outputs, which are designed to source or sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

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description (continued)

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, \overline{OE} should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

The SN54ABT162501 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT162501 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B_0^{\ddagger}
H	L	L	X	B_0^{\S}

† A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

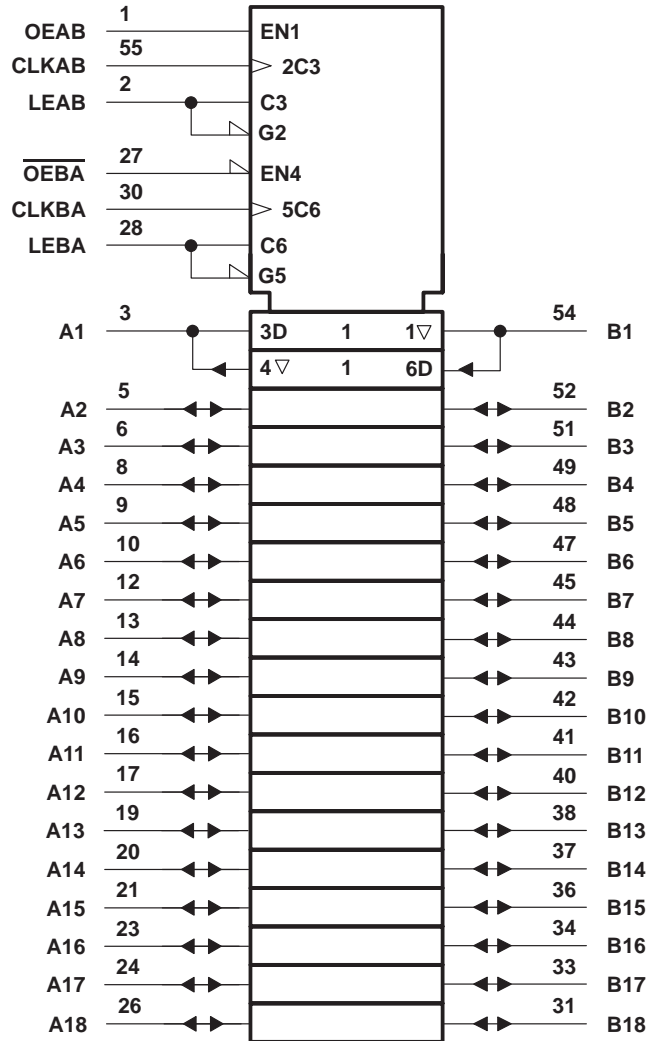
‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low

§ Output level before the indicated steady-state input conditions were established

SN54ABT162501, SN74ABT162501 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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logic symbol†

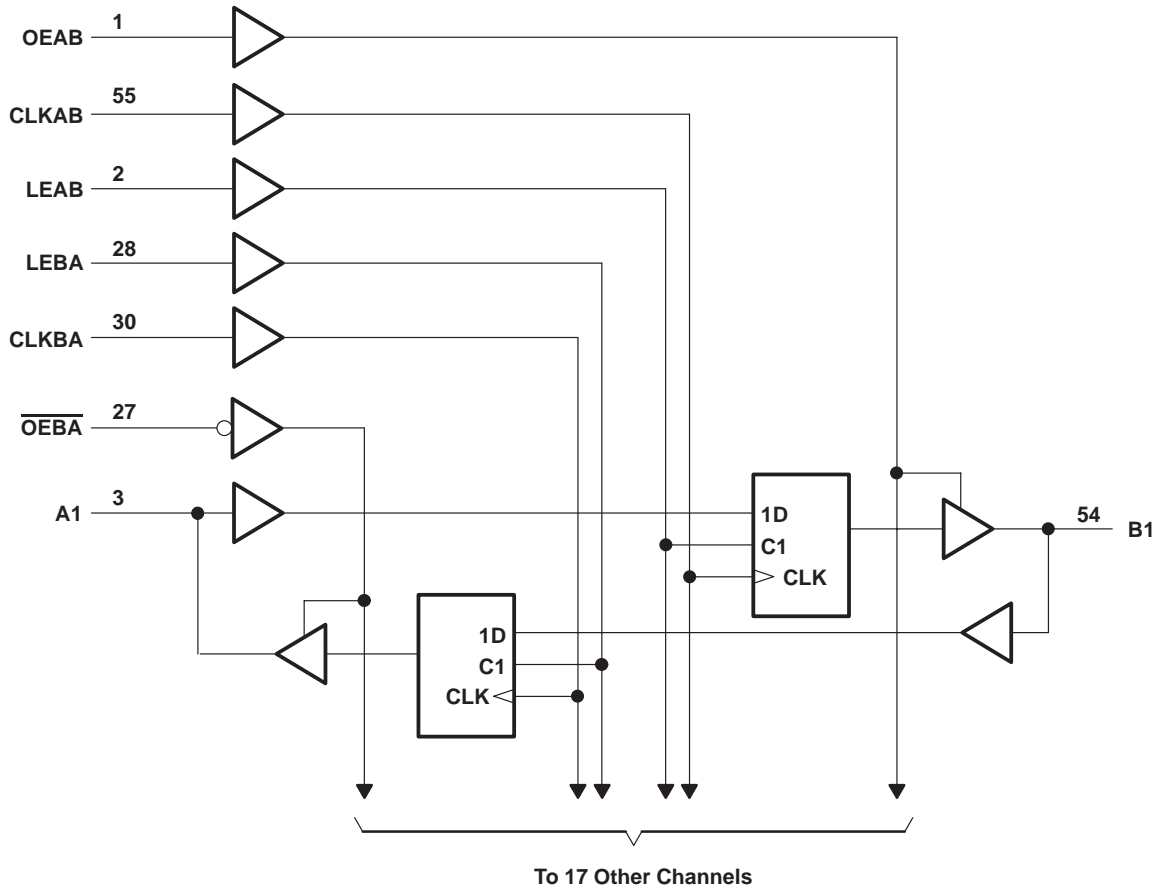


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	-0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT162501 (A port)	96 mA
SN74ABT162501 (A port)	128 mA
B port	30 mA
Input clamp current, I_{IK} ($V_I < 0$)	-18 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

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recommended operating conditions (see Note 3)

		SN54ABT162501		SN74ABT162501		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	A port		-24		mA
		B port		-12		
I _{OL}	Low-level output current	A port		48		mA
		B port		12		
Δt/Δv	Input transition rise or fall rate		10		10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate	200		200		μs/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54ABT162501, SN74ABT162501

18-BIT UNIVERSAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54ABT162501		SN74ABT162501		UNIT	
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2		-1.2		-1.2	V	
V_{OH}	A port	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -3\text{ mA}$	2.5		2.5		2.5		V	
		$V_{CC} = 5\text{ V}$, $I_{OH} = -3\text{ mA}$	3		3		3			
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -24\text{ mA}$	2		2			2		
		$I_{OH} = -32\text{ mA}$	2*					2		
	B port	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -1\text{ mA}$	3.35		3.3		3.35			
		$V_{CC} = 5\text{ V}$, $I_{OH} = -1\text{ mA}$	3.85		3.8		3.85			
$V_{CC} = 4.5\text{ V}$		$I_{OH} = -3\text{ mA}$	3.1		3		3.1			
V_{OL}	A port	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 48\text{ mA}$		0.55		0.55		V	
			$I_{OL} = 64\text{ mA}$		0.55*			0.55		
B port	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 12\text{ mA}$			0.8		0.8		0.8		
V_{hys}			100						mV	
I_I	Control inputs	$V_{CC} = 0\text{ to }5.5\text{ V}$, $V_I = V_{CC}\text{ or GND}$		± 1		± 1		± 1	μA	
	A or B ports	$V_{CC} = 2.1\text{ V to }5.5\text{ V}$, $V_I = V_{CC}\text{ or GND}$		± 20		± 20		± 20		
I_{OZPU}	$V_{CC} = 0\text{ to }2.1\text{ V}$, $V_O = 0.5\text{ V to }2.7\text{ V}$, \overline{OE} or $OE = X\text{§}$			± 50		± 50		± 50	μA	
I_{OZPD}	$V_{CC} = 2.1\text{ V to }0$, $V_O = 0.5\text{ V to }2.7\text{ V}$, \overline{OE} or $OE = X\text{§}$			± 50		± 50		± 50	μA	
I_{OZH}^\ddagger	$V_{CC} = 2.1\text{ V to }5.5\text{ V}$, $V_O = 2.7\text{ V}$, $OE \geq 2\text{ V}$ or $OE \leq 0.8\text{ V}$			10		10		10	μA	
I_{OZL}^\ddagger	$V_{CC} = 2.1\text{ V to }5.5\text{ V}$, $V_O = 0.5\text{ V}$, $OE \geq 2\text{ V}$ or $OE \leq 0.8\text{ V}$			-10		-10		-10	μA	
I_{off}	$V_{CC} = 0$, V_I or $V_O \leq 4.5\text{ V}$			± 100				± 100	μA	
I_{CEX}	Outputs high	$V_{CC} = 5.5\text{ V}$, $V_O = 5.5\text{ V}$		50		50		50	μA	
$I_{O\uparrow}$	A port	$V_{CC} = 5.5\text{ V}$, $V_O = 2.5\text{ V}$	-50	-110	-180	-50	-180	-50	-180	mA
	B port	$V_{CC} = 5.5\text{ V}$, $V_O = 2.5\text{ V}$	-25	-55	-90	-25	-90	-25	-90	
I_{CC}	A or B ports	$V_{CC} = 5.5\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high		3		3		3	mA
			Outputs low		36		36		36	
			Outputs disabled		3		3		3	
$\Delta I_{CC}^\#$		$V_{CC} = 5.5\text{ V}$, One input at 3.4 V , Other inputs at V_{CC} or GND		50		50		50	μA	
C_i	Control inputs	$V_I = 2.5\text{ V or }0.5\text{ V}$		3					pF	
C_{iO}	A or B ports	$V_O = 2.5\text{ V or }0.5\text{ V}$		9					pF	

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at $V_{CC} = 5\text{ V}$.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ For V_{CC} between 2.1 V and 4 V , OE should be less than or equal to 0.5 V to ensure a low state.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND .

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		SN54ABT162501		SN74ABT162501		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	150		150		MHz
t_w	Pulse duration	LEAB or LEBA high		3		ns
		CLKAB or CLKBA high or low		3.3		
t_{su}	Setup time	A before CLKAB \uparrow		4.3		ns
		B before CLKBA \uparrow		4.3		
		A before LEAB \downarrow or B before LEBA \downarrow	CLK high	2.5		
			CLK low	1		
t_h	Hold time	A after CLKAB \uparrow or B after CLKBA \uparrow		0		ns
		A after LEAB \downarrow or B after LEBA \downarrow		2		

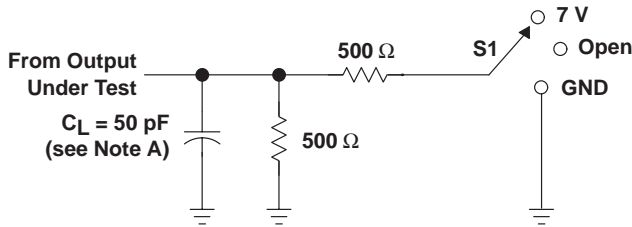
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ$ C			SN54ABT162501		SN74ABT162501		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			150	200		150		150	MHz	
t_{PLH}	A or B	B or A	1.5	2.6	4	1.5	5.1	1.5	4.8	ns
t_{PHL}			2	3.4	5.2	2	6.1	2	5.7	
t_{PLH}	LEAB or LEBA	B or A	2	3.3	4.8	2	6.1	2	5.6	ns
t_{PHL}			2	3.8	5.2	2	6.4	2	5.9	
t_{PLH}	CLKAB or CLKBA	B or A	1.5	3.5	4.7	1.5	6	1.5	5.5	ns
t_{PHL}			1.5	3.5	4.8	1.5	5.8	1.5	5.3	
t_{PZH}	OEAB or $\overline{\text{OEBA}}$	B or A	1.5	3.4	4.6	1.5	5.6	1.5	5.3	ns
t_{PZL}			2	3.8	4.7	2	5.6	2	5.4	
t_{PHZ}	OEAB or $\overline{\text{OEBA}}$	B or A	2	4.5	5.7	2	6.9	2	6.5	ns
t_{PLZ}			1.5	3.8	5.3	1.5	6.3	1.5	5.8	

SN54ABT162501, SN74ABT162501 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

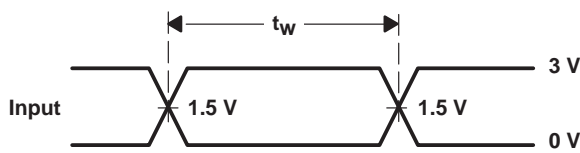
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PARAMETER MEASUREMENT INFORMATION

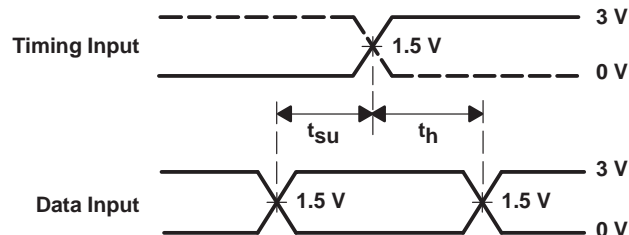


LOAD CIRCUIT

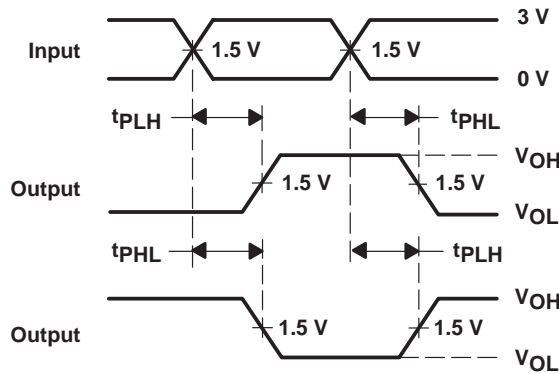
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



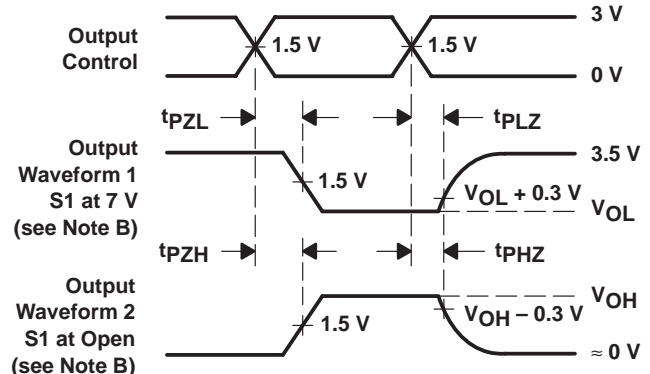
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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