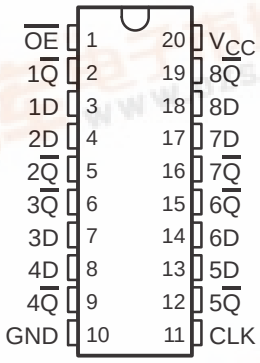
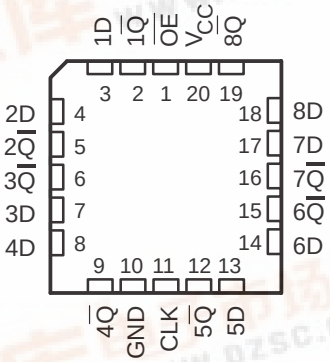
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Plastic (N) and Ceramic (J) DIPs, and Ceramic Flat (W) Package**

SN54ABT534 . . . J OR W PACKAGE
SN74ABT534A . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54ABT534 . . . FK PACKAGE
(TOP VIEW)



description

These 8-bit flip-flops with 3-state outputs are designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK), the $\overline{Q}$ outputs are set to the complement of the logic levels set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the flip-flop. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

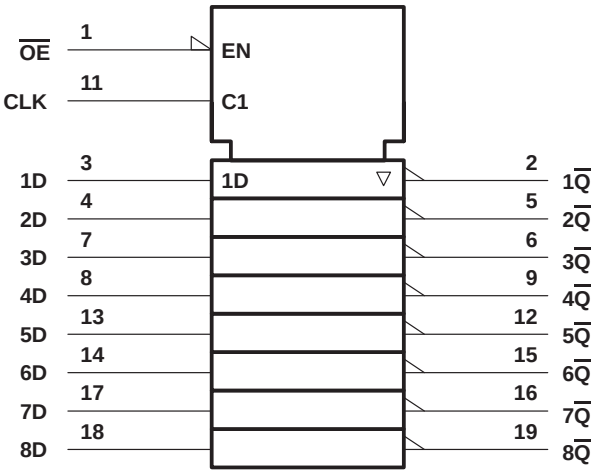
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT534 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT534A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

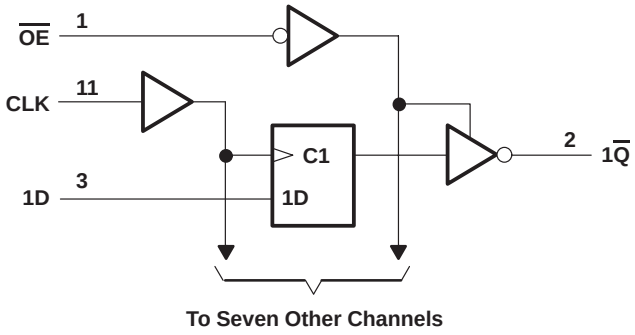
INPUTS			OUTPUT
$\overline{OE}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	H or L	X	$\overline{Q}_0$
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT534 . . . . . 96 mA
SN74ABT534A . . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package . . . . . 115°C/W
DW package . . . . . 97°C/W
N package . . . . . 67°C/W
PW package . . . . . 128°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

			SN54ABT534		SN74ABT534A		UNIT
				MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT534		SN74ABT534A		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = –3 mA		3			3		3		
	V_{CC} = 4.5 V	I_{OH} = –24 mA		2			2				
		I_{OH} = –32 mA		2*					2		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA				0.55		0.55			V
		I_{OL} = 64 mA				0.55*				0.55	
V_{hys}					100						mV
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V				10‡		10‡		10‡	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V				–10‡		–10‡		–10‡	µA
I_{off}	V_{CC} = 0,	V_I or $V_O \le$ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–100	–180‡	–50	–180‡	–50	–180‡	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND		Outputs high		1	250		250		250	µA
			Outputs low		24	30		30		30	mA
			Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V				3.5						pF
C_o	V_O = 2.5 V or 0.5 V				6.5						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at V_{CC} = 5 V.
‡ This data sheet limit may vary among suppliers.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN54ABT534			UNIT
			V_{CC} = 5 V, T_A = 25°C		MIN MAX	
			MIN	MAX		
f_{clock}	Clock frequency			125	125	MHz
t_w	Pulse duration	CLK high or low	3.5		3.5	ns
t_{su}	Setup time, data before CLK↑	High or low	1.6		1.6	ns
t_h	Hold time, data after CLK↑	High or low	1.6		1.6	ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN74ABT534A			UNIT
			V_{CC} = 5 V, T_A = 25°C		MIN MAX	
			MIN	MAX		
f_{clock}	Clock frequency			125	125	MHz
t_w	Pulse duration	CLK high or low	3.5		3.5	ns
t_{su}	Setup time, data before CLK↑	High or low	1.6		1.6	ns
t_h	Hold time, data after CLK↑	High or low	2†		2†	ns

† This data sheet limit may vary among suppliers.

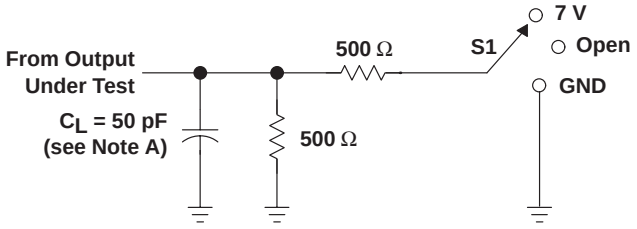
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT534					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
f_{max}			125	175		125		MHz
t_{PLH}	CLK	$\overline{Q}$	2.6	4.5	6.1	2.6	7	ns
t_{PHL}			3.4	5.5	6.7	3.4	7.9	
t_{PZH}	$\overline{OE}$	$\overline{Q}$	1	3.4	5.2	1	5.8	ns
t_{PZL}			2.6	4	5.8	2.6	7	
t_{PHZ}	$\overline{OE}$	$\overline{Q}$	2.4	4.7	6.6	2.4	7.6	ns
t_{PLZ}			2.3	3.8	5.8	2.3	6.8	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

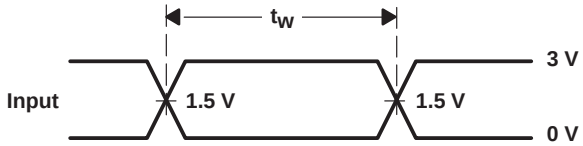
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT534A					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
f_{max}			125	175		125		MHz
t_{PLH}	CLK	$\overline{Q}$	2.6	4.5	5.9	2.6	6.7	ns
t_{PHL}			3.4	5.5	6.7	3.4	7.6	
t_{PZH}	$\overline{OE}$	$\overline{Q}$	1	3.4	4.2	1	5	ns
t_{PZL}			2.6	4	5.8	2.6	6.8	
t_{PHZ}	$\overline{OE}$	$\overline{Q}$	2.4	4.7	6.6	2.4	7.3	ns
t_{PLZ}			2.3	3.8	5.8	2.3	6.5	

PARAMETER MEASUREMENT INFORMATION

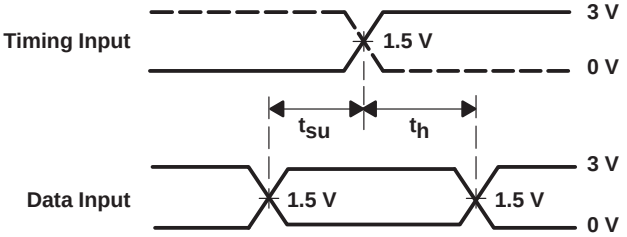


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

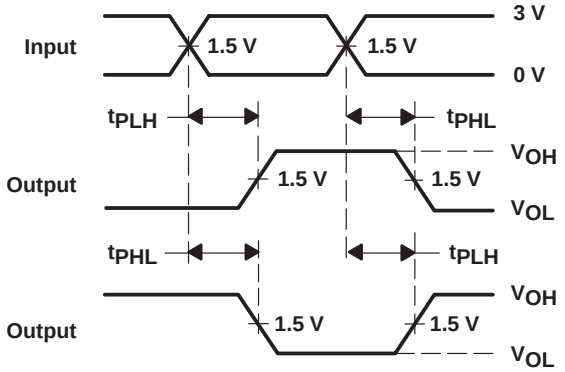
LOAD CIRCUIT



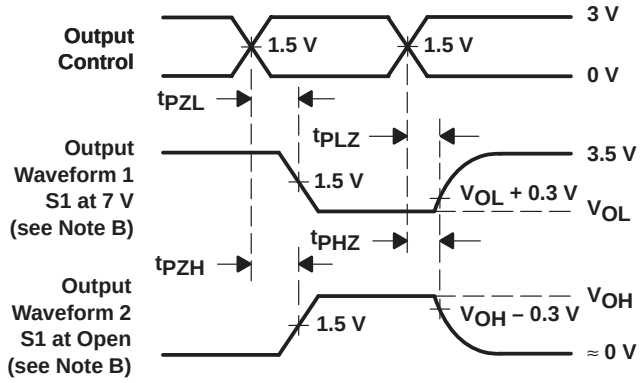
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.