

SN54LVC374A, SN74LVC374A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce)**
 $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
 $> 2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- **Power Off Disables Inputs/Outputs, Permitting Live Insertion**
- **Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200\text{ pF}$, $R = 0$)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and DIPs (J)**

description

The SN54LVC374A octal edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation and the SN74LVC374A octal edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing buffer registers, input/output (I/O) ports, bidirectional bus drivers, and working registers.

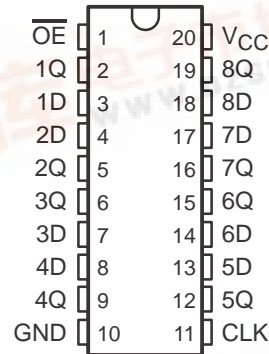
On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

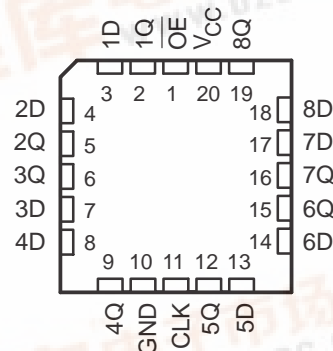
\overline{OE} does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

SN54LVC374A . . . J OR W PACKAGE
SN74LVC374A . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVC374A . . . FK PACKAGE
(TOP VIEW)



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description (continued)

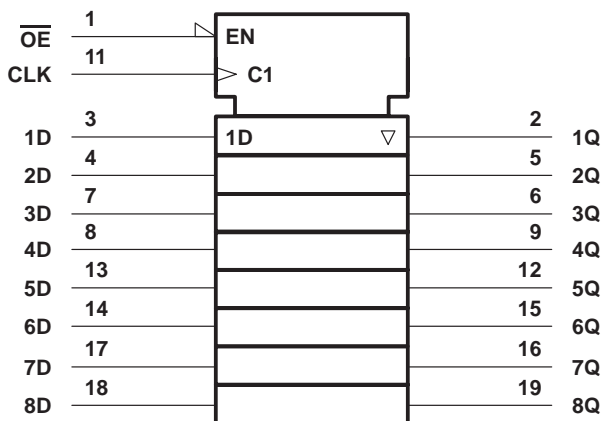
resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVC374A is characterized for operation over the full military temperature range of -55°C to 125°C .

(each flip-flop)

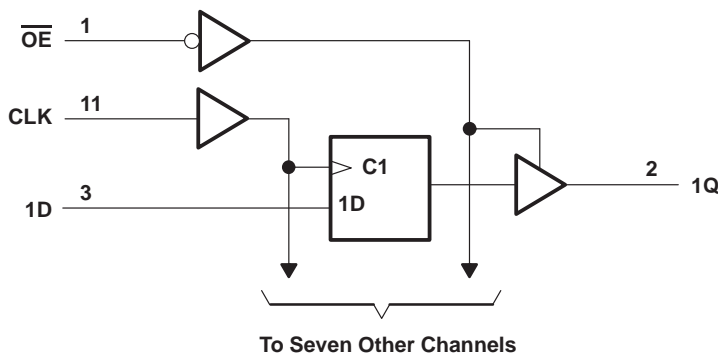
INPUTS			OUTPUT Q
\overline{OE}	CLK	D	
L	\uparrow	H	H
L	\uparrow	L	L
L	H or L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LVC374A		SN74LVC374A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	Operating	2	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V_{IH}	High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V			$0.65 \times V_{CC}$		V
		$V_{CC} = 2.3$ V to 2.7 V			1.7		
		$V_{CC} = 2.7$ V to 3.6 V	2		2		
V_{IL}	Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V			$0.35 \times V_{CC}$		V
		$V_{CC} = 2.3$ V to 2.7 V			0.7		
		$V_{CC} = 2.7$ V to 3.6 V		0.8	0.8		
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	0	V_{CC}	V
		3 state	0	5.5	0	5.5	
I_{OH}	High-level output current	$V_{CC} = 1.65$ V			–4		mA
		$V_{CC} = 2.3$ V			–8		
		$V_{CC} = 2.7$ V		–12	–12		
		$V_{CC} = 3$ V		–24	–24		
I_{OL}	Low-level output current	$V_{CC} = 1.65$ V			4		mA
		$V_{CC} = 2.3$ V			8		
		$V_{CC} = 2.7$ V		12	12		
		$V_{CC} = 3$ V		24	24		
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	0	10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	SN54LVC374A			SN74LVC374A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{OH}	I _{OH} = –100 μA		1.65 V to 3.6 V				V _{CC} –0.2			V
			2.7 V to 3.6 V	V _{CC} –0.2						
	I _{OH} = –4 mA		1.65 V				1.2			
	I _{OH} = –8 mA		2.3 V				1.7			
	I _{OH} = –12 mA		2.7 V	2.2			2.2			
			3 V	2.4			2.4			
	I _{OH} = –24 mA		3 V	2.2			2.2			
V _{OL}	I _{OL} = 100 μA		1.65 V to 3.6 V				0.2			V
			2.7 V to 3.6 V	0.2						
	I _{OL} = 4 mA		1.65 V				0.45			
	I _{OL} = 8 mA		2.3 V				0.7			
	I _{OL} = 12 mA		2.7 V	0.4			0.4			
	I _{OL} = 24 mA		3 V	0.55			0.55			
I _I	V _I = 0 to 5.5 V		3.6 V	±5			±5			μA
I _{off}	V _I or V _O = 5.5 V		0				±10			μA
I _{OZ}	V _O = 0 to 5.5 V		3.6 V	±15			±10			μA
I _{CC}	V _I = V _{CC} or GND	I _O = 0	3.6 V	10			10			μA
	3.6 V ≤ V _I ≤ 5.5 V‡			10			10			
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND		2.7 V to 3.6 V	500			500			μA
C _i	V _I = V _{CC} or GND		3.3 V	4 12			4			pF
C _o	V _O = V _{CC} or GND		3.3 V	5.5 12			5.5			pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ This applies in the disabled state only.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

		SN54LVC374A				UNIT
		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
		MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	80		100		MHz
t _w	Pulse duration, CLK high or low	3.3		3.3		ns
t _{su}	Setup time, data before CLK↑	2		2		ns
t _h	Hold time, data after CLK↑	1.5		1.5		ns

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		SN74LVC374A								UNIT
		$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	†		†		80		100		MHz
t _w	Pulse duration, CLK high or low	†		†		3.3		3.3		ns
t _{su}	Setup time, data before CLK↑	†		†		2		2		ns
t _h	Hold time, data after CLK↑	†		†		1.5		1.5		ns

† This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC374A				UNIT
			V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
f _{max}			80		100		MHz
t _{pd}	CLK	Q	9.5		1	8.5	ns
t _{en}	$\overline{\text{OE}}$	Q	9.5		1	8.5	ns
t _{dis}	$\overline{\text{OE}}$	Q	8		1	7	ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC374A								UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		†		80		100		MHz
t _{pd}	CLK	Q	†	†	†	†	8.1		1.5	7	ns
t _{en}	$\overline{\text{OE}}$	Q	†	†	†	†	8.5		1.5	7.5	ns
t _{dis}	$\overline{\text{OE}}$	Q	†	†	†	†	7.1		1.5	6.5	ns
t _{sk(o)} [†]										1	ns

† This information was not available at the time of publication.

‡ Skew between any two outputs of the same package switching in the same direction

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	$f = 10\text{ MHz}$	†	†	54.5	pF
		Outputs disabled		†	†	13.5	

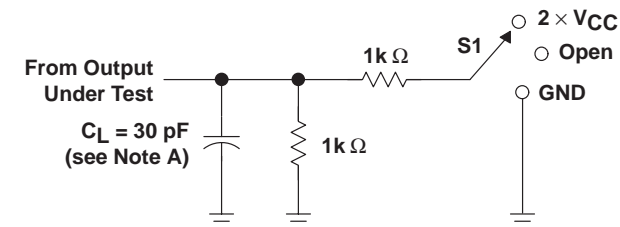
† This information was not available at the time of publication.

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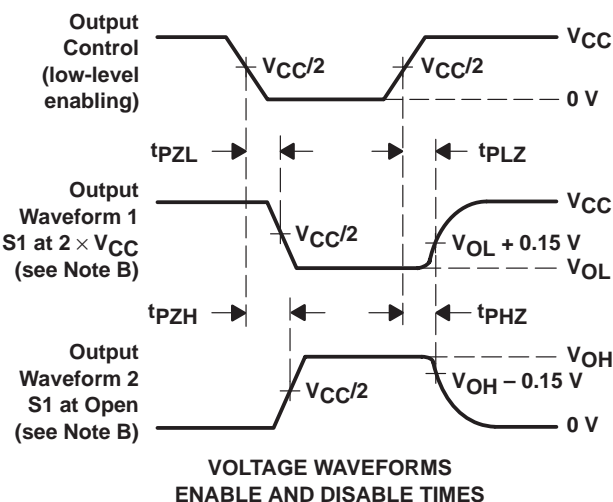
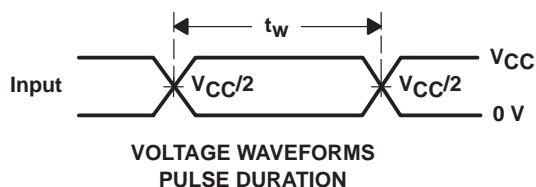
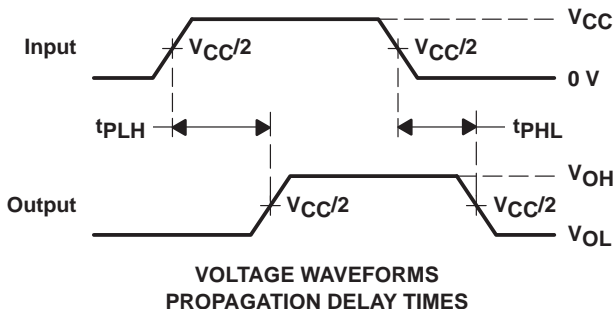
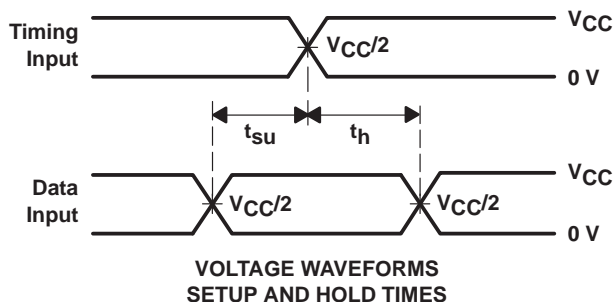
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	Open



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

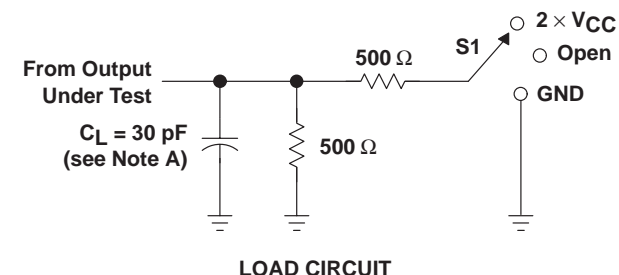
Figure 1. Load Circuit and Voltage Waveforms

SN54LVC374A, SN74LVC374A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

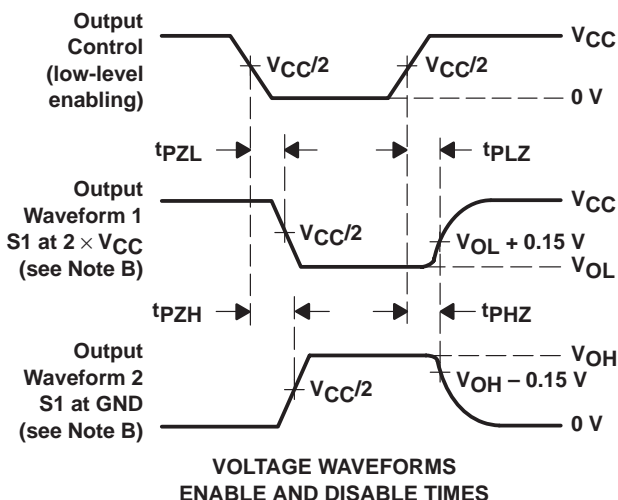
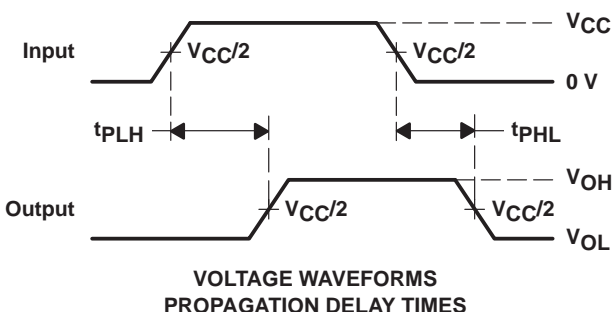
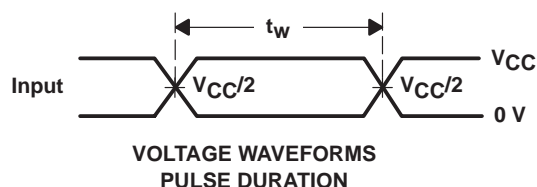
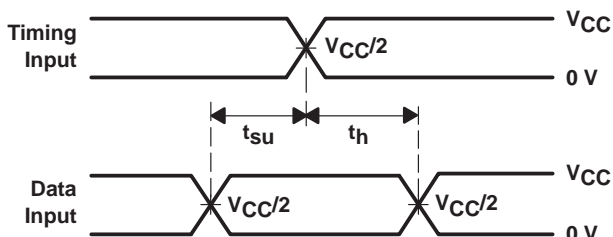
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PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PHZ}	GND



- NOTES:
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 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

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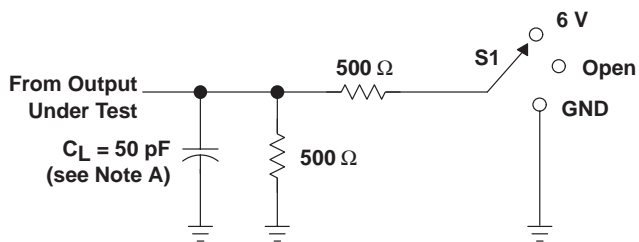
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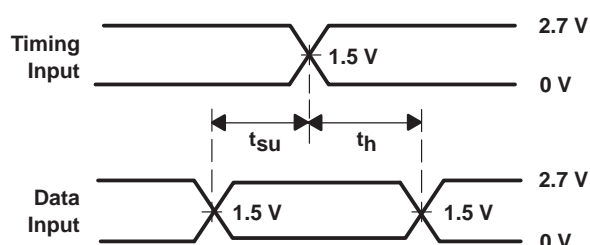
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V} \pm 0.3 \text{ V}$

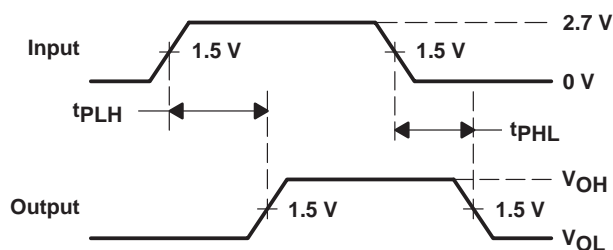


LOAD CIRCUIT

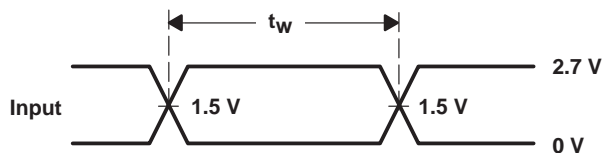
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



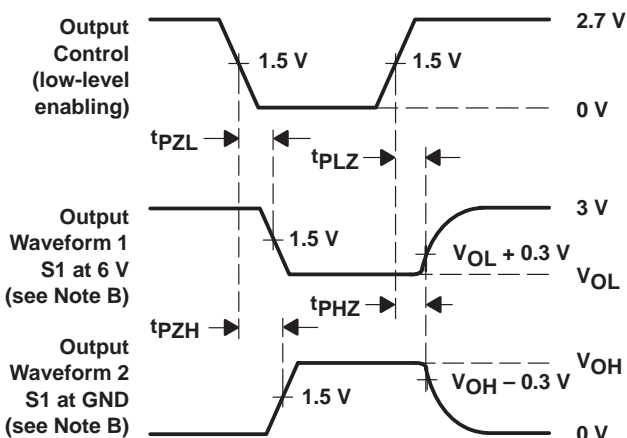
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

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