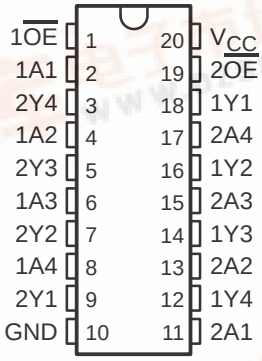
SN54LVCH244A, SN74LVCH244A
OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

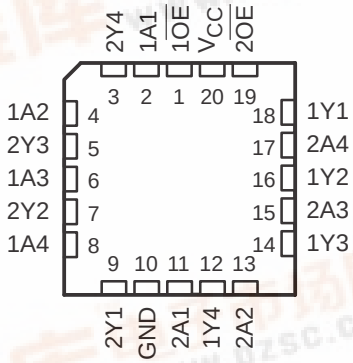
SCES009G – JULY 1995 - REVISED JUNE 1998

- *EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Power Off Disables Outputs, Permitting Live Insertion
- Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Package, Ceramic Chip Carriers (FK), and DIPs (J)

SN54LVCH244A . . . J OR W PACKAGE
SN74LVCH244A . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVCH244A . . . FK PACKAGE
(TOP VIEW)



description

The SN54LVCH244A octal buffer/line driver is designed for 2.7-V to 3.6-V V_{CC} operation and the SN74LVCH244A octal buffer/line driver is designed for 1.65-V to 3.6-V V_{CC} operation.

These devices are organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, these devices pass data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

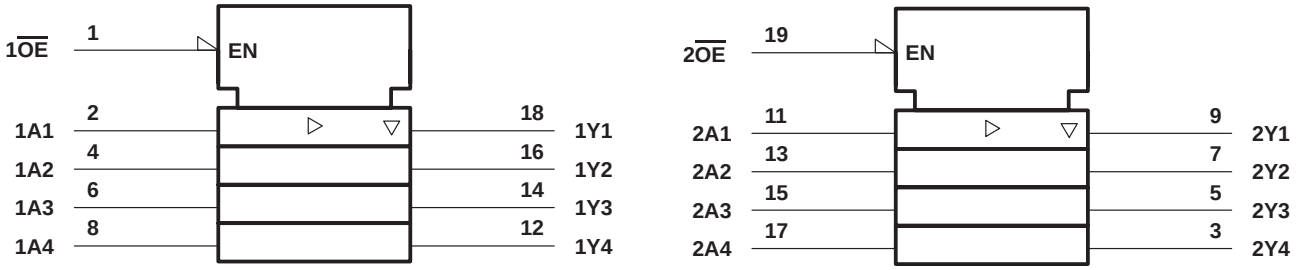
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVCH244A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVCH244A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

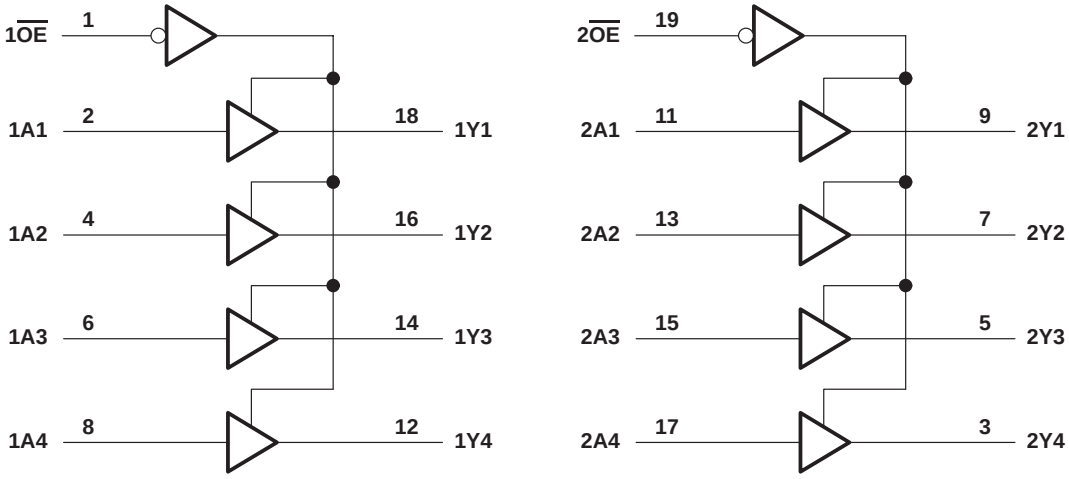
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 6.5 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) . . . . . –0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Continuous output current, I_O . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package . . . . . 115°C/W
DW package . . . . . 97°C/W
PW package . . . . . 128°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LVCH244A		SN74LVCH244A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	Operating	2	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V			0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V			1.7		
		V_{CC} = 2.7 V to 3.6 V	2		2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V				0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V				0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8		0.8	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	0	V_{CC}	V
		3 state	0	5.5	0	5.5	
I_{OH}	High-level output current	V_{CC} = 1.65 V				–4	mA
		V_{CC} = 2.3 V				–8	
		V_{CC} = 2.7 V		–12		–12	
		V_{CC} = 3 V		–24		–24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V				4	mA
		V_{CC} = 2.3 V				8	
		V_{CC} = 2.7 V		12		12	
		V_{CC} = 3 V		24		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	0	10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	SN54LVCH244A			SN74LVCH244A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	I_{OH} = –100 µA		1.65 V to 3.6 V				V_{CC}–0.2			V
			2.7 V to 3.6 V	V_{CC}–0.2						
	I_{OH} = –4 mA		1.65 V				1.2			
	I_{OH} = –8 mA		2.3 V				1.7			
	I_{OH} = –12 mA		2.7 V	2.2			2.2			
			3 V	2.4			2.4			
	I_{OH} = –24 mA		3 V	2.2			2.2			
V_{OL}	I_{OL} = 100 µA		1.65 V to 3.6 V						0.2	V
			2.7 V to 3.6 V			0.2				
	I_{OL} = 4 mA		1.65 V						0.45	
	I_{OL} = 8 mA		2.3 V						0.7	
	I_{OL} = 12 mA		2.7 V			0.4			0.4	
	I_{OL} = 24 mA		3 V			0.55			0.55	
I_I	V_I = 0 to 5.5 V		3.6 V			±5			±5	µA
I_{off}	V_I or V_O = 5.5 V		0						±10	µA
$I_{I(hold)}$	V_I = 0.58 V		1.65 V				‡			µA
	V_I = 1.07 V						‡			
	V_I = 0.7 V		2.3 V				45			
	V_I = 1.7 V						–45			
$I_{I(hold)}$	V_I = 0.8 V		3 V	75			75			µA
	V_I = 2 V			–75			–75			
	V_I = 0 to 3.6 V§		3..6 V			±500			±500	
I_{OZ}	V_O = 0 to 5.5 V		3.6 V			±15			±10	µA
I_{CC}	V_I = V_{CC} or GND	I_O = 0	3.6 V			10			10	µA
	3.6 V ≤ V_I ≤ 5.5 V¶					10			10	
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		2.7 V to 3.6 V			500			500	µA
C_i	V_I = V_{CC} or GND		3.3 V		4	12		4		pF
C_o	V_O = V_{CC} or GND		3.3 V		5.5	12		5.5		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This information was not available at the time of publication.
§ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
¶ This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVCH244A				UNIT
			V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t_{pd}	A	Y		7.5	1	6.5	ns
t_{en}	$\overline{OE}$	Y		9	1	8	ns
t_{dis}	$\overline{OE}$	Y		8	1	7	ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVCH244A						UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V	V_{CC} = 3.3 V ± 0.3 V	
			MIN	MAX	MIN	MAX	MIN MAX	MIN MAX	
t_{pd}	A	Y	†	†	†	†	6.9	1.5 5.9	ns
t_{en}	$\overline{OE}$	Y	†	†	†	†	8.6	1 7.6	ns
t_{dis}	$\overline{OE}$	Y	†	†	†	†	6.8	1.5 5.8	ns

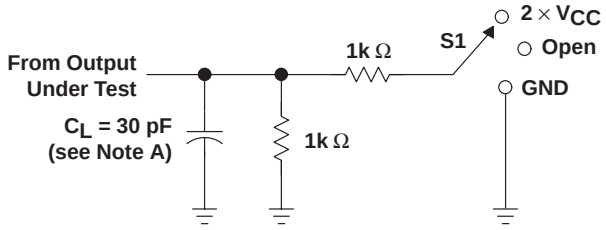
† This information was not available at the time of publication.

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10 MHz	†	†	47	pF
		Outputs disabled		†	†	2	

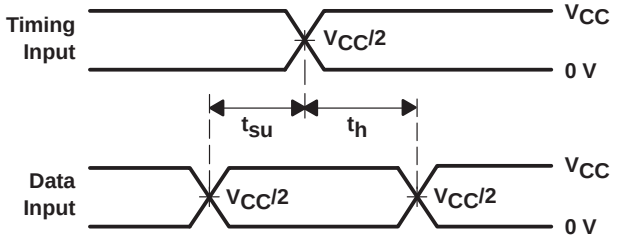
† This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 1.8 V ± 0.15 V

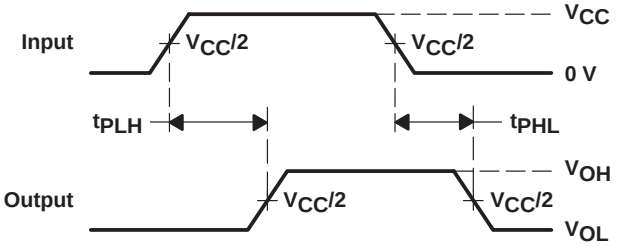


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	Open

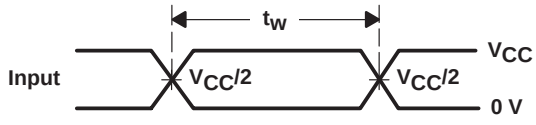
LOAD CIRCUIT



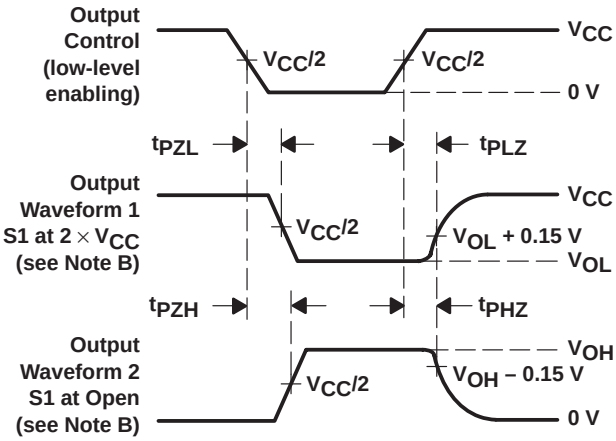
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION

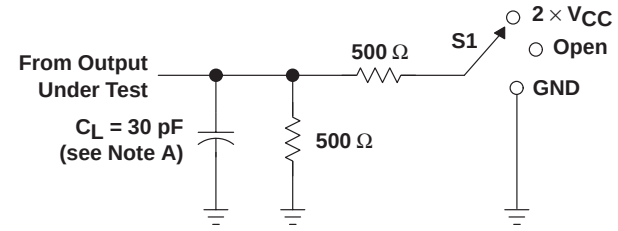


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤10 MHz, Z_O = 50 Ω, t_r≤2 ns, t_f≤2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

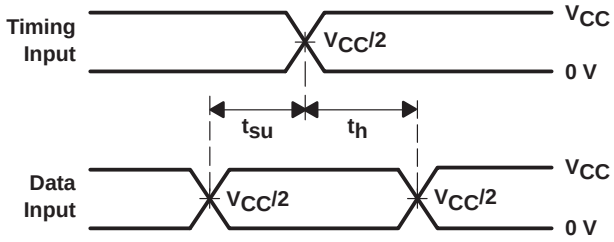
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

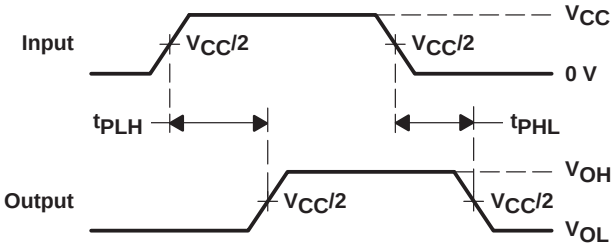


TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 × V_{CC} GND

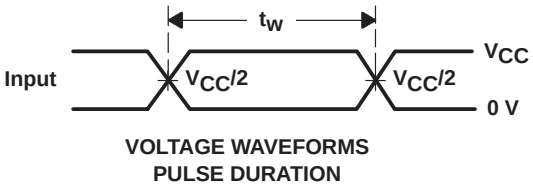
LOAD CIRCUIT



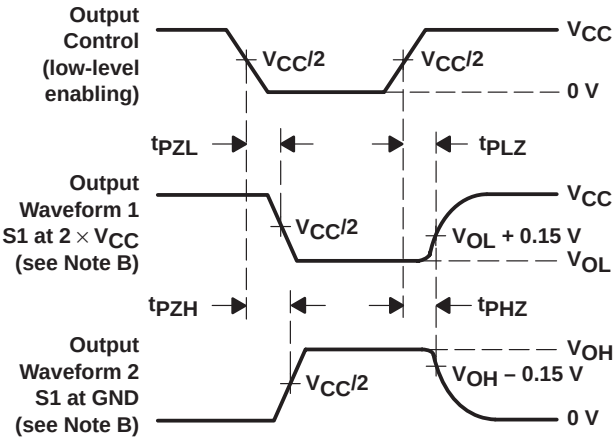
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION

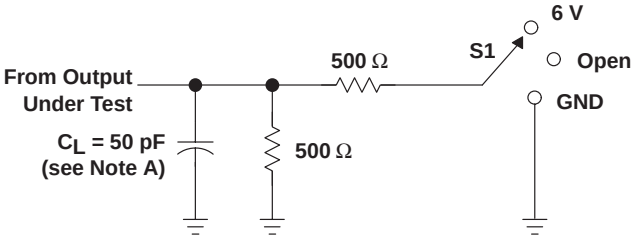


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤10 MHz, Z_O = 50 Ω, t_r≤2 ns, t_f≤2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

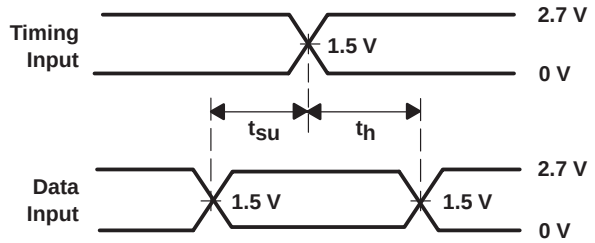
Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7 V AND 3.3 V ± 0.3 V

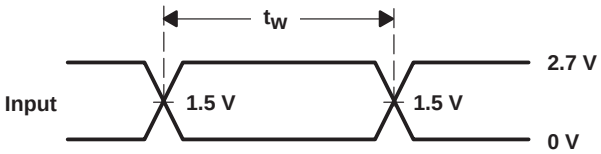


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

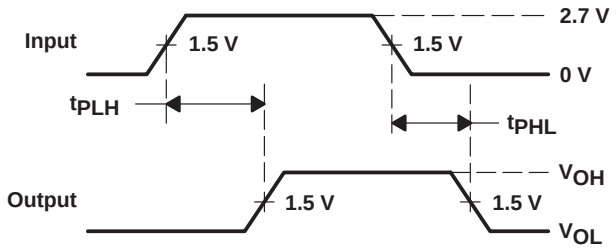
LOAD CIRCUIT



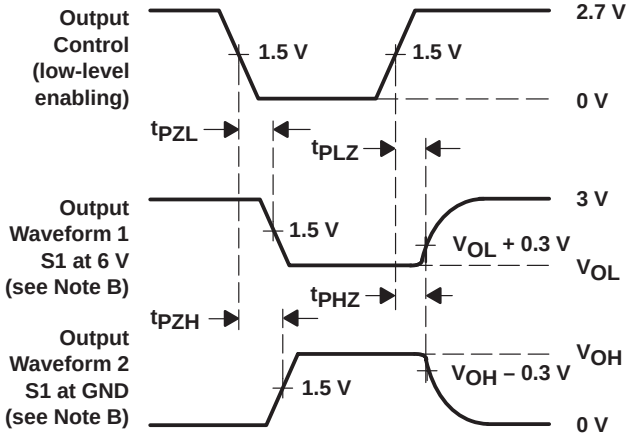
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 3. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.