National **S**emiconductor

54F/74F646 • 74F646B • 54F/74F648
Octal Transceiver/Register with TRI-STATE® Outputs

General Description

These devices consist of bus transceiver circuits with TRI-STATE, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Control $\overline{G}$ and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control $\overline{G}$ is Active LOW. In the isolation mode (control $\overline{G}$ HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

Features

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- 'F648 has inverting data paths
- 'F646/'F646B have non-inverting data paths
- 'F646B is a faster version of the 'F646
- TRI-STATE outputs
- 300 mil slim DIP
- Guaranteed 4000V minimum ESD protection

| Commercial	Military	Package Number	Package Description
74F646SPC		N24C	24-Lead (0.300″ Wide) Molded Dual-In-Line
	54F646DM (Note 2)	J24F	24-Lead (0.300″ Wide) Ceramic Dual-In-Line
74F646SC (Note 1)		M24B	24-Lead (0.300″ Wide) Molded Small Outline, JEDEC
74F646MSA (Note 1)		MSA24	24-Lead Molded Shrink Small Outline, EIAJ, Type II
	54F646FM (Note 2)	W24C	24-Lead Cerpack
	54F646LM (Note 2)	E28A	28-Lead Ceramic Leadless Chip Carrier, Type C
74F646BSPC		N24C	24-Lead (0.300″ Wide) Molded Dual-In-Line
74F646BSC (Note 1)		M24B	24-Lead (0.300″ Wide) Molded Small Outline, JEDEC
74F648SPC		N24C	24-Lead (0.300″ Wide) Molded Dual-In-Line
	54F648SDM (Note 2)	J24F	24-Lead (0.300″ Wide) Ceramic Dual-In-Line
74F648SC (Note 1)		M24B	24-Lead (0.300″ Wide) Molded Small Outline, JEDEC
	54F648FM (Note 2)	W24C	24-Lead Cerpack
	54F648LM (Note 2)	E28A	24-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13″ reel. Use suffix = SCX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.
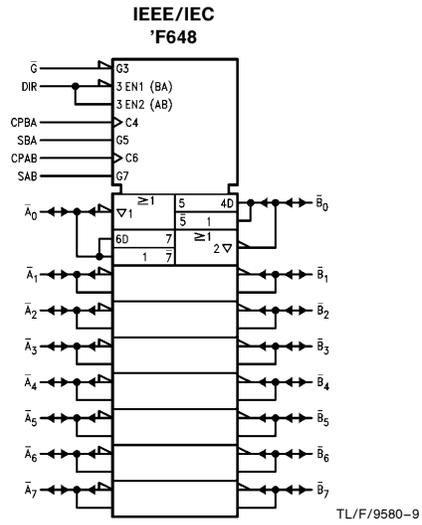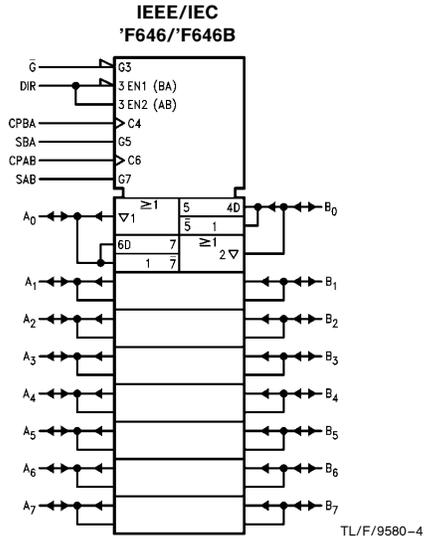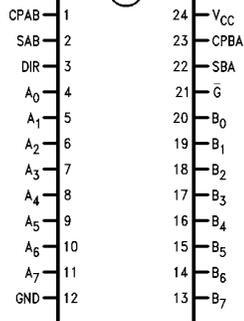
Logic Symbols
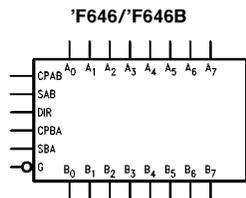
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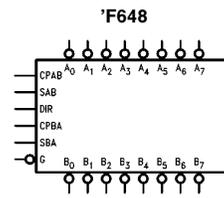
TL/F/9580–1

'F648

TL/F/9580–7

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Logic Symbols (Continued)

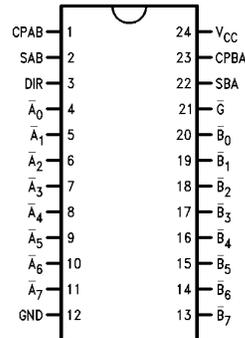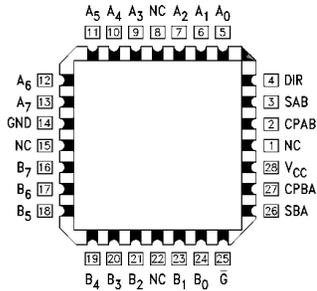### IEEE/IEC 'F646/'F646B

TL/F/9580–4

IEEE/IEC 'F648

TL/F/9580–9

Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak 'F646/'F646B

CPAB	1	24	V_{CC}
SAB	2	23	CPBA
DIR	3	22	SBA
A_0	4	21	$\overline{G}$
A_1	5	20	B_0
A_2	6	19	B_1
A_3	7	18	B_2
A_4	8	17	B_3
A_5	9	16	B_4
A_6	10	15	B_5
A_7	11	14	B_6
GND	12	13	B_7

TL/F/9580–2

Pin Assignment for DIP, SOIC and Flatpak 'F648

CPAB	1	24	V_{CC}
SAB	2	23	CPBA
DIR	3	22	SBA
$\overline{A}_0$	4	21	$\overline{G}$
$\overline{A}_1$	5	20	$\overline{B}_0$
$\overline{A}_2$	6	19	$\overline{B}_1$
$\overline{A}_3$	7	18	$\overline{B}_2$
$\overline{A}_4$	8	17	$\overline{B}_3$
$\overline{A}_5$	9	16	$\overline{B}_4$
$\overline{A}_6$	10	15	$\overline{B}_5$
$\overline{A}_7$	11	14	$\overline{B}_6$
GND	12	13	$\overline{B}_7$

TL/F/9580–8

Pin Assignment for LCC 'F646/'F646B

TL/F/9580–3

Pin Assignment for LCC 'F648

TL/F/9580–10

2
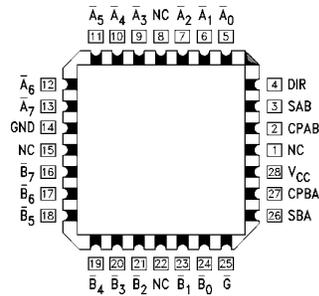
Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_0-A_7	Data Register A Inputs/	3.5/1.083	70 μA/$-$650 μA
	TRI-STATE Outputs	600/106.6 (80)	$-$12 mA/64 mA (48 mA)
B_0-B_7	Data Register B Inputs/	3.5/1.083	70 μA/$-$650 μA
	TRI-STATE Outputs	600/106.6 (80)	$-$12 mA/64 mA (48 mA)
CPAB, CPBA	Clock Pulse Inputs	1.0/1.0	20 μA/$-$0.6 mA
SAB, SBA	Select Inputs	1.0/1.0	20 μA/$-$0.6 mA
$\overline{G}$	Output Enable Input	1.0/1.0	20 μA/$-$0.6 mA
DIR	Direction Control Input	1.0/1.0	20 μA/$-$0.6 mA

Function Table

Inputs						Data I/O*		Function
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_0-A_7	B_0-B_7	
H	X	H or L	H or L	X	X			Isolation
H	X	⟋	X	X	X	Input	Input	Clock A_n Data into A Register
H	X	X	⟋	X	X			Clock B_n Data into B Register
L	H	X	X	L	X			A_n to B_n—Real Time (Transparent Mode)
L	H	⟋	X	L	X			Clock A_n Data into A Register
L	H	H or L	X	H	X	Input	Output	A Register to B_n (Stored Mode)
L	H	⟋	X	H	X			Clock A_n Data into A Register and Output to B_n
L	L	X	X	X	L			B_n to A_n—Real Time (Transparent Mode)
L	L	X	⟋	X	L			Clock B_n Data into B Register
L	L	X	H or L	X	H	Output	Input	B Register to A_n (Stored Mode)
L	L	X	⟋	X	H			Clock B_n Data into B Register and Output to A_n

*The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR Inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Irrelevant
⟋ = LOW-to-HIGH Transition

Logic Diagrams (Continued)
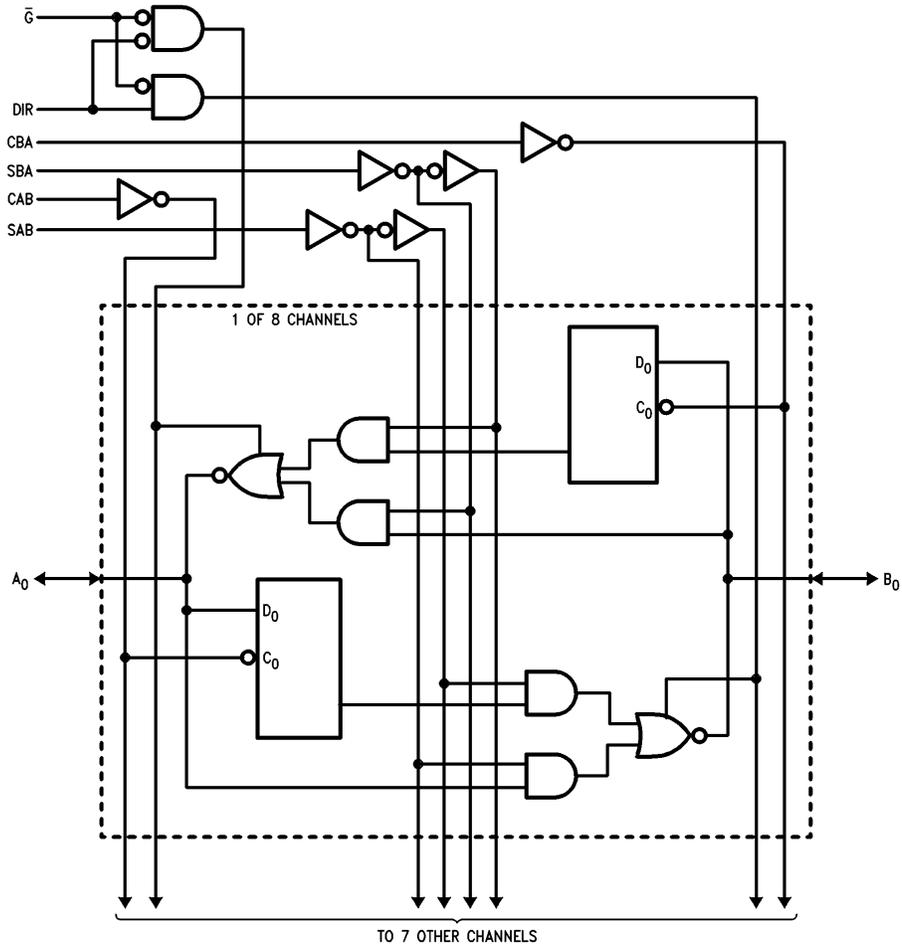
'F646/'F646B
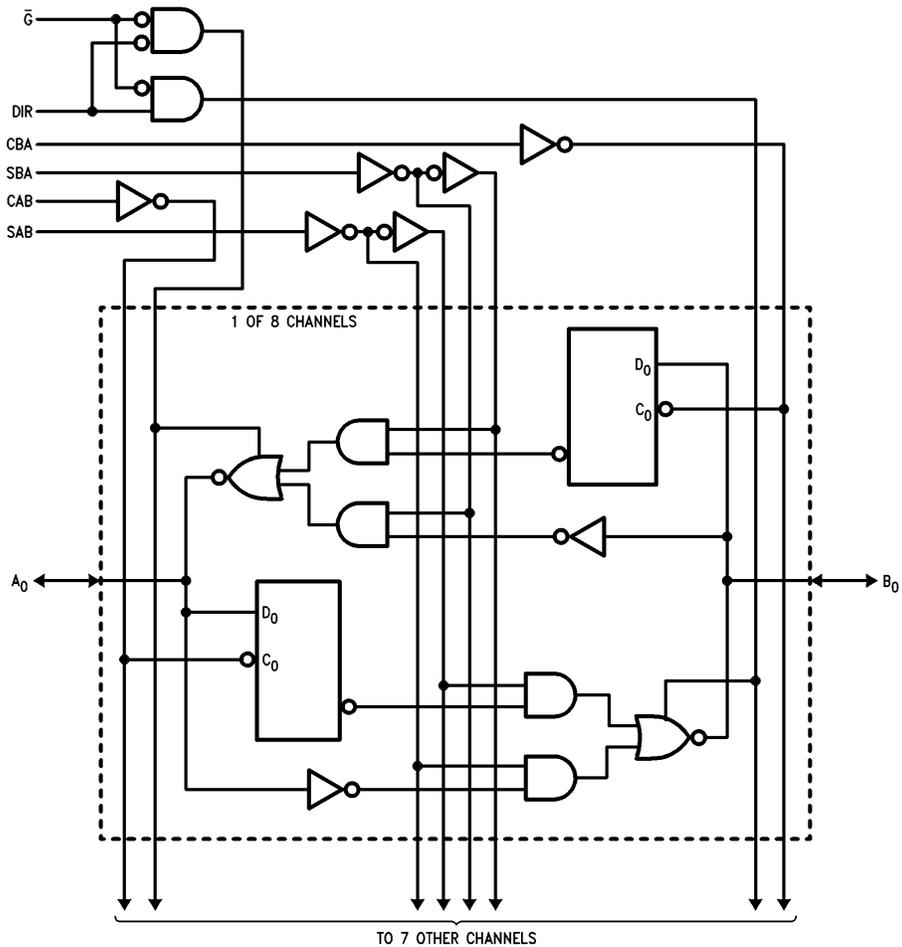
TL/F/9580–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Logic Diagrams (Continued)

'F648

TL/F/9580–6

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V_{CC}	Conditions
			Min	Typ	Max			
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.0			V	Min	I_{OH} = −12 mA (A_n, B_n)
		74F 10% V_{CC}	2.0					I_{OH} = −15 mA (A_n, B_n)
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.55	V	Min	I_{OL} = 48 mA (A_n, B_n)
		74F 10% V_{CC}			0.55			I_{OL} = 64 mA (A_n, B_n)
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	V_{IN} = 2.7V (Non I/O Pins)
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	V_{IN} = 7.0V (Non I/O Pins)
		74F			7.0			
I_{BVIT}	Input HIGH Current Breakdown (I/O)	54F			1.0	mA	Max	V_{IN} = 5.5V (A_n, B_n)
		74F			0.5			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	V_{OUT} = V_{CC}
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (Non I/O Pins)
I_{IH} + I_{OZH}	Output Leakage Current				70	μA	Max	V_{OUT} = 2.7V (A_n, B_n)
I_{IL} + I_{OZL}	Output Leakage Current				−650	μA	Max	V_{OUT} = 0.5V (A_n, B_n)
I_{OS}	Output Short-Circuit Current		−100		−225	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test				500	μA	0.0V	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current				135	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current				150	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current				150	mA	Max	V_O = HIGH Z

'F646/'F648

AC Electrical Characteristics

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		54F $T_A, V_{CC} = $ Mil $C_L = 50$ pF		74F $T_A, V_{CC} = $ Com $C_L = 50$ pF		Units
		Min	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	90		75		90		MHz
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	2.0 2.0	7.0 8.0	2.0 2.0	8.5 9.5	2.0 2.0	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus ('F646)	1.0 1.0	7.0 6.5	1.0 1.0	8.0 8.0	1.0 1.0	7.5 7.0	ns
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus ('F648)	2.0 1.0	8.5 7.5	1.0 1.0	10.0 9.0	2.0 1.0	9.0 8.0	ns
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B	2.0 2.0	8.5 8.0	2.0 2.0	11.0 10.0	2.0 2.0	9.5 9.0	ns
t_{PZH} t_{PZL}	Enable Time $\overline{OE}$ to A or B	2.0 2.0	8.5 12.0	2.0 2.0	10.0 13.5	2.0 2.0	9.0 12.5	ns
t_{PHZ} t_{PLZ}	Disable Time $\overline{OE}$ to A or B	1.0 2.0	7.5 9.0	1.0 2.0	9.0 11.0	1.0 2.0	8.5 9.5	ns
t_{PZH} t_{PZL}	Enable Time DIR to A or B	2.0 2.0	14.0 13.0	2.0 2.0	16.0 15.0	2.0 2.0	15.0 14.0	ns
t_{PHZ} t_{PLZ}	Disable Time DIR to A or B	1.0 2.0	9.0 11.0	1.0 2.0	10.0 12.0	1.0 2.0	9.5 11.5	ns

'F646/'F648

AC Operating Requirements

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$		54F $T_A, V_{CC} = $ Mil		74F $T_A, V_{CC} = $ Com		Units
		Min	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW Bus to Clock	5.0 5.0		5.0 5.0		5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW Bus to Clock	2.0 2.0		2.5 2.5		2.0 2.0		ns
$t_w(H)$ $t_w(L)$	Clock Pulse Width HIGH or LOW	5.0 5.0		5.0 5.0		5.0 5.0		ns

'F646B

AC Electrical Characteristics

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		54F $T_A, V_{CC} =$ Mil $C_L = 50$ pF		74F $T_A, V_{CC} =$ Com $C_L = 50$ pF		Units
		Min	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	165				150		MHz
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	2.5 3.0	7.0 7.5			2.5 3.0	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	2.0 2.0	6.0 6.0			2.0 2.0	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B	2.5 2.5	7.5 7.5			2.5 2.5	8.5 8.5	ns
t_{PZH} t_{PZL}	Enable Time $\overline{OE}$ to A or B	2.5 2.5	6.5 9.0			2.5 2.5	8.0 10.0	ns
t_{PHZ} t_{PLZ}	Disable Time $\overline{OE}$ to A or B	1.5 2.0	6.5 7.0			1.5 2.0	7.5 8.5	ns
t_{PZH} t_{PZL}	Enable Time DIR to A or B	2.0 3.0	7.0 9.5			2.0 3.0	8.5 10.0	ns
t_{PHZ} t_{PLZ}	Disable Time DIR to A or B	1.5 2.5	7.5 8.5			1.5 2.5	8.5 9.5	ns

'F646B

AC Operating Requirements

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$		54F $T_A, V_{CC} =$ Mil		74F $T_A, V_{CC} =$ Com		Units
		Min	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW Bus to Clock	5.0 5.0				4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW Bus to Clock	1.5 1.5				1.5 1.5		ns
$t_w(H)$ $t_w(L)$	Clock Pulse Width HIGH or LOW	5.0 5.0				5.0 5.0		ns

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

<div style="text-align:center">74F   646/646B/648   S   C   X</div>

Temperature Range Family
  74F = Commercial
  54F = Military

Device Type

Package Code
  SP = Slim Plastic DIP
  SD = Slim Ceramic DIP
  S = Small Outline (SOIC)
  MSA = Shrink Small Outline SOIC EIAJ Type II (M646 only)
  L = Leadless Chip Carrier
  F = Flatpak

Special Variations
  QB = Military grade device with environmental and burn-in processing
  X = Devices shipped in 13″ reel

Temperature Range
  C = Commercial (0°C to +70°C)
  M = Military (−55°C to +125°C)

Physical Dimensions inches (millimeters)

0.015 MIN TYP — PIN #1 INDEX

0.300±0.005 TYP

45° x 0.015±0.010

□0.450 ± 0.008

0.075
0.063

0.093
0.077

R 0.011 / 0.007 TYP

0.003 MIN TYP

0.015 MAX TYP

0.028
0.022 TYP

0.022 MAX TYP
0.006 MIN TYP

0.055
0.045 TYP

0.055
0.045 TYP

45° x 0.040±0.010
3 PLCS

0.083
0.067 TYP

DETAIL A   DETAIL A

26   4   25   5   19   11   18   12

TOP VIEW   BOTTOM VIEW   SIDE VIEW   E28A (REV D)

28-Lead Ceramic Leadless Chip Carrier, Type C
NS Package Number E28A

0.025 / (0.635) RAD

1.290 / (32.77) MAX

0.315 MAX (8.001) GLASS

0.295 / (7.493) MAX

24 23 22 21 20 19 18 17 16 15 14 13

1 2 3 4 5 6 7 8 9 10 11 12

0.030–0.055
(0.762–1.397)
RAD TYP

GLASS
SEALANT

0.060 ±0.005
(1.524 ±0.127) TYP

0.020–0.070
(0.508–1.778)

0.290–0.320
(7.366–8.128)

0.180
(4.572)
MAX

0.225
(5.715)
MAX

86° 94°
TYP

0.095 MAX
(2.413) BOTH
ENDS

0.100 ±0.010
(2.54 ±0.254)
TYP

0.018 ±0.003
(0.457 ±0.076)
TYP

0.125
(3.175)
MIN

95° ±5°

0.008–0.012
(0.203–0.305)
TYP

0.310–0.410
(7.874–10.41)

J24F(REV G)

24-Lead (0.300″ Wide) Ceramic Dual-In-Line Package (SD)
NS Package Number J24F

Physical Dimensions inches (millimeters) (Continued)

24-Lead (0.300″ Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M24B

Physical Dimensions inches (millimeters) (Continued)
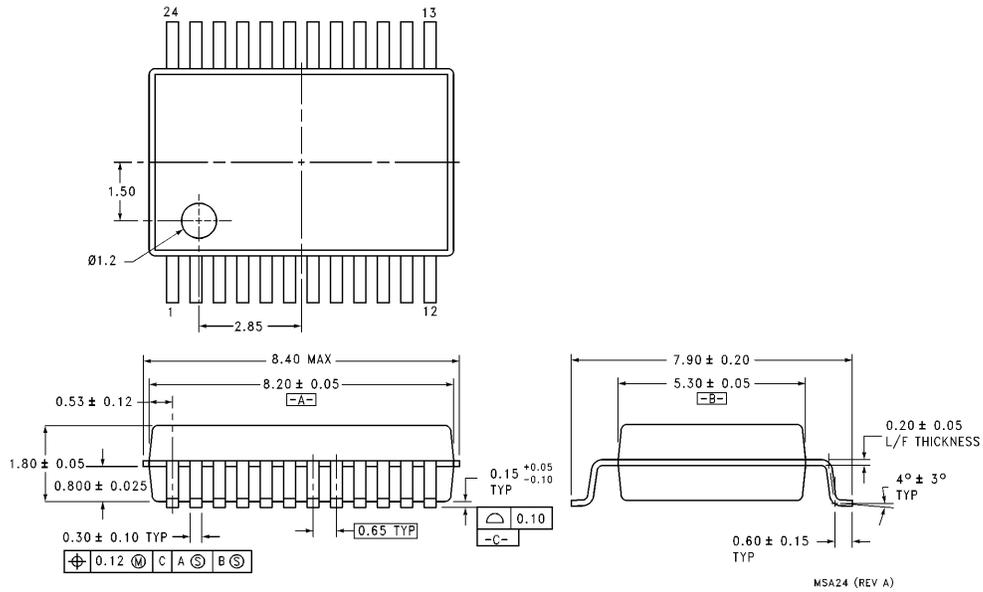
24-Lead Molded Shrink Small Outline Package, EIAJ, Type II
NS Package Number MSA24

MSA24 (REV A)
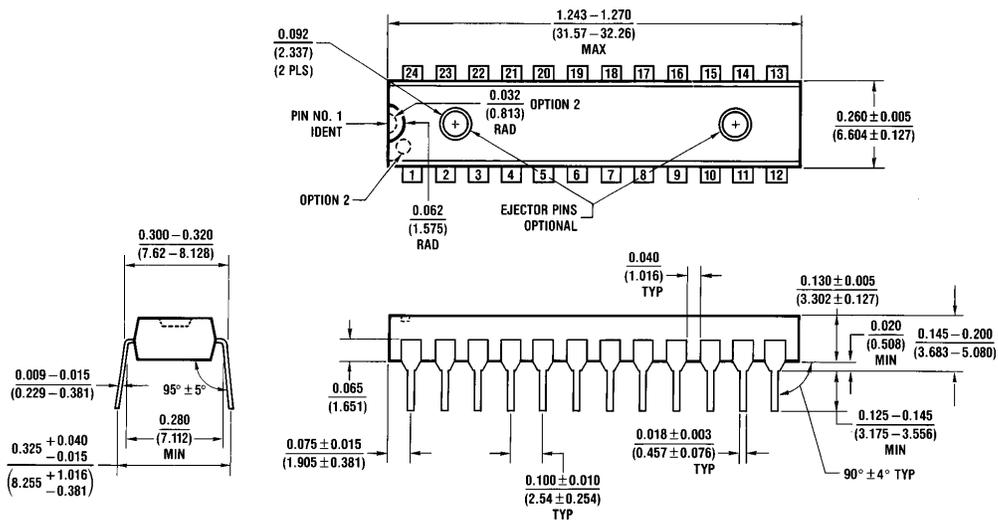
24-Lead (0.300″ Wide) Molded Dual-In-Line Package (SP)
NS Package Number N24C

N24C (REV F)

Physical Dimensions inches (millimeters) (Continued)

0.090
0.060

0.040
0.030

0.625
0.590

0.050 ± 0.005

0.005 MIN TYP

24

13

0.370
0.250

0.015
0.008

0.019
0.015 TYP

0.420 MAX

0.015
0.008

0.370
0.250

SEE
DETAIL A

1

12

0.006
0.004

0.045 MAX

W24C (REV E)
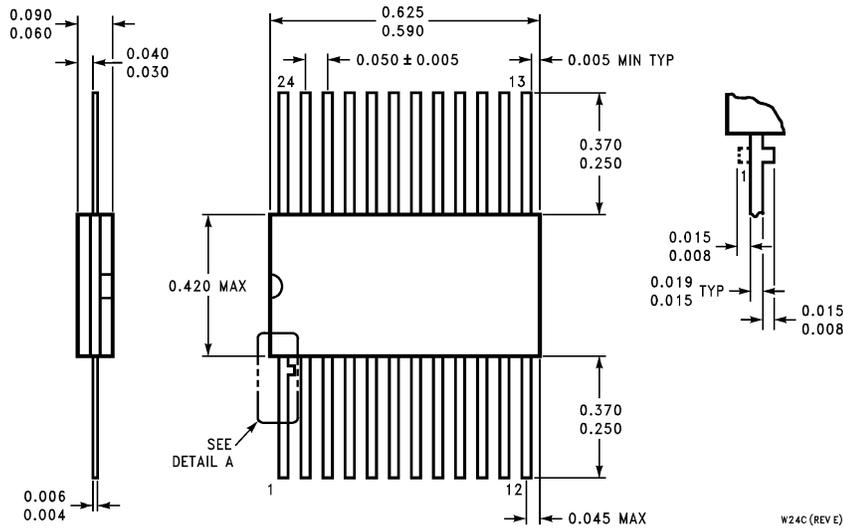
24-Lead Cerpack
NS Package Number W24C