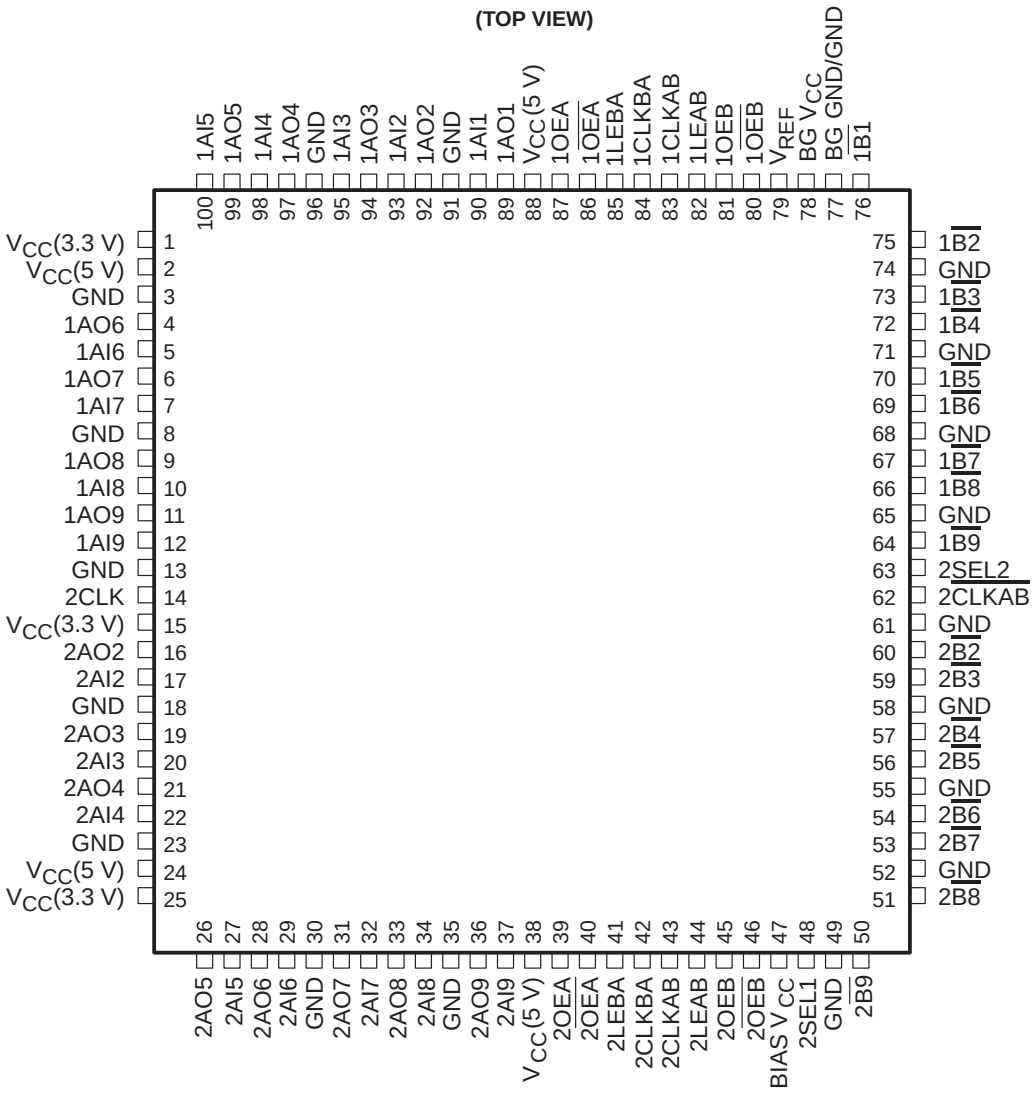
- **Compatible With IEEE Std 1194.1-1991 (BTL)**
- **LVTTL A Port, Backplane Transceiver Logic (BTL) $\overline{B}$ Port**
- **Open-Collector $\overline{B}$-Port Outputs Sink 100 mA**
- **$\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the BTL High-Level Voltage**
- **High-Impedance State During Power Up and Power Down**
- **Selectable Clock Delay**
- **TTL-Input Structures Incorporate Active Clamping Networks to Aid in Line Termination**
- **BIAS V_{CC} Minimizes Signal Distortion During Live Insertion/Withdrawal**
- **Packaged in Plastic High-Power Low-Profile Quad Flatpack**

PCA PACKAGE
(TOP VIEW)



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description

The SN74FB1653 device contains an 8-bit and a 9-bit transceiver with a buffered clock. The clock and transceivers are designed to translate signals between LVTTL and BTL environments. It is specifically designed to be compatible with IEEE Std 1194.1-1991 (BTL).

The A port operates at LVTTL signal levels. The A outputs reflect the inverse of the data at the $\overline{B}$ port when the A-port output enable (OEA) is high. When OEA is low or when V_{CC}(5 V) is typically less than 2.5 V, the A outputs are in the high-impedance state.

The $\overline{B}$ port operates at BTL signal levels. The open-collector $\overline{B}$ ports are specified to sink 100 mA. Two output enables (OEB and $\overline{OEB}$) are provided for the $\overline{B}$ outputs. When OEB is low, $\overline{OEB}$ is high, or V_{CC}(5 V) is typically less than 2.5 V, the $\overline{B}$ port is turned off.

The clock-select inputs (2SEL1 and 2SEL2) are used to configure the TTL-to-BTL clock paths and delays. Refer to the *Mux-Mode Delay* table.

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC}(5 V) is not connected.

BG V_{CC} and BG GND are the supply inputs for the bias generator.

V_{REF} is used to bypass the internal threshold reference voltage of the device. It is recommended that this pin be decoupled with a 0.1-µF capacitor.

Enhanced heat-dissipation techniques should be used when operating this device from: (a) AI to A0 at frequencies greater than 50 MHz, or (b) AI to $\overline{B}$, or $\overline{B}$ to A0 at frequencies greater than 100 MHz.

The SN74FB1653 is characterized for operation from 0°C to 70°C.

Function Tables

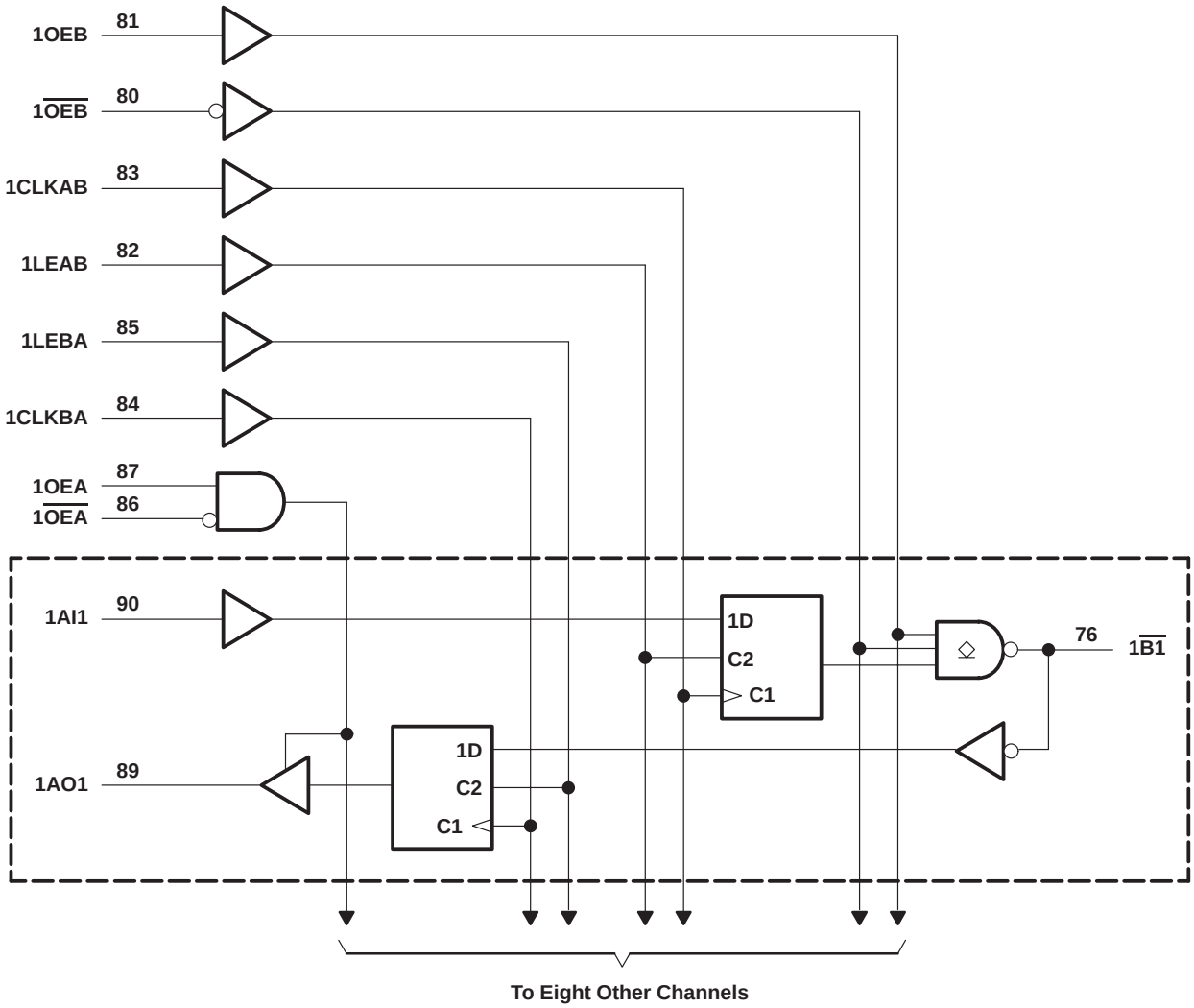
TRANSCEIVER

INPUTS				FUNCTION
$\overline{OEA}$	OEA	OEB	$\overline{OEB}$	
X	X	H	L	$\overline{A}$ data to B bus
L	H	X	X	$\overline{B}$ data to A bus
L	H	H	L	$\overline{A}$ data to B bus, $\overline{B}$ data to A bus
X	X	L	X	B-bus isolation
X	X	X	H	
H	X	X	X	A-bus isolation
X	L	X	X	

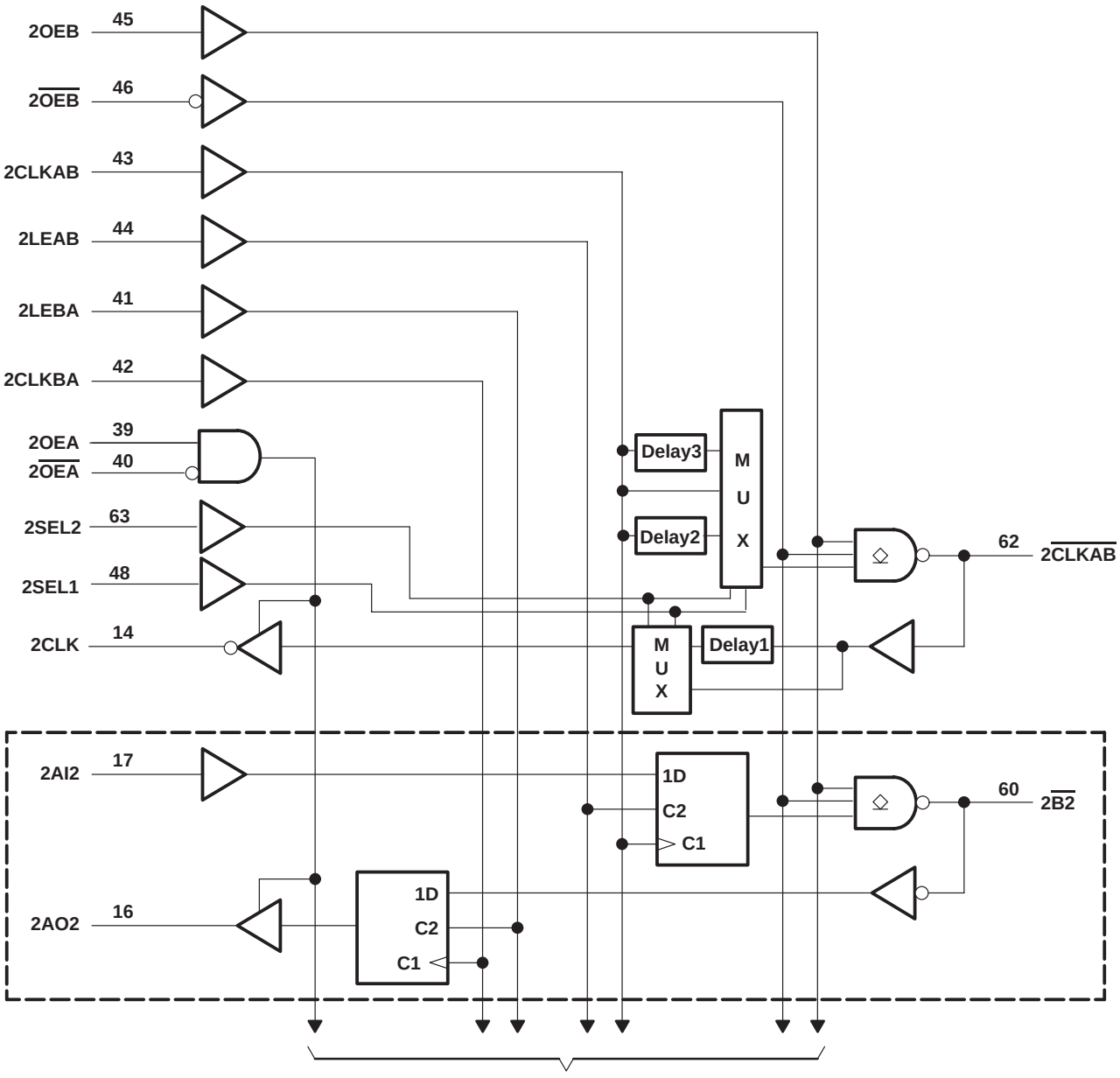
STORAGE MODE

INPUTS		FUNCTION
LE	CLK	
H	X	Transparent
L	↑	Store data
L	L	Storage

functional block diagram



functional block diagram (continued)



MUX-MODE DELAY

INPUTS		DELAY PATH†	
2SEL1	2SEL2	2CLKAB TO 2$\overline{\text{CLKAB}}$	2$\overline{\text{CLKAB}}$ TO 2CLK
L	L	No delay	No delay
L	H	No delay	Delay1
H	L	Delay2	Delay1
H	H	Delay3	Delay1

† Refer to delay1 through delay3 in the functional block diagram.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range: V_{CC}(5 V), BIAS V_{CC}, BG V_{CC} . . . . . –0.5 V to 7 V
V_{CC}(3.3 V) . . . . . –0.5 V to 4.6 V
Input voltage range, V_I: Except $\overline{B}$ port . . . . . –1.2 V to 7 V
$\overline{B}$ port . . . . . –1.2 V to 3.5 V
Input clamp current, I_{IK}: Except $\overline{B}$ port . . . . . –40 mA
$\overline{B}$ port . . . . . –18 mA
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state . . . . . –0.5 V to 3.5 V
Voltage range applied to any output in the high state . . . . . –0.5 V to V_{CC}
Current applied to any single output in the low state: A port . . . . . 48 mA
$\overline{B}$ port . . . . . 200 mA
Package thermal impedance, θ_{JA} (see Note 1) . . . . . 22°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}, BG V_{CC}, BIAS V_{CC}	Supply voltage		4.5	5	5.5	V
V_{CC}(3.3 V)	Supply voltage		3	3.3	3.6	V
V_{IH}	High-level input voltage	$\overline{B}$ port	1.62		2.3	V
		Except $\overline{B}$ port	2			
V_{IL}	Low-level input voltage	$\overline{B}$ port	0.75		1.47	V
		Except $\overline{B}$ port			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	AO port			–3	mA
I_{OL}	Low-level output current	AO port			24	mA
		$\overline{B}$ port			100	
T_A	Operating free-air temperature		0		70	°C

NOTE 2: To ensure proper device operation, all unused inputs must be terminated as follows: control inputs to V_{CC}(5 V) or GND, A inputs to V_{CC}(5 V) only, and B inputs to GND only. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	$\overline{B}$ port	V_{CC}(5 V) = 4.5 V, V_{CC}(3.3 V) = 3.3 V	I_I = –18 mA			–1.2	V
	Except $\overline{B}$ port		I_I = –40 mA			–0.5	V
V_{OH}	AO port	V_{CC}(5 V) = 4.5 V, V_{CC}(3.3 V) = 3 V	I_{OH} = –1 mA				V
			I_{OH} = –3 mA	2.5			
V_{OL}	AO port	V_{CC}(5 V) = 4.5 V, V_{CC}(3.3 V) = 3 V	I_{OL} = 24 mA		0.35	0.5	V
	$\overline{B}$ port	V_{CC}(5 V) = 4.5 V, V_{CC}(3.3 V) = 3 V	I_{OL} = 80 mA	0.75		1.1	
			I_{OL} = 100 mA			1.15	
I_I	Except $\overline{B}$ port	V_{CC}(5 V) = 5.5 V, V_{CC}(3.3 V) = 3.6 V	V_I = 5.5 V			50	µA
I_{IH}‡	Except $\overline{B}$ port	V_{CC}(5 V) = 5.5 V, V_{CC}(3.3 V) = 3.6 V	V_I = 2.7 V			50	µA
I_{IL}‡	Except $\overline{B}$ port	V_{CC}(5 V) = 5.5 V, V_{CC}(3.3 V) = 3.6 V	V_I = 0.5 V			–50	µA
	$\overline{B}$ port	V_{CC}(5 V) = 5.5 V, V_{CC}(3.3 V) = 3.6 V	V_I = 0.75 V			–100	
I_{OH}	$\overline{B}$ port	V_{CC}(5 V) = 0 to 5.5 V, V_{CC}(3.3 V) = 3.6 V	V_O = 2.1 V			100	µA
I_{OZH}	AO port	V_{CC}(5 V) = 5.5 V, V_{CC}(3.3 V) = 3.6 V	V_O = 2.7 V			50	µA
I_{OZL}	AO port	V_{CC}(5 V) = 5.5 V, V_{CC}(3.3 V) = 3.6 V	V_O = 0.5 V			–50	µA
I_{OZPU}	AO port	V_{CC} = 0 to 2.1 V,	V_O = 0.5 V to 2.7 V			–50	µA
I_{OZPD}	AO port	V_{CC} = 2.1 V to 0,	V_O = 0.5 V to 2.7 V			–50	µA
I_{CC}(5 V)	AI port to $\overline{B}$ port	V_{CC}(5 V) = 5.5 V, V_{CC}(3.3 V) = 3.3 V	I_O = 0			145	mA
	$\overline{B}$ port to AO port					130	
	Outputs disabled					120	
I_{CC}(3.3 V)	$\overline{B}$ port to AO port	V_{CC}(5 V) = 5.5 V, V_{CC}(3.3 V) = 3.3 V	I_O = 0			1	mA
C_i	Control and AI inputs	V_I = 0.5 V or 2.5 V			6.5		pF
C_o	AO port	V_O = 0.5 V or 2.5 V			3.5		pF
C_{io}	$\overline{B}$ port per IEEE Std 1194.1-1991	V_{CC}(5 V) = 0 to 5.5 V, V_{CC}(3.3 V) = 3.3 V				6.5	pF

† All typical values are at V_{CC}(5 V) = 5 V and V_{CC}(3.3 V) = 3.3 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
I_{CC} (BIAS V_{CC})		V_{CC}(5 V) = 0 to 4.5 V, V_{CC}(3.3 V) = 3.3 V	V_B = 0 to 2 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		450	µA
		V_{CC}(5 V) = 4.5 V to 5.5 V, V_{CC}(3.3 V) = 3.3 V			10	
V_O	$\overline{B}$ port	V_{CC}(5 V) = 0, V_{CC}(3.3 V)= 0 V	V_I (BIAS V_{CC}) = 5 V	1.62	2.1	V
I_O	$\overline{B}$ port	V_{CC}(5 V) = 0, V_{CC}(3.3 V) = 0 V	V_B = 1 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	–1		µA
		V_{CC}(5 V) = 0 to 5.5 V, V_{CC}(3.3 V) = 3.3 V	OEB = 0 to 0.8 V		100	
		V_{CC}(5 V) = 0 to 2.2 V, V_{CC}(3.3 V) = 3.3 V	OEB = 0 to 5 V		100	

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

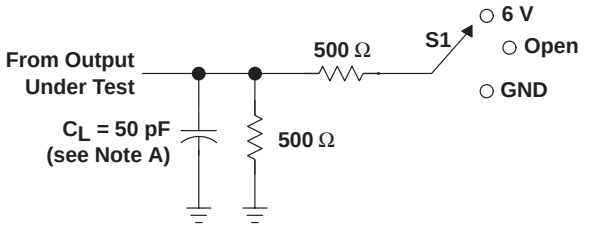
			MIN	MAX	UNIT
f_{clock}	Clock frequency			90	MHz
t_w	Pulse duration	LE high	3		ns
		CLK high or low	3		
t_{su}	Setup time	AI or $\overline{B}$ before LE↓	3.5		ns
		AI or $\overline{B}$ before CLK↑	3.5		
t_h	Hold time	AI or $\overline{B}$ after LE↓	1		ns
		AI or $\overline{B}$ after CLK↑	0.7		

switching characteristics over recommended operating free-air temperature range, V_{CC}(5 V) = 5 V ± 0.5 V and V_{CC}(3.3 V) = 3.3 V (see Figure 1)

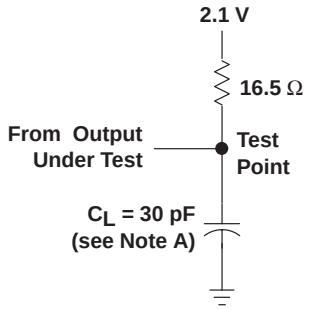
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}			90		MHz
t_{PLH}	AI	$\overline{B}$	1.8	6.2	ns
t_{PHL}			2.9	6.6	
t_{PLH}	LEAB	$\overline{B}$	2.7	6.9	ns
t_{PHL}			3.5	7.3	
t_{PLH}	CLKAB	$\overline{B}$	2.3	6.4	ns
t_{PHL}			2.9	6.7	
t_{PLH}	2CLKAB (no delay)	$2\overline{CLKAB}$	2.3	6	ns
t_{PHL}			2.9	6.7	
t_{PLH}	2CLKAB (delay2)	$2\overline{CLKAB}$	4.5	9.5	ns
t_{PHL}			4.5	9.5	
t_{PLH}	2CLKAB (delay3)	$2\overline{CLKAB}$	9.3	15.4	ns
t_{PHL}			9.3	15.4	
t_{PLH}	$\overline{B}$	AO	2	6.5	ns
t_{PHL}			2	6.5	
t_{PLH}	LEBA	AO	1.8	6.3	ns
t_{PHL}			1.8	6.3	
t_{PLH}	CLKBA	AO	1.8	6.3	ns
t_{PHL}			1.8	6.3	
t_{PLH}	$2\overline{CLKAB}$ (delay1)	2CLK	5.7	12.3	ns
t_{PHL}			5.7	12.3	
t_{PLH}	$2\overline{CLKAB}$ (no delay)	2CLK	2	6.5	ns
t_{PHL}			2	6.5	
t_{PLH}	OEB or $\overline{OEB}$	$\overline{B}$	2.6	7	ns
t_{PHL}			2.6	7	
t_{PZH}	OEA or $\overline{OEA}$	AO	1.4	5.5	ns
t_{PZL}			1.4	5.5	
t_{PHZ}	OEA or $\overline{OEA}$	AO	1.4	6.5	ns
t_{PLZ}			1.4	5.8	
$t_{sk(p)}$†	Pulse skew, AI to $\overline{B}$ or $\overline{B}$ to AO			1.6	ns
	Pulse skew, $2\overline{CLKAB}$ to 2CLK			1.8	
$t_{sk(p)}$	Pulse skew, CLKAB to $\overline{B}$ or CLKBA to AO			1.5	ns
	Pulse skew, CLKAB to $2\overline{CLKAB}$			1.4	
$t_{sk(HL)}$, $t_{sk(LH)}$†	Pulse skew, AI to $\overline{B}$ or $\overline{B}$ to AO			1	ns
$t_{sk(o)}$‡	Pulse skew, non-delayed mode for $2\overline{CLKAB}$, CLKAB to AO			1	ns
	Pulse skew, non-delayed mode for $2\overline{CLKAB}$, CLKAB to $\overline{B}$ and $2\overline{CLKAB}$			1	
$t_{sk(o)}$‡	Pulse skew, non-delayed mode for $2\overline{CLKAB}$, CLKAB to $\overline{B}$ and $2\overline{CLKAB}$			1.5	ns
t_t	Transition time, $\overline{B}$ outputs (1.3 V to 1.8 V)		0.5	4.6	ns
	Transition time, AO outputs (10% to 90%)		0.4	4.2	
t_{PR}	$\overline{B}$-port input pulse rejection		1		ns

† Skew values are applicable for through mode only, with single-output switching.
‡ Skew values are applicable for CLK mode only, with all outputs simultaneously switching high-to-low or low-to-high.

PARAMETER MEASUREMENT INFORMATION

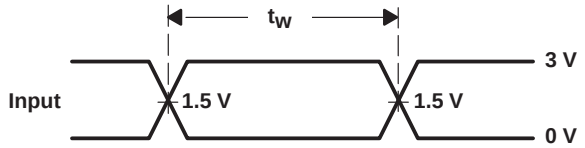


LOAD CIRCUIT FOR A OUTPUTS

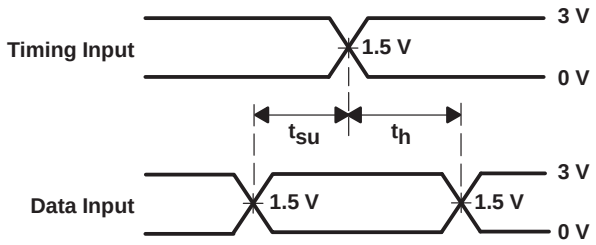


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

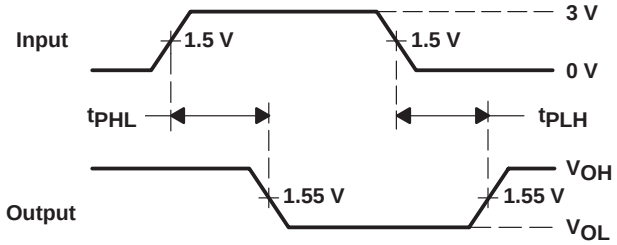
LOAD CIRCUIT FOR B OUTPUTS



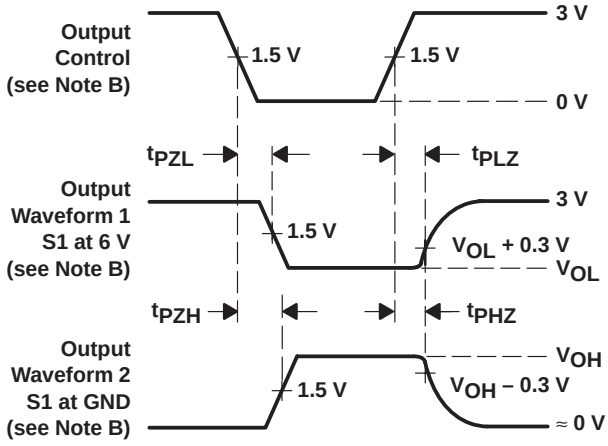
VOLTAGE WAVEFORMS
PULSE DURATION



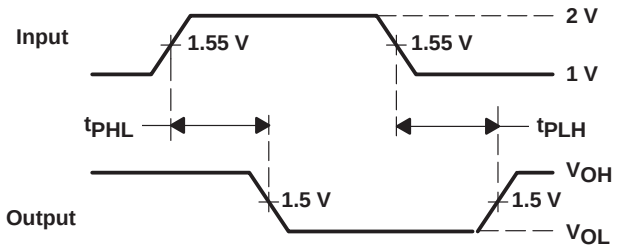
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A to B)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B to A)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: TTL inputs – PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns. BTL inputs – PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 1 ns, t_f ≤ 1 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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