



Integrated Device Technology, Inc.

16-BIT SYNCHRONOUS 2:1 MUX/DEMUX SWITCH

**IDT74FST163232
ADVANCE INFORMATION**

FEATURES:

- Bus switches provide zero delay paths
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- Low switch on-resistance:
FST163xxx – 4Ω
- TTL-compatible input and output levels
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- Available in SSOP, TSSOP and TVSOP

DESCRIPTION:

The FST163232 belong to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. Thus they generate little or no noise of their own while providing a low resistance path for an external

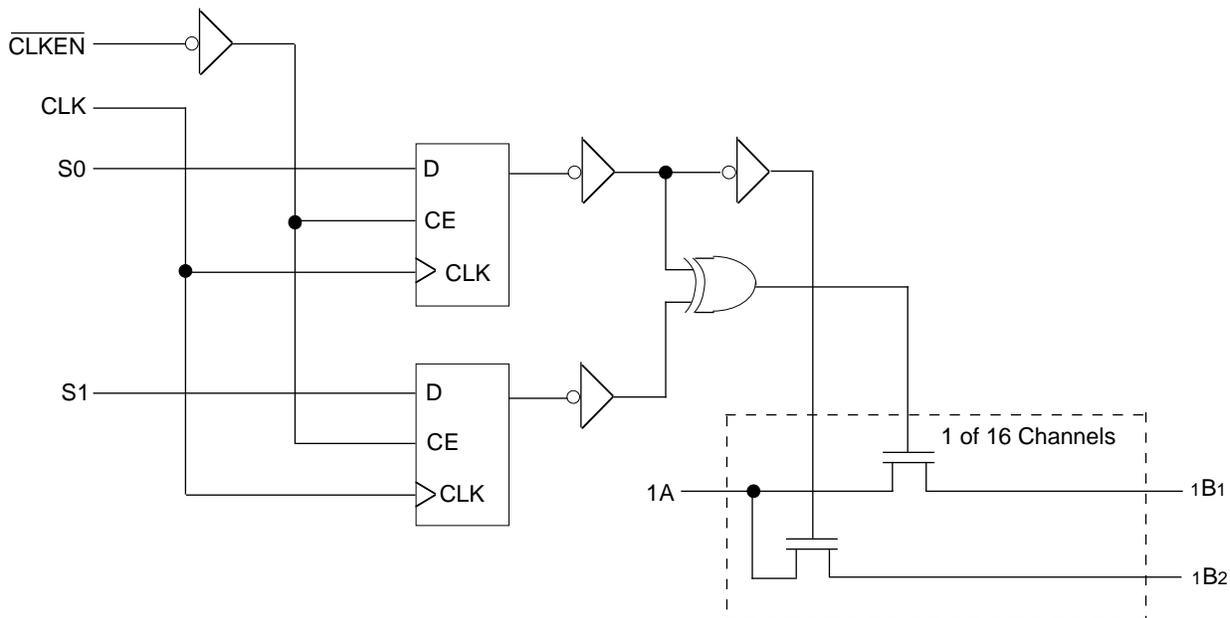
driver. These devices connect input and output ports through an n-channel FET. When the gate-to-source junction of this FET is adequately forward-biased the device conducts and the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off, therefore with no VCC applied, the device has hot insertion capability.

The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

The FST163232 provides three 16-bit TTL-compatible ports that support 2:1 multiplexing. The S_{0,1} pins control mux select and switch enable/disable. The S_{0,1} inputs are synchronous and clocked on the rising edge of CLK when $\overline{\text{CLKEN}}$ is low.

Port A can be connected to port B1 or port B2 or both ports B1 and B2.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin Names	I/O	Description
A	I/O	Bus A
B1, B2	I/O	Buses B1, B2
S _{0,1}	I	Control Pins
CLK	I	Clock Input. Clocks S _{0,1} on Rising Edge
$\overline{\text{CLKEN}}$	I	Clock Enable Input

3511 tbl 01

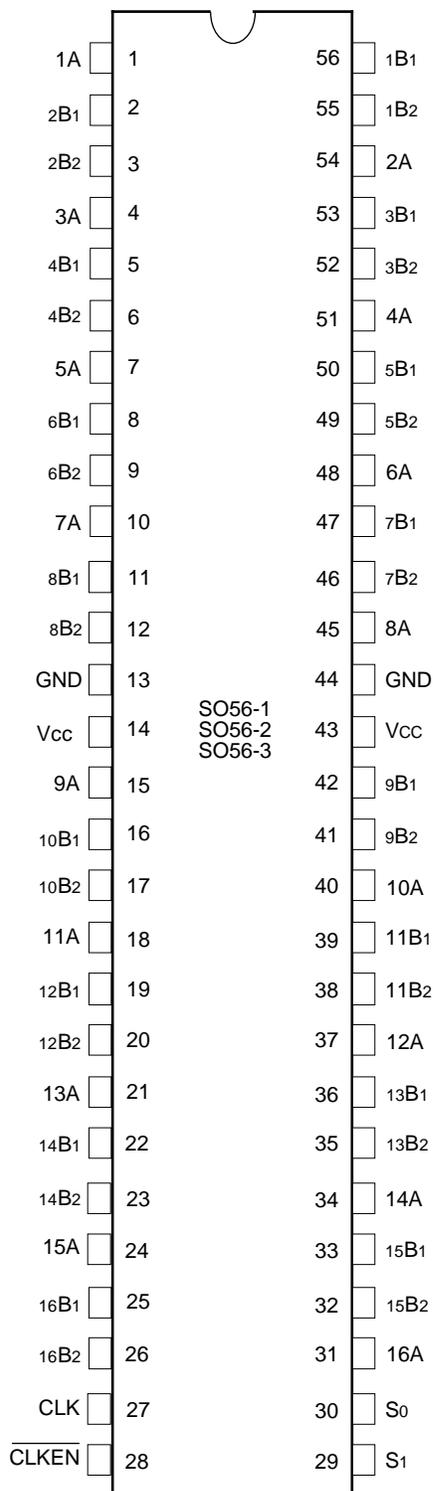
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COMMERCIAL TEMPERATURE RANGE

FEBRUARY 1997

PIN CONFIGURATION



SSOP/
TSSOP/TVSOP
TOP VIEW

3511 drw 02

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	Maximum Continuous Channel Current	128	mA

3511 tbl 02

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Vcc, Control and Switch terminals.

CAPACITANCE⁽¹⁾

Symbol	Parameter	Conditions ⁽²⁾	Typ.	Unit
CIN	Control Input Capacitance		4	pF
CI/O	Switch Input/Output Capacitance	Switch Off		pF

3511 tbl 03

NOTES:

- Capacitance is characterized but not tested
- T_A = 25°C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V

FUNCTION TABLE

S ₁	S ₀	CLK	CLKEN	Description
X	X	X	H	Last state
L	L	↑	L	Disconnect
L	H	↑	L	A to B ₁ and A to B ₂
H	L	↑	L	A to B ₁ or B ₁ to A
H	H	↑	L	A to B ₂ or B ₂ to A

3511 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2.0	—	—	V	
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	—	—	0.8	V	
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	± 1	μA
I_{IL}	Input LOW Current		$V_I = \text{GND}$	—	—	± 1	μA
I_{OZH}	High Impedance Output Current (3-State Output pins)	$V_{CC} = \text{Max.}$	$V_O = V_{CC}$	—	—	± 1	μA
I_{OZL}			$V_O = \text{GND}$	—	—	± 1	μA
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$	—	300	—	mA	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$	—	-0.7	-1.2	V	
R_{ON}	Switch On Resistance ⁽⁴⁾	$V_{CC} = \text{Min.}, V_{IN} = 0.0\text{V}$ $I_{ON} = 64\text{mA}$	—	4	7	Ω	
		$V_{CC} = \text{Min.}, V_{IN} = 0.0\text{V}$ $I_{ON} = 32\text{mA}$	—	4	7	Ω	
		$V_{CC} = \text{Min.}, V_{IN} = 2.4\text{V}$ $I_{ON} = 15\text{mA}$	—	6	15	Ω	
I_{OFF}	Input/Output Power Off Leakage	$V_{CC} = 0\text{V}, V_{IN}$ or $V_O \leq 4.5\text{V}$	—	—	± 1	μA	
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND}$ or V_{CC}	—	0.1	3	μA	

NOTES:

3511 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Measured by voltage drop between ports at indicated current through the switch.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open Enable Pin Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	30	40	$\mu A/$ MHz/ Switch
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open CLK Pin Toggling (16 Switches Toggling) $f_i = 10\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	4.8	6.4	mA
			$V_{IN} = 3.4$ $V_{IN} = GND$	—	5.1	7.2	

NOTES:

3511 tbl 06

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ C$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_i N)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_i = Input Frequency
 N = Number of Switches Toggling at f_i
 All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^\circ C$ to $+85^\circ C$, $V_{CC} = 5.0V \pm 10\%$

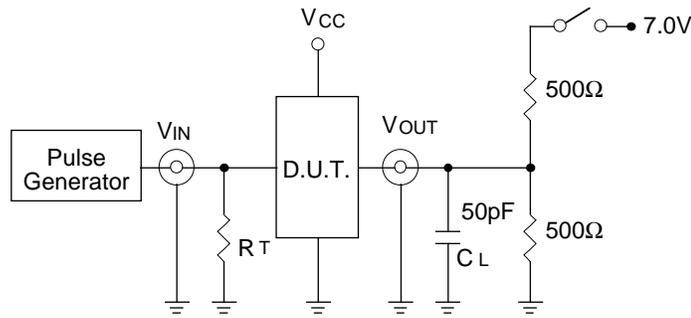
Symbol	Description	Condition ⁽¹⁾	Min. ⁽²⁾	Typ.	Max.	Unit
t_{PLH} t_{PHL}	Data Propagation Delay A to B, B to A ^(3,4)	$CL = 50pF$ $RL = 500\Omega$	—	—	0.25	ns
t_{CEWS}	Clock Enable Set-Up Time \overline{CLKEN} to CLK Low-to-High		—	—	ns	
t_{CENH}	Clock Enable Hold Time \overline{CLKEN} to CLK Low-to-High		—	—	ns	
t_{BX}	Switch Multiplex Delay CLK to A, B		1.5	—	6.5	ns
t_{PZH} t_{PZL}	Switch Turn on Delay CLK to A, B		1.5	—	6.5	ns
t_{PHZ} t_{PLZ}	Switch Turn off Delay CLK to A, B		1.5	—	7	ns
$ Q_{CI} $	Charge Injection, Typical ^(5,7)		—	1.5	—	pC
$ Q_{DCI} $	Differential Charge Injection, Typical ^(6,7)		—	0.5	—	

NOTES:

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- See test circuit and waveforms.
- Minimum limits guaranteed but not tested.
- This parameter is guaranteed by design but not tested.
- The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 2.5ns for 50pF load. Since this time is constant and much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay on the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
- Measured at switch turn off, load = 50 pF in parallel with 10 M Ω scope probe, $V_{IN} = 0.0$ volts.
- Measured at switch turn off through bus multiplexer, (e.g.- A to B₁ =>A to B₂), load = 50 pF in parallel with 10 M Ω scope probe, V_{IN} at A = 0.0 volts. Charge injection is reduced because the injection from the turn off of the A to B₁ switch is compensated by the turn on of the A to B₂ switch.
- Characterized parameter. Not 100% tested.

TEST CIRCUITS AND WAVEFORMS
TEST CIRCUITS FOR ALL OUTPUTS



3511 Ink 03

SWITCH POSITION

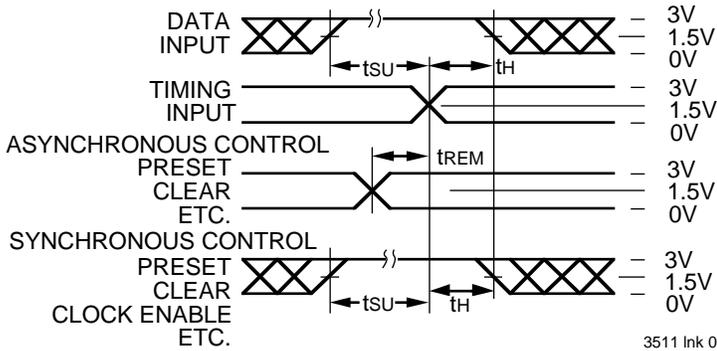
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

CL= Load capacitance: includes jig and probe capacitance.
RT= Termination resistance: should be equal to ZOUT of the Pulse Generator.

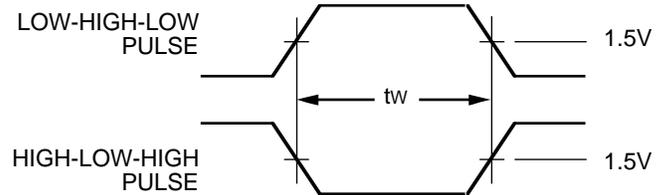
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SET-UP, HOLD AND RELEASE TIMES



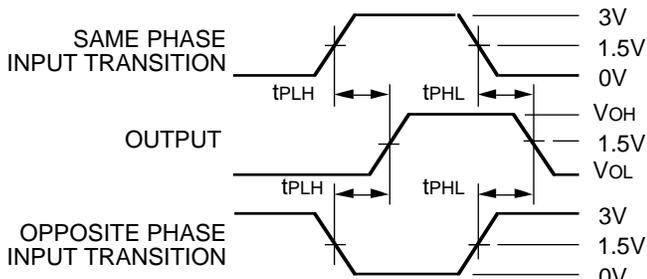
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PULSE WIDTH



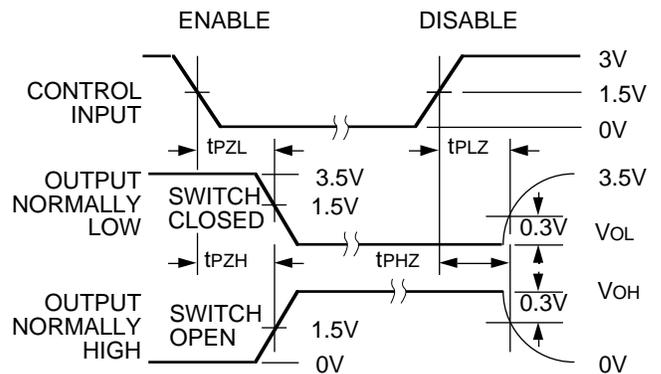
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PROPAGATION DELAY



3511 Ink 06

ENABLE AND DISABLE TIMES

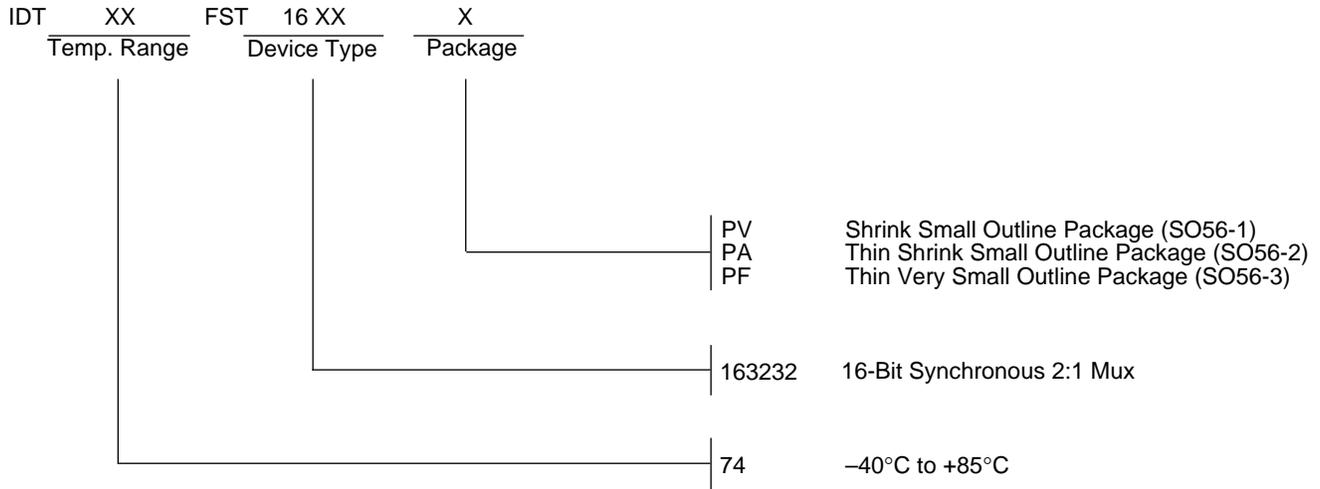


NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tr ≤ 2.5ns; tr ≤ 2.5ns

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ORDERING INFORMATION



3511 ldrw 08

Integrated Device Technology, Inc. reserves the right to make changes to the specifications in this data sheet in order to improve design or performance and to supply the best possible product.

Integrated Device Technology, Inc.

2975 Stender Way, Santa Clara, CA 95054-3090

Telephone: (408) 727-6116

FAX 408-492-8674

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