

Structure	Silicon monolithic integrated circuit
Product name	Power management switch
Type	BD6524HFV
Features	Low on resistance (Typ. = 200mΩ) Output load current (I_{OUT} 0 ~ 500mA) Control input : High Active

◇ Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{IN}	-0.3 ~ 6.0	V
Control Input voltage	V_{EN}	-0.3 ~ $V_{IN} + 0.3$	V
Switch output voltage	V_{OUT}	-0.3 ~ 6.0	V
Storage temperature	T_{STG}	-55 ~ 150	°C
Power Dissipation *1	P_d	510	mW

*1 Derating : 4.08mW/°C for operation above Ta = 25°C

* This product is not designed for protection against radioactive rays.

* Operation is not guaranteed.

◇ Operating conditions (Ta=-25°C~75°C)

Parameter	Symbol	MIN	TYP	MAX	Unit
Supply voltage	V_{IN}	3.0	5.0	5.5	V
Switch current	I_{OUT}	0	-	500	mA

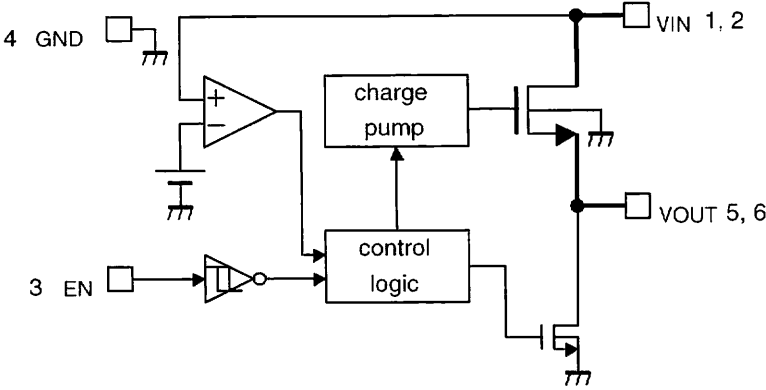
Application example

- ROHM cannot provide adequate confirmation of patents.
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◇ Electric characteristics (Unless otherwise specified, Ta = 25, VIN = 5V)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Operating Current	I _{DD}	-	50	75	uA	V _{EN} = 5V, V _{OUT} = Open
Standby Current	I _{STB}	-	0.1	1	uA	V _{EN} = 0V, V _{OUT} = Open
EN input voltage	V _{EN}	-	-	2.5	V	High level input voltage
		0.7	-	-	V	Low level input voltage
EN input leak current	I _{EN}	-1	0.01	1	uA	
Switch ON resistance	R _{ON}	-	200	255	mΩ	V _{IN} = 5V
		-	250	335	mΩ	V _{IN} = 3.3V
Switch leak current	I _{LEAK}	-	-	10	uA	At switch OFF
Switch rise time	T _{ON1}	-	0.4	0.8	ms	RL=10Ω
Switch rise delay time	T _{ON2}	-	0.5	1.0	ms	RL=10Ω
Switch fall time	T _{OFF1}	-	1	2	us	RL=10Ω
Switch fall delay time	T _{OFF2}	-	2	4	us	RL=10Ω
UVLO threshold voltage	V _{UVLO}	1.9	2.2	2.5	V	At V _{IN} increase
		1.8	2.1	2.4	V	At V _{IN} decrease
Discharge resistance	R _{DISC}	-	200	350	Ω	V _{EN} = 0V, I _L = 1mA
Discharge current	I _{DISC}	0.8	1.8	-	mA	V _{EN} = 0V V _{IN} = V _{OUT} = 1.8V

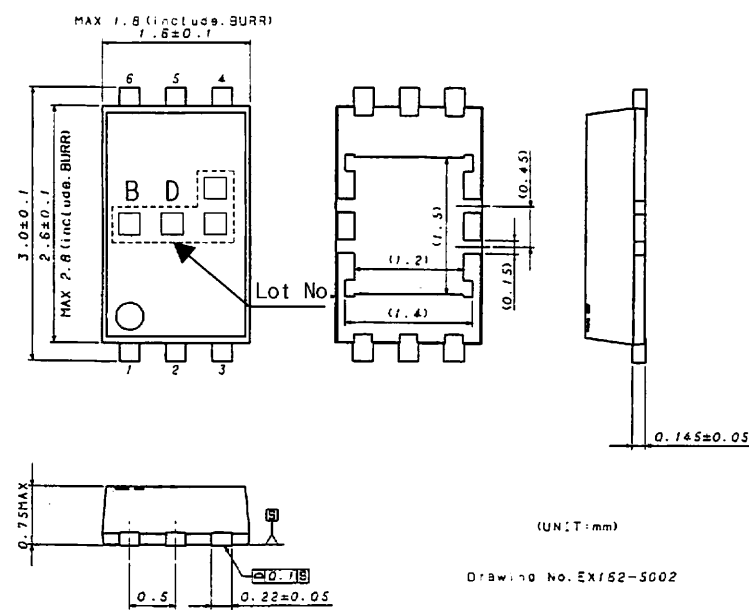
◇ Block diagram



◇ Pin Description

Pin Number	Pin Name	Pin Function
1	VIN	Supply Input
2	VIN	Supply Input
3	EN	Enable Input
4	GND	Ground
5	VOUT	Switch Output
6	VOUT	Switch Output

◇ Package outline



HVSO6 (Unit : mm)

◇Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Power supply and GND line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. Pay attention to the interference by common impedance of layout pattern when there are plural power supplies and GND lines. Especially, when there are GND pattern for small signal and GND pattern for large current included the external circuits, separate each GND pattern. Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use a capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(3) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(4) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(5) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(6) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(7) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(8) Thermal design

Perform thermal design in which there are adequate margins by taking into account the power dissipation (P_d) in actual states of use.

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