13-BIT 250 MSPS ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 13-Bit Resolution
- 250 MSPS Sample Rate
- SNR = 68.7 dBc at 100-MHz IF and 250 MSPS
- SFDR = 71 dBc at 100-MHz IF and 250 MSPS
- SNR = 67.6 dBc at 230-MHz IF and 250 MSPS
- SFDR = 78 dBc at 230-MHz IF and 250 MSPS
- 2.2 V_{PP} Differential Input Voltage
- Fully Buffered Analog Inputs
- 5 V Analog Supply Voltage
- 3.3 V LVDS Compatible Outputs
- Total Power Dissipation: 2.1 W
- 2's Complement Output Format
- TQFP-80 PowerPAD™ Package
- Industrial Temperature Range = –40°C to 85°C

APPLICATIONS

- Test and Measurement
- Software-Defined Radio
- Multi-channel Basestation Receivers
- Basestation TX Digital Predistortion
- Communications Instrumentation

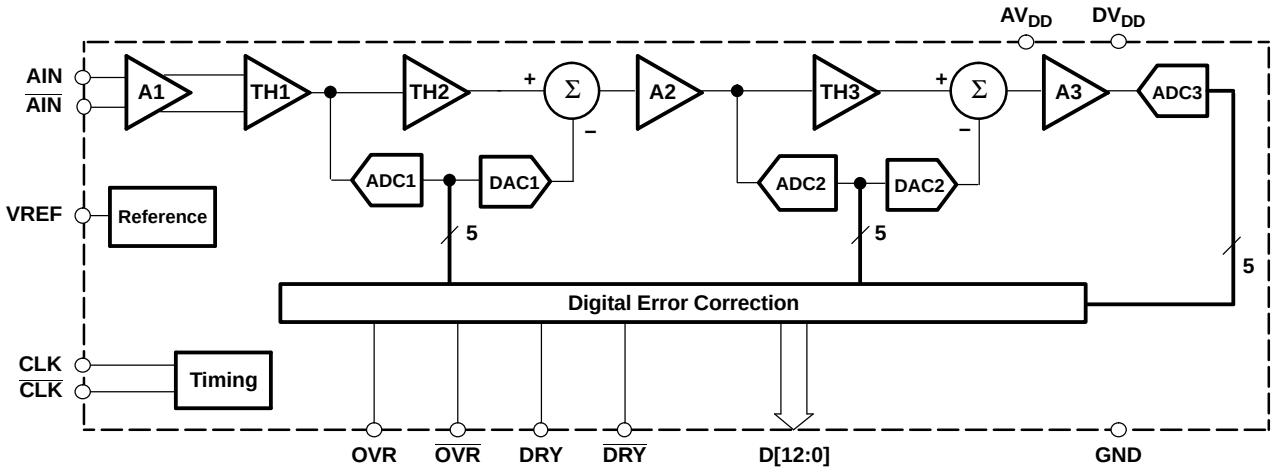
RELATED PRODUCTS

- ADS5424 - 14-bit, 105 MSPS
- ADS5423 - 14-bit, 80 MSPS
- ADS5440 - 13-bit, 210 MSPS

PRODUCT PREVIEW

DESCRIPTION

The ADS5444 is a 13-bit 250 MSPS analog-to-digital converter (ADC) that operates from a 5 V supply, while providing LVDS-compatible digital outputs from a 3.3 V supply. The ADS5444 input buffer isolates the internal switching of the onboard track and hold (T&H) from disturbing the signal source. An internal reference generator is also provided to further simplify the system design. The ADS5444 has outstanding low noise and linearity over input frequency.



The ADS5444 is available in an 80-pin TQFP PowerPAD™ package. The ADS5444 is built on state of the art Texas Instruments complementary bipolar process (BiCom3X) and is specified over the full industrial temperature range (–40°C to 85°C).

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGING/ORDERING INFORMATION(1)

Product	Package-Lead	Package Designator (1)	Specified Temperature Range	Package Marking	Ordering Number	Transport Media, Quantity
ADS5444	HTQFP-80(2) PowerPAD	PFP	–40°C to 85°C	ADS5444I	ADS5444IPFP	Tray, 96
					ADS5444IPFPR	Tape and Reel, 1000

(1) For the most current product and ordering information, see the Package Option Addendum located at the end of this data sheet.
(2) Thermal pad size: 6 x 6 array of thermal vias with a maximum thermal pad size of 10 mm x 10 mm

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE / UNIT
Supply voltage	AV_{DD} to GND	6 V
	DRV_{DD} to GND	5 V
Analog input to GND		–0.3 V to AV_{DD}+0.3 V
Clock input to GND		–0.3 V to AV_{DD}+0.3 V
CLK to $\overline{CLK}$		±2.5
Digital data output to GND		–0.3 V to DRV_{DD}+0.3 V
Operating temperature range		–40°C to 85°C
Maximum junction temperature		150°C
Storage temperature range		–65°C to 150°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only and functional operation of the device at these or any other conditions beyond those specified is not implied.

THERMAL CHARACTERISTICS(1)

PARAMETER	TEST CONDITIONS	TYP	UNIT
θ_{JA}	Soldered slug, no airflow	21.7	°C/W
	Soldered slug, 250-LFPM airflow	15.4	°C/W
	Unsoldered slug, no airflow	50	°C/W
	Unsoldered slug, 250-LFPM airflow	43.4	°C/W
θ_{JC}	Bottom of package (heatslug)	2.99	°C/W

(1) Using 36 thermal vias (6 x 6 array). See the Application Section.

PRODUCT PREVIEW

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
SUPPLIES					
AV_{DD}	Analog supply voltage	4.75	5	5.25	V
DRV_{DD}	Output driver supply voltage	3	3.3	3.6	V
ANALOG INPUT					
	Differential input range		2.2		V_{PP}
V_{CM}	Input common mode		2.4		V
CLOCK INPUT					
$1/t_C$	ADCLK input sample rate (sine wave)			250	MSPS
	Clock amplitude, differential sine wave		3		Vpp
	Clock duty cycle		50%		
T_A	Open free air temperature	–40		85	°C

ELECTRICAL CHARACTERISTICS

MIN, TYP, and MAX values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, sampling rate = 250 MSPS, 50% clock duty cycle, AV_{DD} = 5 V, DRV_{DD} = 3.3 V, –1 dBFS differential input, and 3 V_{PP} differential clock, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution			13		Bits
ANALOG INPUTS						
	Differential input range			2.2		V_{pp}
	Differential input resistance (DC)			1		kΩ
	Differential input capacitance			1.5		pF
	Analog input bandwidth			1000		MHz
INTERNAL REFERENCE VOLTAGE						
VREF	Reference voltage			2.4		V
DYNAMIC ACCURACY						
	No missing codes			Tested		
DNL	Differential linearity error	f_{IN} = 10 MHz		±0.9		LSB
INL	Integral linearity error	f_{IN} = 10 MHz		±1.5		LSB
	Offset error		–5		5	mV
	Offset temperature coefficient					mV/°C
	Gain error		–5		5	%FS
	Gain temperature coefficient					Δ%/°C
	PSRR					mV/V
POWER SUPPLY						
I_{AVDD}	Analog supply current	V_{IN} = full scale, f_{IN} = 70 MHz, F_S = 250 MSPS		365		mA
I_{DRVDD}	Output buffer supply current			76		mA
	Power dissipation			2.1		W
	Power-up time			20		ms
DYNAMIC AC CHARACTERISTICS						
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz		69.1		dBc
		f_{IN} = 70 MHz		68.9		
		f_{IN} = 100 MHz		68.7		
		f_{IN} = 170 MHz		68.1		
		f_{IN} = 230 MHz		67.6		
		f_{IN} = 300 MHz		66.8		
		f_{IN} = 400 MHz		66.0		

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

MIN, TYP, and MAX values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, sampling rate = 250 MSPS, 50% clock duty cycle, AV_{DD} = 5 V, DRV_{DD} = 3.3 V, –1 dBFS differential input, and 3 V_{PP} differential clock, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SFDR	Spurious free dynamic range	f_{IN} = 10 MHz		83		dBc
		f_{IN} = 70 MHz		77		
		f_{IN} = 100 MHz		71		
		f_{IN} = 170 MHz		73		
		f_{IN} = 230 MHz		78		
		f_{IN} = 300 MHz		70		
		f_{IN} = 400 MHz		63		
HD2	Second harmonic	f_{IN} = 10 MHz		88		dBc
		f_{IN} = 70 MHz		82		
		f_{IN} = 100 MHz		78		
		f_{IN} = 170 MHz		75		
		f_{IN} = 230 MHz		78		
		f_{IN} = 300 MHz		70		
		f_{IN} = 400 MHz		63		
HD3	Third harmonic	f_{IN} = 10 MHz		83		dBc
		f_{IN} = 70 MHz		79		
		f_{IN} = 100 MHz		72		
		f_{IN} = 170 MHz		76		
		f_{IN} = 230 MHz		90		
		f_{IN} = 300 MHz		81		
		f_{IN} = 400 MHz		68		
	Worst other harmonic/spur (other than HD2 and HD3)	f_{IN} = 10 MHz		95		dBc
		f_{IN} = 70 MHz		92		
		f_{IN} = 100 MHz		83		
		f_{IN} = 170 MHz		88		
		f_{IN} = 230 MHz		89		
		f_{IN} = 300 MHz		87		
		f_{IN} = 400 MHz		76		
	SINAD	f_{IN} = 10 MHz		68.8		dBc
		f_{IN} = 70 MHz		68.1		
		f_{IN} = 100 MHz		66.2		
		f_{IN} = 170 MHz		66.4		
		f_{IN} = 230 MHz		67.1		
		f_{IN} = 300 MHz		64.8		
		f_{IN} = 400 MHz		60.2		
ENOB	Effective number of bits	f_{IN} = 70 MHz		11		Bits
	RMS idle channel noise	Inputs tied to common-mode		0.4		LSB
DIGITAL CHARACTERISTICS – LVDS DIGITAL OUTPUTS						
	Differential output voltage			0.35		V
	Output offset voltage		1.125		1.375	V

PRODUCT PREVIEW

TIMING CHARACTERISTICS

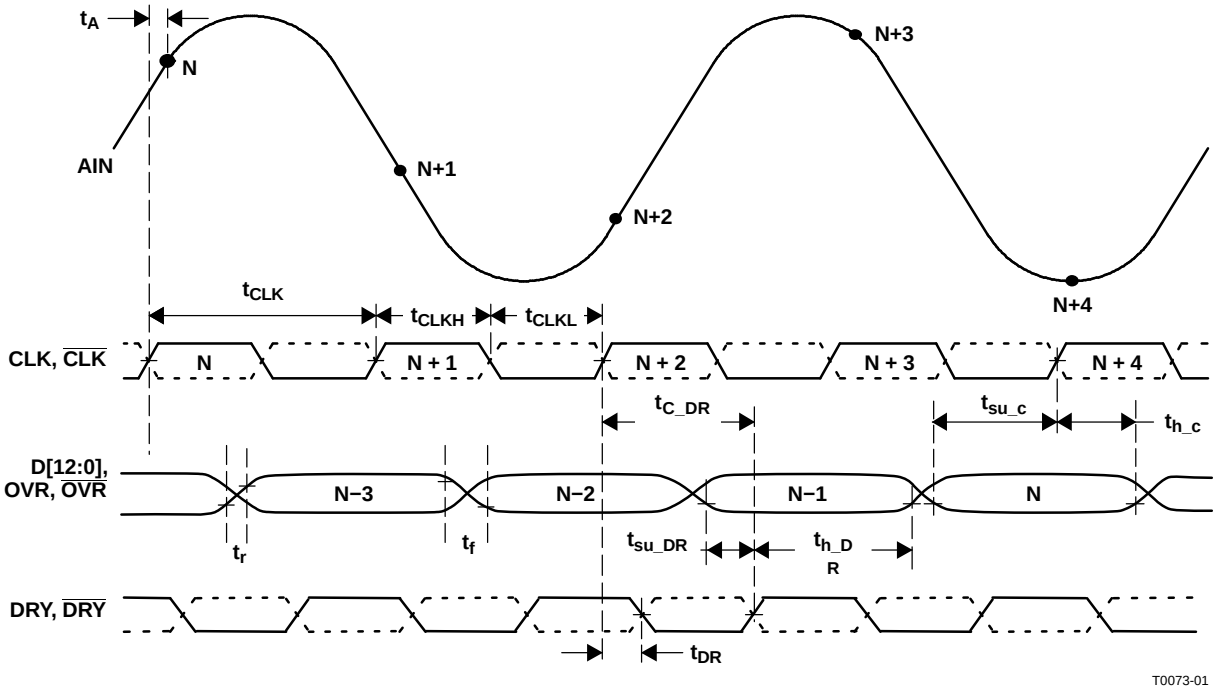


Figure 1. Timing Diagram

TIMING CHARACTERISTICS

over full temperature range, 50% clock duty cycle, sampling rate = 250 MSPS, AV_{DD} = 5 V, DRV_{DD} = 3.3 V

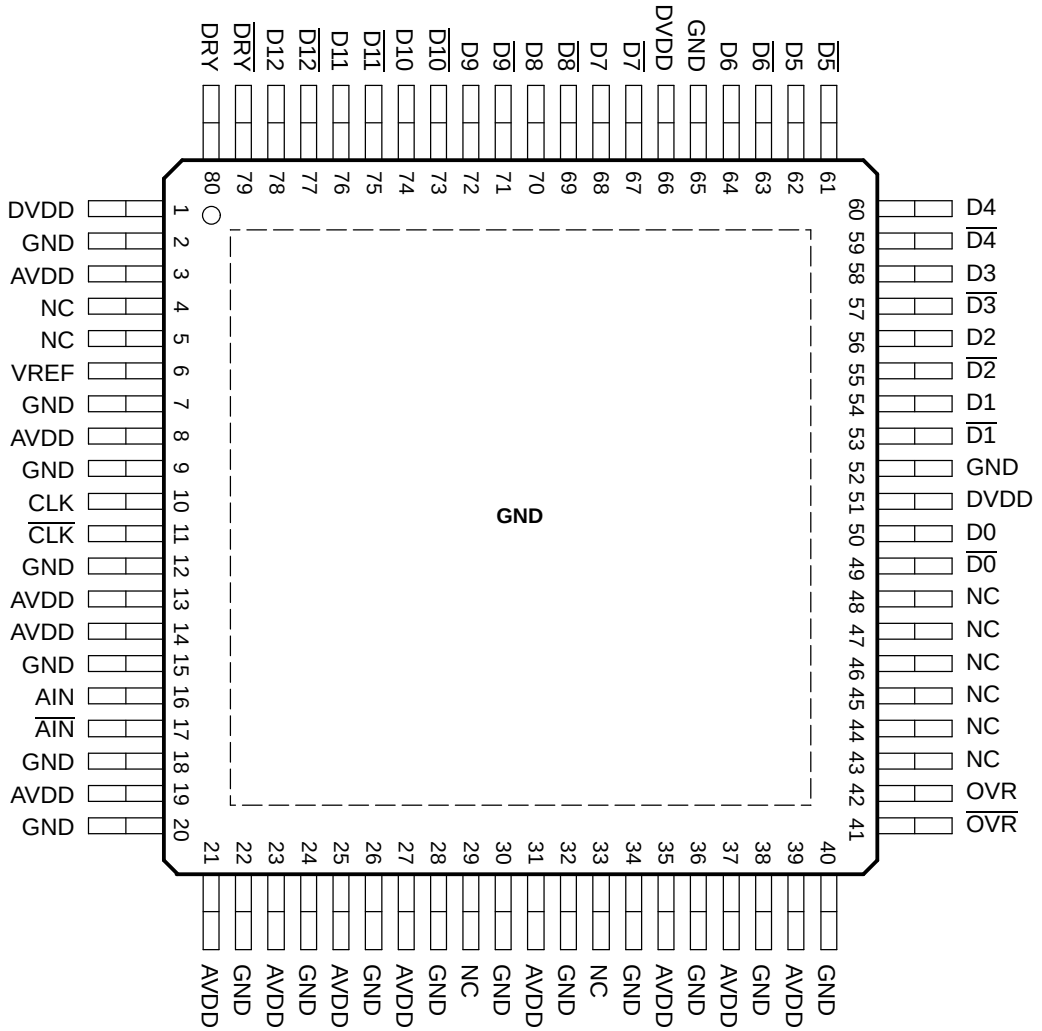
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_A	Aperture delay					ps
t_J	Clock slope independent Aperture uncertainty (jitter)					fs
k_J	Clock slope jitter factor dependency					s/V
	Latency			4		cycles
Clock Input						
t_{CLK}	Clock period			4.0		ns
t_{CLKH}	Clock pulsewidth high			2.0		ns
t_{CLKL}	Clock pulsewidth low			2.0		ns
Clock to DataReady (DRY)						
t_{DR}	Clock rising to DataReady falling			2.08		ns
t_{C_DR}	Clock rising to DataReady rising	Clock duty cycle = 50% (1)		4.08		ns
Clock to DATA, OVR(2)						
t_r	Data V_{OL} to Data V_{OH} (rise time)			0.8		ns
t_f	Data V_{OH} to Data V_{OL} (fall time)			0.8		ns
t_{su_c}	Data valid to clock (setup time)			2.4		ns
t_{h_c}	Clock to invalid Data (hold time)			5.5		ns
DataReady (DRY)/DATA, OVR(2)						
$t_{su\_DR)}$	Data valid to DRY			1.7		ns
$t_{h\_DR)}$	DRY to invalid Data			1.4		ns

(1) $t_{C\_DR} = t_{DR} + t_{CLKH}$ for clock duty cycles other than 50%
(2) Data is updated with clock rising edge or DRY falling edge.

PRODUCT PREVIEW

DEVICE INFORMATION

PFP PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
AVDD	3, 8, 13, 14, 19, 21, 23, 25, 27, 31, 35, 37, 39	Analog power supply
DVDD	1, 51, 66	Output driver power supply
GND	2, 7, 9, 12, 15, 18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 52, 65	Ground
VREF	6	Reference voltage
CLK	10	Differential input clock (positive). Conversion initiated on rising edge
$\overline{\text{CLK}}$	11	Differential input clock (negative)
AIN	16	Differential input signal (positive)
$\overline{\text{AIN}}$	17	Differential input signal (negative)
OVR, $\overline{\text{OVR}}$	42, 41	Over range indicator LVDS output. A logic high signals an analog input in excess of the full-scale range.

PRODUCT PREVIEW

DEVICE INFORMATION (continued)

TERMINAL FUNCTIONS (continued)

TERMINAL		DESCRIPTION
NAME	NO.	
D0, $\overline{D0}$	50, 49	LVDS digital output pair, least-significant bit (LSB)
D1–D6, $\overline{D1}$–$\overline{D6}$	53–64	LVDS digital output pairs
D7–D11, $\overline{D7}$–$\overline{D11}$	67–76	LVDS digital output pairs
D12, $\overline{D12}$	78, 77	LVDS digital output pair, most-significant bit (MSB)
DRY, $\overline{DRY}$	80, 79	Data ready LVDS output pair
NC	4, 5, 29, 33, 43–48	No connect

DEFINITION OF SPECIFICATIONS

Analog Bandwidth The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low frequency value.

Aperture Delay The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs.

Aperture Uncertainty (Jitter) The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine wave clock results in a 50% duty cycle.

Maximum Conversion Rate The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL) An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSB.

Integral Nonlinearity (INL) The INL is the deviation of the ADCs transfer function from a best fit line determined by a least squares curve fit of that transfer function. The INL at each analog input value is the difference between the actual transfer function and this best fit line, measured in units of LSB.

Gain Error The gain error is the deviation of the ADCs actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range.

Offset Error Offset error is the deviation of output code from mid-code when both inputs are tied to common-mode.

Temperature Drift Temperature drift (with respect to gain error and offset error) specifies the change from the value at the nominal temperature to the value at T_{MIN} or T_{MAX}. It is computed as the maximum variation the parameters over the whole temperature range divided by T_{MIN}– T_{MAX}.

Signal-to-Noise Ratio (SNR) SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and the first five harmonics.

(1)

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Signal-to-Noise and Distortion (SINAD) SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

(2)

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Effective Resolution Bandwidth The highest input frequency where the SNR (dB) is dropped by 3 dB for a full-scale input amplitude.

Total Harmonic Distortion (THD) THD is the ratio of the power of the fundamental (P_S) to the power of the first five harmonics (P_D).

PRODUCT PREVIEW

DEFINITION OF SPECIFICATIONS (continued)

(3)

THD is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion IMD3 is the ratio of the power of the fundamental (at frequencies f_1, f_2) to the power of the worst spectral component at either frequency $2f_1 - f_2$ or $2f_2 - f_1$). IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

TYPICAL CHARACTERISTICS

T_A =25°C, AV_{DD} = 5 V, DRV_{DD} = 3.3 V, differential input amplitude = -1 dBFS, sampling rate = 250 MSPS, $3V_{PP}$ sinusoidal clock, 50% duty cycle, unless otherwise noted

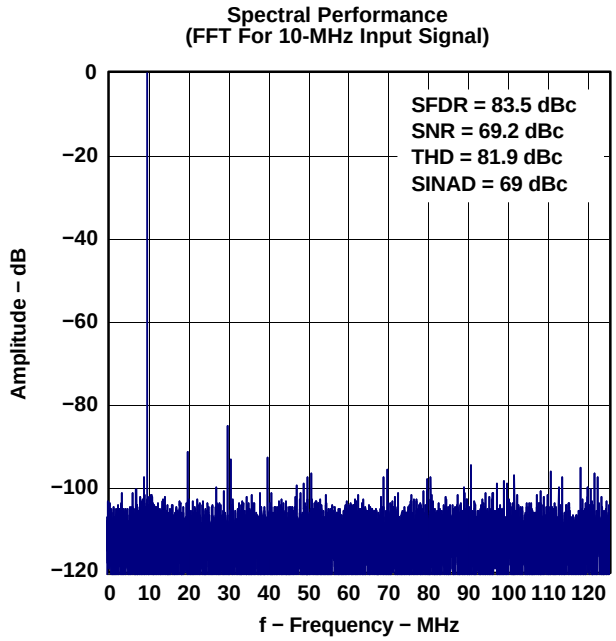


Figure 2.

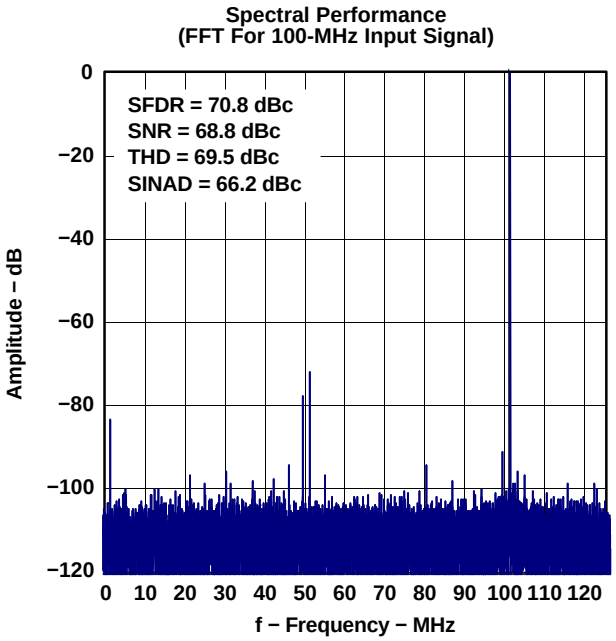


Figure 3.

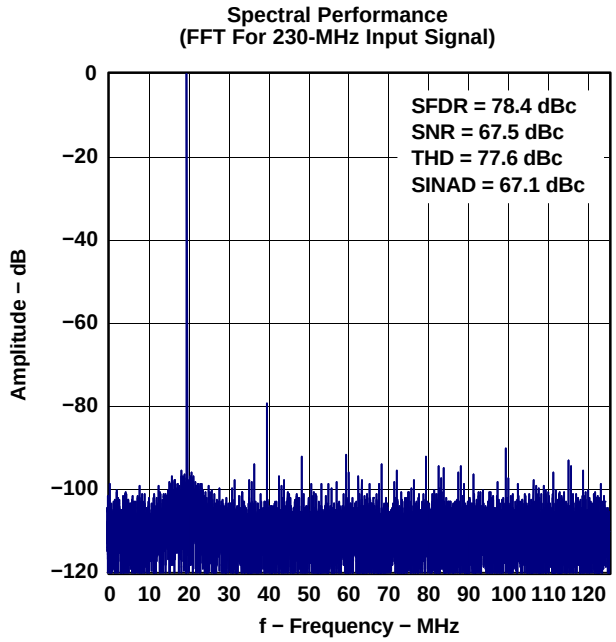


Figure 4.

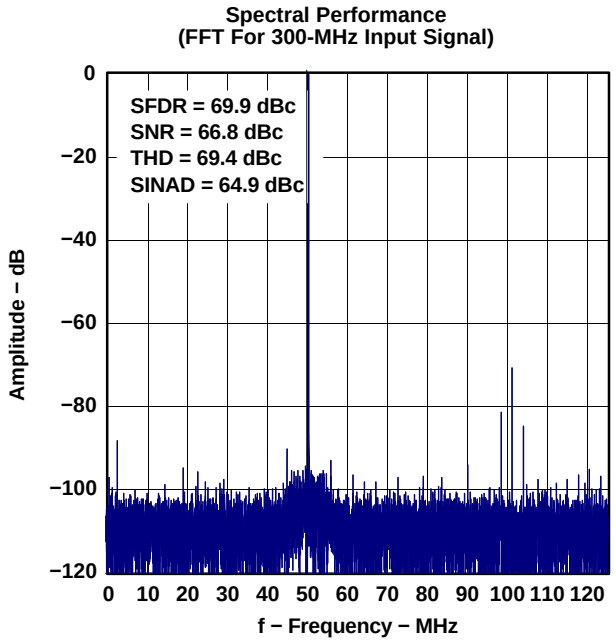


Figure 5.

PRODUCT PREVIEW

APPLICATION INFORMATION

Theory of Operation

The ADS5444 is a 13 bit, 250 MSPS, monolithic pipeline analog to digital converter. Its bipolar analog core operates from a 5 V supply, while the output uses a 3.3 V supply to provide LVDS compatible outputs. The conversion process is initiated by the rising edge of the external input clock. At that instant, the differential input signal is captured by the input track and hold (T&H) and the input sample is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. Both the rising and the falling clock edges are used to propagate the sample through the pipeline every half clock cycle. This process results in a data latency of four clock cycles, after which the output data is available as a 13 bit parallel word, coded in binary two's complement format.

Input Configuration

The analog input for the ADS5444 consists of an analog differential buffer followed by a bipolar track-and-hold. The analog buffer isolates the source driving the input of the ADC from any internal switching. The input common mode is set internally through a 500 Ω resistor connected from 2.4 V to each of the inputs. This results in a differential input impedance of 1 kΩ.

For a full-scale differential input, each of the differential lines of the input signal (pins 16 and 17) swings symmetrically between 2.4 +0.55 V and 2.4 -0.55 V. This means that each input has a maximum signal swing of 1.1 V_{PP} for a total differential input signal swing of 2.2 V_{PP}. The maximum swing is determined by the internal reference voltage generator eliminating the need for any external circuitry for this purpose.

The ADS5444 obtains optimum performance when the analog inputs are driven differentially. The circuit in Figure 6 shows one possible configuration using an RF transformer with termination either on the primary or on the secondary of the transformer. If voltage gain is required, a step up transformer can be used. For gains that would require an impractical transformer turn ratio, a single-ended amplifier driving the transformer is shown in Figure 7).

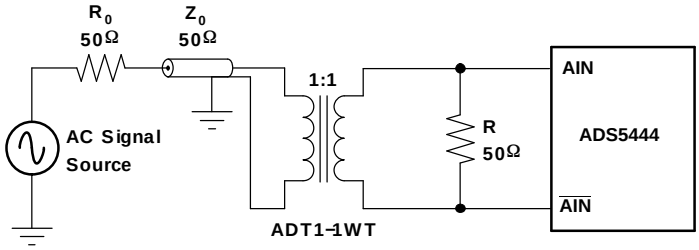


Figure 6. Converting a Single-Ended Input to a Differential Signal Using RF Transformers

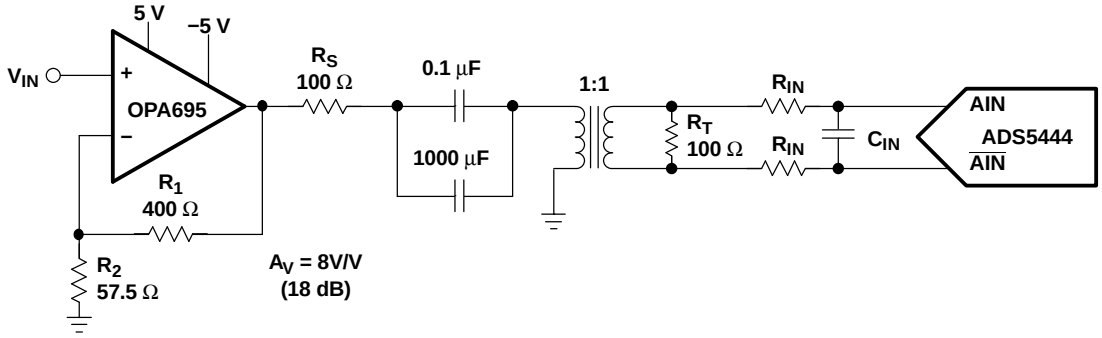


Figure 7. Using the OPA695 With the ADS5444

Besides the OPA695, Texas Instruments offers a wide selection of single-ended operational amplifiers (including

Application Information (continued)

the THS3201, THS3202 and OPA847) that can be selected depending on the application. An RF gain block amplifier, such as Texas Instrument's THS9001, can also be used with an RF transformer for high input frequency applications. For applications requiring dc-coupling with the signal source, a differential input/differential output amplifier like the THS4509 (see Figure 8) is a good solution as it minimizes board space and reduces the number of components.

In this configuration, the THS4509 amplifier circuit provides 10 dB of gain, converts the single-ended input to differential, and sets the proper input common-mode voltage to the ADS5444.

The 225 Ω resistors and 2.7 pF capacitor between the THS4509 outputs and ADS5444 inputs (along with the input capacitance of the ADC) limit the bandwidth of the signal to about 100 MHz (-3 dB).

Input termination is accomplished via the 69.8 Ω resistor and 0.22 µF capacitor to ground in conjunction with the input impedance of the amplifier circuit. A 0.22 µF capacitor and 49.9 Ω resistor is inserted to ground across the 69.8 Ω resistor and 0.22 µF capacitor on the alternate input to balance the circuit.

Gain is a function of the source impedance, termination, and 348 Ω feedback resistor. See the THS4509 data sheet for further component values to set proper 50 Ω termination for other common gains.

Since the ADS5444 recommended input common-mode voltage is +2.4 V, the THS4509 is operated from a single power supply input with V_{S+} = +5 V and V_{S-} = 0 V (ground). This maintains maximum headroom on the internal transistors of the THS4509.

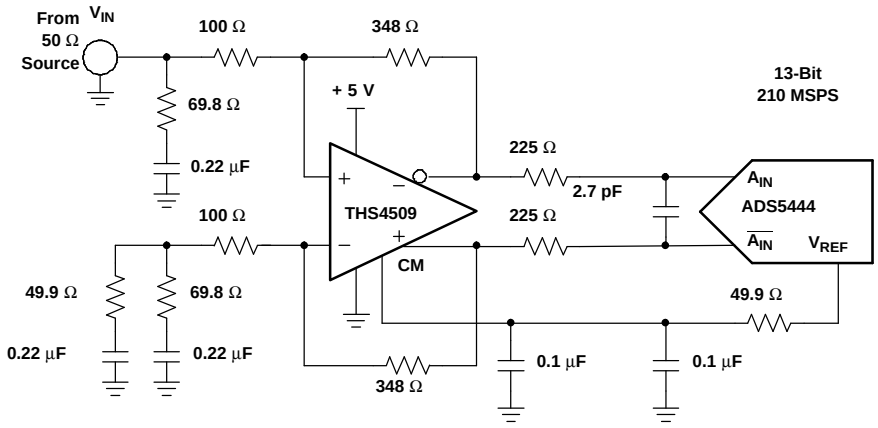


Figure 8. Using the THS4509 With the ADS5444

Clock Inputs

The ADS5444 clock input can be driven with either a differential or a single-ended clock input, with little or no difference in performance between the two configurations. In low input frequency applications, where jitter may not be a big concern, the use of a single-ended clock (see Figure 9) could save some cost and board space without any trade-off in performance. When driven in this configuration, it is best to connect CLK to ground with a 0.01 µF capacitor, while CLK is ac-coupled with a 0.01 µF capacitor to the clock source, as shown in Figure 9.

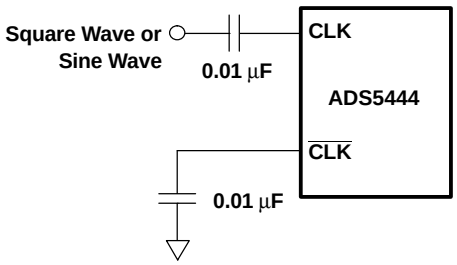


Figure 9. Single-Ended Clock

PRODUCT PREVIEW

Application Information (continued)

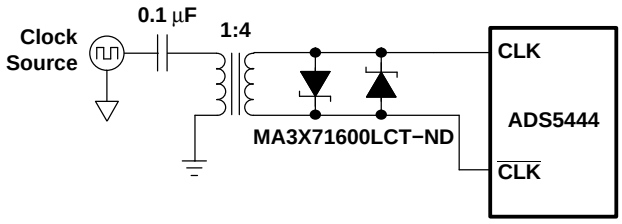


Figure 10. Differential Clock

Nevertheless, for jitter sensitive applications, the use of a differential clock has some advantages (as with any other ADCs). The first advantage is that it allows for common-mode noise rejection at the PCB level.

A differential clock also allows for the use of bigger clock amplitudes without exceeding the absolute maximum ratings. In the case of a sinusoidal clock, this results in higher slew rates and reduces the impact of clock noise on jitter. See Clocking High Speed Data Converters (SLYT075) for more detail.

Figure 10 shows this approach. The back-to-back Schottky diodes can be added to limit the clock amplitude in cases where this would exceed the absolute maximum ratings, even when using a differential clock.

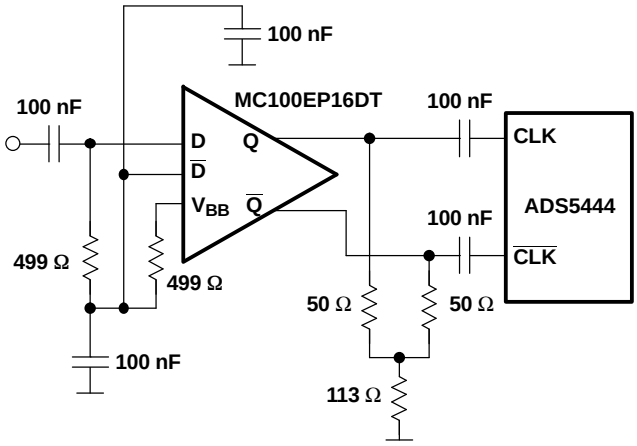


Figure 11. Differential Clock Using PECL Logic

Another possibility is the use of a logic based clock, such as PECL. In this case, the slew rate of the edges will most likely be much higher than the one obtained for the same clock amplitude based on a sinusoidal clock. This solution would minimize the effect of the slope dependent ADC jitter. Using logic gates to square a sinusoidal clock may not produce the best results as logic gates may not have been optimized to act as comparators, adding too much jitter while squaring the inputs.

The common-mode voltage of the clock inputs is set internally to 2.4 V using 1 kΩ resistors. It is recommended to use an ac coupling, but if for any reason, this scheme is not possible, due to, for instance, asynchronous clocking, the ADS5444 presents a good tolerance to clock common-mode variation.

Additionally, the internal ADC core uses both edges of the clock for the conversion process. Ideally, a 50% duty cycle clock signal should be provided.

Digital Outputs

The ADC provides 13 data outputs (D12 to D0, with D12 being the MSB and D0 the LSB), a data-ready signal (DRY), and an over-range indicator (OVR) that equals a logic high when the output reaches the full-scale limits. The output format is binary two's complement.

The ADS5444 digital outputs are LVDS compatible.

Application Information (continued)

Power Supplies

The use of low noise power supplies with adequate decoupling is recommended. Linear supplies are the preferred choice versus switched ones, which tend to generate more noise components that can be coupled to the ADS5444.

The ADS5444 uses two power supplies. For the analog portion of the design, a 5-V AVDD is used, while for the digital outputs supply (DRVDD) we recommend the use of 3.3 V. All the ground pins are marked as GND, although AGND pins and DRGND pins are not tied together inside the package.

Layout Information

The evaluation board represents a good guideline of how to layout the board to obtain the maximum performance out of the ADS5444. General design rules as the use of multilayer boards, single ground plane for ADC ground connections and local decoupling ceramic chip capacitors should be applied. The input traces should be isolated from any external source of interference or noise, including the digital outputs as well as the clock traces. The clock signal traces should also be isolated from other signals, especially in applications where low jitter is required as high IF sampling.

Besides performance oriented rules, special care has to be taken when considering the heat dissipation out of the device. The thermal heat sink should be soldered to the board as described in the *PowerPad Package* section.

PowerPAD PACKAGE

The PowerPAD package is a thermally enhanced standard size IC package designed to eliminate the use of bulky heatsinks and slugs traditionally used in thermal packages. This package can be easily mounted using standard printed circuit board (PCB) assembly techniques, and can be removed and replaced using standard repair procedures.

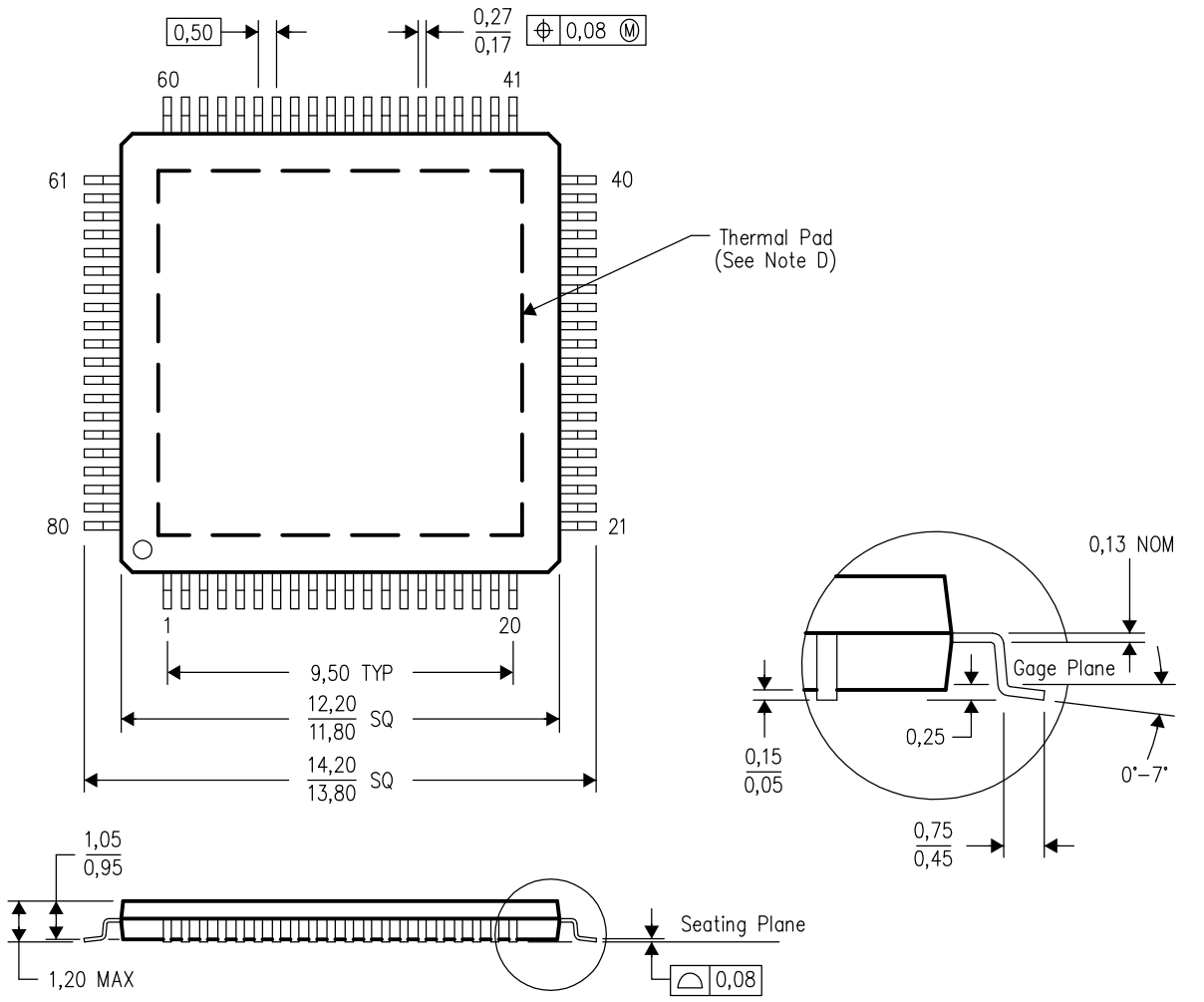
The PowerPAD package is designed so that the leadframe die pad (or thermal pad) is exposed on the bottom of the IC. This provides an extremely low thermal resistance path between the die and the exterior of the package. The thermal pad on the bottom of the IC can then be soldered directly to the printed circuit board (PCB), using the PCB as a heatsink.

Assembly Process

1. Prepare the PCB top-side etch pattern including etch for the leads as well as the thermal pad as illustrated in the Mechanical Data section.
2. Place a 6-by-6 array of thermal vias in the thermal pad area. These holes should be 13 mils in diameter. The small size prevents wicking of the solder through the holes.
3. It is recommended to place a small number of 25 mil diameter holes under the package, but outside the thermal pad area to provide an additional heat path.
4. Connect all holes (both those inside and outside the thermal pad area) to an internal copper plane (such as a ground plane).
5. Do not use the typical web or spoke via connection pattern when connecting the thermal vias to the ground plane. The spoke pattern increases the thermal resistance to the ground plane.
6. The top-side solder mask should leave exposed the terminals of the package and the thermal pad area.
7. Cover the entire bottom side of the PowerPAD vias to prevent solder wicking.
8. Apply solder paste to the exposed thermal pad area and all of the package terminals.

For more detailed information regarding the PowerPAD package and its thermal properties, see either the SLMA004 Application Brief *PowerPAD Made Easy* or the SLMA002 Technical Brief *PowerPAD Thermally Enhanced Package*.

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265