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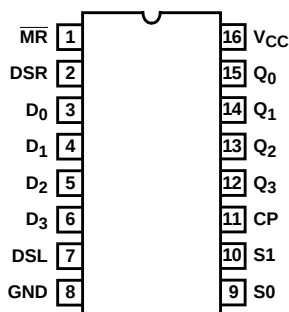
## High-Speed CMOS Logic 4-Bit Bidirectional Universal Shift Register

### Features

- Four Operating Modes
  - Shift Right, Shift Left, Hold and Reset
- Synchronous Parallel or Serial Operation
- Typical  $f_{MAX} = 60\text{MHz}$  at  $V_{CC} = 5\text{V}$ ,  $C_L = 15\text{pF}$ ,  $T_A = 25^\circ\text{C}$
- Asynchronous Master Reset
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . .  $-55^\circ\text{C}$  to  $125^\circ\text{C}$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5\text{V}$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8\text{V}$  (Max),  $V_{IH} = 2\text{V}$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu\text{A}$  at  $V_{OL}$ ,  $V_{OH}$

### Pinout

CD54HC194 (CERDIP)  
CD74HC194 (PDIP, SOIC, SOP, TSSOP)  
CD74HCT194 (PDIP)  
TOP VIEW



### Description

The 'HC194 and CD74HCT194 are 4-bit shift registers with Asynchronous Master Reset ( $\overline{MR}$ ). In the parallel mode ( $S_0$  and  $S_1$  are high), data is loaded into the associated flip-flop and appears at the output after the positive transition of the clock input (CP). During parallel loading serial data flow is inhibited. Shift left and shift right are accomplished synchronously on the positive clock edge with serial data entered at the shift left (DSL) serial input for the shift right mode, and at the shift right (DSR) serial input for the shift left mode. Clearing the register is accomplished by a Low applied to the Master Reset ( $\overline{MR}$ ) pin.

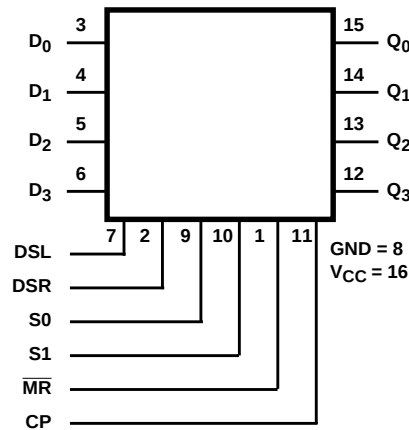
### Ordering Information

| PART NUMBER  | TEMP. RANGE<br>( $^\circ\text{C}$ ) | PACKAGE      |
|--------------|-------------------------------------|--------------|
| CD54HC194F3A | -55 to 125                          | 16 Ld CERDIP |
| CD74HC194E   | -55 to 125                          | 16 Ld PDIP   |
| CD74HC194M   | -55 to 125                          | 16 Ld SOIC   |
| CD74HC194MT  | -55 to 125                          | 16 Ld SOIC   |
| CD74HC194M96 | -55 to 125                          | 16 Ld SOIC   |
| CD74HC194NSR | -55 to 125                          | 16 Ld SOP    |
| CD74HC194PW  | -55 to 125                          | 16 Ld TSSOP  |
| CD74HC194PWR | -55 to 125                          | 16 Ld TSSOP  |
| CD74HC194PWT | -55 to 125                          | 16 Ld TSSOP  |
| CD74HCT194E  | -55 to 125                          | 16 Ld PDIP   |

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

# CD54HC194, CD74HC194, CD74HCT194

## Functional Diagram



TRUTH TABLE

| OPERATING MODE    | INPUTS |                        |            |            |     |     |       | OUTPUT |       |       |       |
|-------------------|--------|------------------------|------------|------------|-----|-----|-------|--------|-------|-------|-------|
|                   | CP     | $\overline{\text{MR}}$ | S1         | S0         | DSR | DSL | $D_n$ | $Q_0$  | $Q_1$ | $Q_2$ | $Q_3$ |
| Reset (Clear)     | X      | L                      | X          | X          | X   | X   | X     | L      | L     | L     | L     |
| Hold (Do Nothing) | X      | H                      | I (Note 1) | I (Note 1) | X   | X   | X     | $q_0$  | $q_1$ | $q_2$ | $q_3$ |
| Shift Left        | ↑      | H                      | h          | I (Note 1) | X   | I   | X     | $q_1$  | $q_2$ | $q_3$ | L     |
|                   | ↑      | H                      | h          | I (Note 1) | X   | h   | X     | $q_1$  | $q_2$ | $q_3$ | H     |
| Shift Right       | ↑      | H                      | I (Note 1) | h          | I   | X   | X     | L      | $q_0$ | $q_1$ | $q_2$ |
|                   | ↑      | H                      | I (Note 1) | h          | h   | X   | X     | H      | $q_0$ | $q_1$ | $q_2$ |
| Parallel Load     | ↑      | H                      | h          | h          | X   | X   | $d_n$ | $d_0$  | $d_1$ | $d_2$ | $d_3$ |

H = High Voltage Level,

h = High Voltage Level One Set-up Time Prior To The Low to High Clock Transition,

L = Low Voltage Level,

I = Low Voltage Level One Set-up Time Prior to the Low to High Clock Transition,

$d_n$  ( $q_n$ ) = Lower Case Letters Indicate the State of the Referenced Input (or output) One Set-up Time Prior to the Low To High Clock Transition,

X = Don't Care,

↑ = Transition from Low to High Level

NOTE:

1. The High-to-Low transition of the S0 and S1 Inputs on the 'HC194 and CD74HCT194 should take place only while CP is High for Conventional Operation.

# CD54HC194, CD74HC194, CD74HCT194

## Absolute Maximum Ratings

DC Supply Voltage,  $V_{CC}$  ..... -0.5V to 7V  
 DC Input Diode Current,  $I_{IK}$   
     For  $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$  .....  $\pm 20mA$   
 DC Output Diode Current,  $I_{OK}$   
     For  $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$  .....  $\pm 20mA$   
 DC Output Source or Sink Current per Output Pin,  $I_O$   
     For  $V_O > -0.5V$  or  $V_O < V_{CC} + 0.5V$  .....  $\pm 25mA$   
 DC  $V_{CC}$  or Ground Current,  $I_{CC}$  or  $I_{GND}$  .....  $\pm 50mA$

## Thermal Information

Package Thermal Impedance,  $\theta_{JA}$  (see Note 2):  
     E (PDIP) Package .....  $67^{\circ}C/W$   
     M (SOIC) Package .....  $73^{\circ}C/W$   
     NS (SOP) Package .....  $64^{\circ}C/W$   
     PW (TSSOP) Package .....  $108^{\circ}C/W$   
 Maximum Junction Temperature .....  $150^{\circ}C$   
 Maximum Storage Temperature Range .....  $-65^{\circ}C$  to  $150^{\circ}C$   
 Maximum Lead Temperature (Soldering 10s) .....  $300^{\circ}C$   
     (SOIC - Lead Tips Only)

## Operating Conditions

Temperature Range ( $T_A$ ) .....  $-55^{\circ}C$  to  $125^{\circ}C$   
 Supply Voltage Range,  $V_{CC}$   
     HC Types ..... 2V to 6V  
     HCT Types ..... 4.5V to 5.5V  
 DC Input or Output Voltage,  $V_I$ ,  $V_O$  ..... 0V to  $V_{CC}$   
 Input Rise and Fall Time  
     2V ..... 1000ns (Max)  
     4.5V ..... 500ns (Max)  
     6V ..... 400ns (Max)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

### NOTE:

- The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

| PARAMETER                               | SYMBOL          | TEST CONDITIONS                       |                     | V <sub>CC</sub> (V) | 25°C |     |      | -40°C TO 85°C |      | -55°C TO 125°C |      | UNITS |
|-----------------------------------------|-----------------|---------------------------------------|---------------------|---------------------|------|-----|------|---------------|------|----------------|------|-------|
|                                         |                 | V <sub>I</sub> (V)                    | I <sub>O</sub> (mA) |                     | MIN  | TYP | MAX  | MIN           | MAX  | MIN            | MAX  |       |
| HC TYPES                                |                 |                                       |                     |                     |      |     |      |               |      |                |      |       |
| High Level Input Voltage                | V <sub>IH</sub> | -                                     | -                   | 2                   | 1.5  | -   | -    | 1.5           | -    | 1.5            | -    | V     |
|                                         |                 |                                       |                     | 4.5                 | 3.15 | -   | -    | 3.15          | -    | 3.15           | -    | V     |
|                                         |                 |                                       |                     | 6                   | 4.2  | -   | -    | 4.2           | -    | 4.2            | -    | V     |
| Low Level Input Voltage                 | V <sub>IL</sub> | -                                     | -                   | 2                   | -    | -   | 0.5  | -             | 0.5  | -              | 0.5  | V     |
|                                         |                 |                                       |                     | 4.5                 | -    | -   | 1.35 | -             | 1.35 | -              | 1.35 | V     |
|                                         |                 |                                       |                     | 6                   | -    | -   | 1.8  | -             | 1.8  | -              | 1.8  | V     |
| High Level Output Voltage<br>CMOS Loads | V <sub>OH</sub> | V <sub>IH</sub> or<br>V <sub>IL</sub> | -0.02               | 2                   | 1.9  | -   | -    | 1.9           | -    | 1.9            | -    | V     |
|                                         |                 |                                       | -0.02               | 4.5                 | 4.4  | -   | -    | 4.4           | -    | 4.4            | -    | V     |
|                                         |                 |                                       | -0.02               | 6                   | 5.9  | -   | -    | 5.9           | -    | 5.9            | -    | V     |
| High Level Output Voltage<br>TTL Loads  | V <sub>OH</sub> | V <sub>IH</sub> or<br>V <sub>IL</sub> | -4                  | 4.5                 | 3.98 | -   | -    | 3.84          | -    | 3.7            | -    | V     |
|                                         |                 |                                       | -5.2                | 6                   | 5.48 | -   | -    | 5.34          | -    | 5.2            | -    | V     |
| Low Level Output Voltage<br>CMOS Loads  | V <sub>OL</sub> | V <sub>IH</sub> or<br>V <sub>IL</sub> | 0.02                | 2                   | -    | -   | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                       | 0.02                | 4.5                 | -    | -   | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                       | 0.02                | 6                   | -    | -   | 0.1  | -             | 0.1  | -              | 0.1  | V     |
| Low Level Output Voltage<br>TTL Loads   | V <sub>OL</sub> | V <sub>IH</sub> or<br>V <sub>IL</sub> | 4                   | 4.5                 | -    | -   | 0.26 | -             | 0.33 | -              | 0.4  | V     |
|                                         |                 |                                       | 5.2                 | 6                   | -    | -   | 0.26 | -             | 0.33 | -              | 0.4  | V     |

# CD54HC194, CD74HC194, CD74HCT194

## DC Electrical Specifications (Continued)

| PARAMETER                                                      | SYMBOL                   | TEST CONDITIONS      |            | $V_{CC}$ (V) | 25°C |     |           | -40°C TO 85°C |         | -55°C TO 125°C |         | UNITS   |
|----------------------------------------------------------------|--------------------------|----------------------|------------|--------------|------|-----|-----------|---------------|---------|----------------|---------|---------|
|                                                                |                          | $V_I$ (V)            | $I_O$ (mA) |              | MIN  | TYP | MAX       | MIN           | MAX     | MIN            | MAX     |         |
| Input Leakage Current                                          | $I_I$                    | $V_{CC}$ or GND      | -          | 6            | -    | -   | $\pm 0.1$ | -             | $\pm 1$ | -              | $\pm 1$ | $\mu A$ |
| Quiescent Device Current                                       | $I_{CC}$                 | $V_{CC}$ or GND      | 0          | 6            | -    | -   | 8         | -             | 80      | -              | 160     | $\mu A$ |
| <b>HCT TYPES</b>                                               |                          |                      |            |              |      |     |           |               |         |                |         |         |
| High Level Input Voltage                                       | $V_{IH}$                 | -                    | -          | 4.5 to 5.5   | 2    | -   | -         | 2             | -       | 2              | -       | V       |
| Low Level Input Voltage                                        | $V_{IL}$                 | -                    | -          | 4.5 to 5.5   | -    | -   | 0.8       | -             | 0.8     | -              | 0.8     | V       |
| High Level Output Voltage<br>CMOS Loads                        | $V_{OH}$                 | $V_{IH}$ or $V_{IL}$ | -0.02      | 4.5          | 4.4  | -   | -         | 4.4           | -       | 4.4            | -       | V       |
| High Level Output Voltage<br>TTL Loads                         |                          |                      | -4         | 4.5          | 3.98 | -   | -         | 3.84          | -       | 3.7            | -       | V       |
| Low Level Output Voltage<br>CMOS Loads                         | $V_{OL}$                 | $V_{IH}$ or $V_{IL}$ | 0.02       | 4.5          | -    | -   | 0.1       | -             | 0.1     | -              | 0.1     | V       |
| Low Level Output Voltage<br>TTL Loads                          |                          |                      | 4          | 4.5          | -    | -   | 0.26      | -             | 0.33    | -              | 0.4     | V       |
| Input Leakage Current                                          | $I_I$                    | $V_{CC}$ to GND      | 0          | 5.5          | -    | -   | $\pm 0.1$ | -             | $\pm 1$ | -              | $\pm 1$ | $\mu A$ |
| Quiescent Device Current                                       | $I_{CC}$                 | $V_{CC}$ or GND      | 0          | 5.5          | -    | -   | 8         | -             | 80      | -              | 160     | $\mu A$ |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | $\Delta I_{CC}$ (Note 3) | $V_{CC}$ -2.1        | -          | 4.5 to 5.5   | -    | 100 | 360       | -             | 450     | -              | 490     | $\mu A$ |

NOTE:

- For dual-supply systems theoretical worst case ( $V_I = 2.4V$ ,  $V_{CC} = 5.5V$ ) specification is 1.8mA.

## HCT Input Loading Table

| INPUT           | UNIT LOADS |
|-----------------|------------|
| CP              | 0.6        |
| $\overline{MR}$ | 0.55       |
| DSL, DSR, $D_n$ | 0.25       |
| Sn              | 1.10       |

NOTE: Unit Load is  $\Delta I_{CC}$  limit specified in DC Electrical Specifications table, e.g. 360 $\mu A$  max at 25°C.

# CD54HC194, CD74HC194, CD74HCT194

## Prerequisite For Switching Function

| PARAMETER                                   | SYMBOL           | TEST<br>CONDITIONS | V <sub>CC</sub> (V) | 25°C |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|---------------------------------------------|------------------|--------------------|---------------------|------|-----|---------------|-----|----------------|-----|-------|
|                                             |                  |                    |                     | MIN  | MAX | MIN           | MAX | MIN            | MAX |       |
| HC TYPES                                    |                  |                    |                     |      |     |               |     |                |     |       |
| Max. Clock Frequency<br>(Figure 1)          | f <sub>MAX</sub> | -                  | 2                   | 6    | -   | 5             | -   | 4              | -   | MHz   |
|                                             |                  |                    | 4.5                 | 30   | -   | 24            | -   | 20             | -   | MHz   |
|                                             |                  |                    | 6                   | 35   | -   | 28            | -   | 23             | -   | MHz   |
| MR Pulse Width<br>(Figure 2)                | t <sub>W</sub>   | -                  | 2                   | 80   | -   | 100           | -   | 120            | -   | ns    |
|                                             |                  |                    | 4.5                 | 16   | -   | 20            | -   | 24             | -   | ns    |
|                                             |                  |                    | 6                   | 14   | -   | 17            | -   | 20             | -   | ns    |
| Clock Pulse Width<br>(Figure 1)             | t <sub>W</sub>   | -                  | 2                   | 80   | -   | 100           | -   | 120            | -   | ns    |
|                                             |                  |                    | 4.5                 | 16   | -   | 20            | -   | 24             | -   | ns    |
|                                             |                  |                    | 6                   | 14   | -   | 17            | -   | 20             | -   | ns    |
| Set-up Time<br>Data to Clock (Figure 3)     | t <sub>SU</sub>  | -                  | 2                   | 70   | -   | 90            | -   | 105            | -   | ns    |
|                                             |                  |                    | 4.5                 | 14   | -   | 18            | -   | 21             | -   | ns    |
|                                             |                  |                    | 6                   | 12   | -   | 15            | -   | 19             | -   | ns    |
| Removal Time,<br>MR to Clock (Figure 2)     | t <sub>REM</sub> | -                  | 2                   | 60   | -   | 75            | -   | 90             | -   | ns    |
|                                             |                  |                    | 4.5                 | 12   | -   | 15            | -   | 18             | -   | ns    |
|                                             |                  |                    | 6                   | 10   | -   | 13            | -   | 15             | -   | ns    |
| Set-Up Time<br>S1, S0 to Clock (Figure 4)   | t <sub>SU</sub>  | -                  | 2                   | 80   | -   | 100           | -   | 120            | -   | ns    |
|                                             |                  |                    | 4.5                 | 16   | -   | 20            | -   | 24             | -   | ns    |
|                                             |                  |                    | 6                   | 14   | -   | 17            | -   | 20             | -   | ns    |
| Set-up Time<br>DSL, DSR to Clock (Figure 4) | t <sub>SU</sub>  | -                  | 2                   | 70   | -   | 90            | -   | 105            | -   | ns    |
|                                             |                  |                    | 4.5                 | 14   | -   | 18            | -   | 21             | -   | ns    |
|                                             |                  |                    | 6                   | 12   | -   | 15            | -   | 18             | -   | ns    |
| Hold Time<br>S1, S0 to Clock (Figure 4)     | t <sub>H</sub>   | -                  | 2                   | 0    | -   | 0             | -   | 0              | -   | ns    |
|                                             |                  |                    | 4.5                 | 0    | -   | 0             | -   | 0              | -   | ns    |
|                                             |                  |                    | 6                   | 0    | -   | 0             | -   | 0              | -   | ns    |
| Hold Time<br>Data to Clock (Figure 3)       | t <sub>H</sub>   | -                  | 2                   | 0    | -   | 0             | -   | 0              | -   | ns    |
|                                             |                  |                    | 4.5                 | 0    | -   | 0             | -   | 0              | -   | ns    |
|                                             |                  |                    | 6                   | 0    | -   | 0             | -   | 0              | -   | ns    |
| HCT TYPES                                   |                  |                    |                     |      |     |               |     |                |     |       |
| Max. Clock Frequency (Figure 1)             | f <sub>MAX</sub> | -                  | 4.5                 | 27   | -   | 22            | -   | 18             | -   | MHz   |
| MR Pulse Width (Figure 2)                   | t <sub>W</sub>   | -                  | 4.5                 | 16   | -   | 20            | -   | 24             | -   | ns    |
| Clock Pulse Width (Figure 1)                | t <sub>W</sub>   | -                  | 4.5                 | 16   | -   | 20            | -   | 24             | -   | ns    |
| Set-up Time, Data to Clock<br>(Figure 3)    | t <sub>SU</sub>  | -                  | 4.5                 | 14   | -   | 18            | -   | 21             | -   | ns    |
| Removal Time MR to Clock<br>(Figure 2)      | t <sub>REM</sub> | -                  | 4.5                 | 12   | -   | 15            | -   | 18             | -   | ns    |

# Prerequisite For Switching Function (Continued)

| PARAMETER                                   | SYMBOL          | TEST CONDITIONS | V <sub>CC</sub> (V) | 25°C |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|---------------------------------------------|-----------------|-----------------|---------------------|------|-----|---------------|-----|----------------|-----|-------|
|                                             |                 |                 |                     | MIN  | MAX | MIN           | MAX | MIN            | MAX |       |
| Set-up Time<br>S1, S0 to Clock (Figure 4)   | t <sub>SU</sub> | -               | 4.5                 | 20   | -   | 25            | -   | 30             | -   | ns    |
| Set-up Time<br>DSL, DSR to Clock (Figure 4) | t <sub>SU</sub> | -               | 4.5                 | 14   | -   | 18            | -   | 21             | -   | ns    |
| Hold Time<br>S1, S0 to Clock (Figure 4)     | t <sub>H</sub>  | -               | 4.5                 | 0    | -   | 0             | -   | 0              | -   | ns    |
| Hold Time<br>Data to Clock (Figure 3)       | t <sub>H</sub>  | -               | 4.5                 | 0    | -   | 0             | -   | 0              | -   | ns    |

## Switching Specifications Input t<sub>r</sub>, t<sub>f</sub> = 6ns

| PARAMETER                                     | SYMBOL                              | TEST CONDITIONS       | V <sub>CC</sub> (V) | 25°C |     | -40°C TO 85°C | -55°C TO 125°C | UNITS |
|-----------------------------------------------|-------------------------------------|-----------------------|---------------------|------|-----|---------------|----------------|-------|
|                                               |                                     |                       |                     | TYP  | MAX | MAX           | MAX            |       |
| HC TYPES                                      |                                     |                       |                     |      |     |               |                |       |
| Propagation Delay, Clock to Output (Figure 1) | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | 175 | 220           | 265            | ns    |
|                                               |                                     |                       | 4.5                 | -    | 35  | 44            | 53             | ns    |
|                                               |                                     |                       | 6                   | -    | 30  | 37            | 45             | ns    |
| Propagation Delay, Clock to Q                 | t <sub>PLH</sub> , t <sub>PHL</sub> | -                     | 5                   | 14   | -   | -             | -              | ns    |
| Output Transition Time (Figure 1)             | t <sub>TLH</sub> , t <sub>THL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | 75  | 95            | 110            | ns    |
|                                               |                                     |                       | 4.5                 | -    | 15  | 19            | 22             | ns    |
|                                               |                                     |                       | 6                   | -    | 13  | 16            | 19             | ns    |
| Propagation Delay, MR to Output (Figure 2)    | t <sub>PHL</sub>                    | C <sub>L</sub> = 50pF | 2                   | -    | 140 | 175           | 210            | ns    |
|                                               |                                     |                       | 4.5                 | -    | 28  | 35            | 42             | ns    |
|                                               |                                     |                       | 6                   | -    | 24  | 30            | 36             | ns    |
| Input Capacitance                             | C <sub>IN</sub>                     | -                     | -                   | -    | 10  | 10            | 10             | pF    |
| Maximum Clock Frequency                       | f <sub>MAX</sub>                    | -                     | 5                   | 60   | -   | -             | -              | MHz   |
| Power Dissipation Capacitance (Notes 4, 5)    | C <sub>PD</sub>                     | -                     | 5                   | 55   | -   | -             | -              | pF    |
| HCT TYPES                                     |                                     |                       |                     |      |     |               |                |       |
| Propagation Delay, Clock to Output (Figure 1) | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 4.5                 | -    | 37  | 46            | 56             | ns    |
| Propagation Delay, Clock to Q                 | t <sub>PLH</sub> , t <sub>PHL</sub> | -                     | 5                   | 15   | -   | -             | -              | ns    |
| Output Transition Times (Figure 1)            | t <sub>TLH</sub> , t <sub>THL</sub> | C <sub>L</sub> = 50pF | 4.5                 | -    | 15  | 19            | 22             | ns    |
| Propagation Delay, MR to Output (Figure 2)    | t <sub>PHL</sub>                    | C <sub>L</sub> = 50pF | 4.5                 | -    | 40  | 50            | 60             | ns    |
| Input Capacitance                             | C <sub>IN</sub>                     | -                     | -                   | -    | 10  | 10            | 10             | pF    |
| Maximum Clock Frequency                       | f <sub>MAX</sub>                    | -                     | 5                   | 50   | -   | -             | -              | MHz   |
| Power Dissipation Capacitance (Notes 4, 5)    | C <sub>PD</sub>                     | -                     | 5                   | 60   | -   | -             | -              | pF    |

### NOTES:

- C<sub>PD</sub> is used to determine the dynamic power consumption, per gate.
- $P_D = V_{CC}^2 f_i + \sum (C_L V_{CC}^2)$  where  $f_i$  = Input Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

## Test Circuits and Waveforms

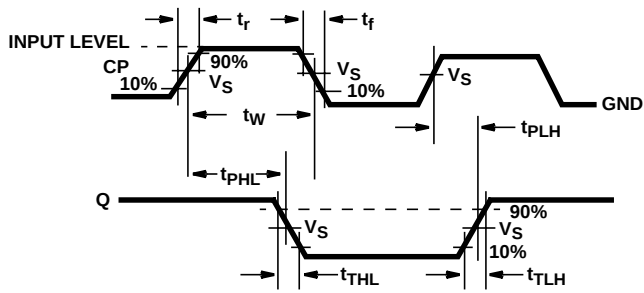


FIGURE 1. CLOCK PREREQUISITE TIMES AND PROPAGATION AND OUTPUT TRANSITION TIMES

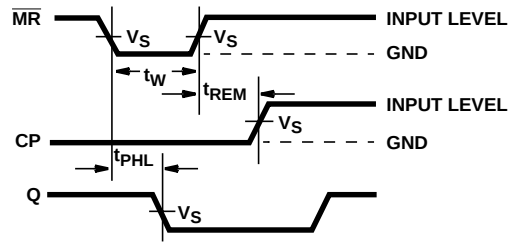


FIGURE 2. MASTER RESET PREREQUISITE TIMES AND PROPAGATION DELAYS

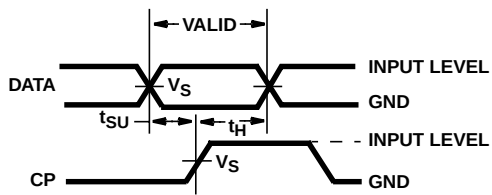


FIGURE 3. DATA PREREQUISITE TIMES

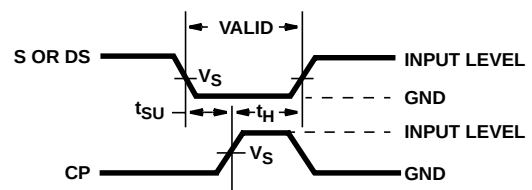


FIGURE 4. PARALLEL LOAD OR SHIFT-LEFT/SHIFT-RIGHT PREREQUISITE TIMES

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



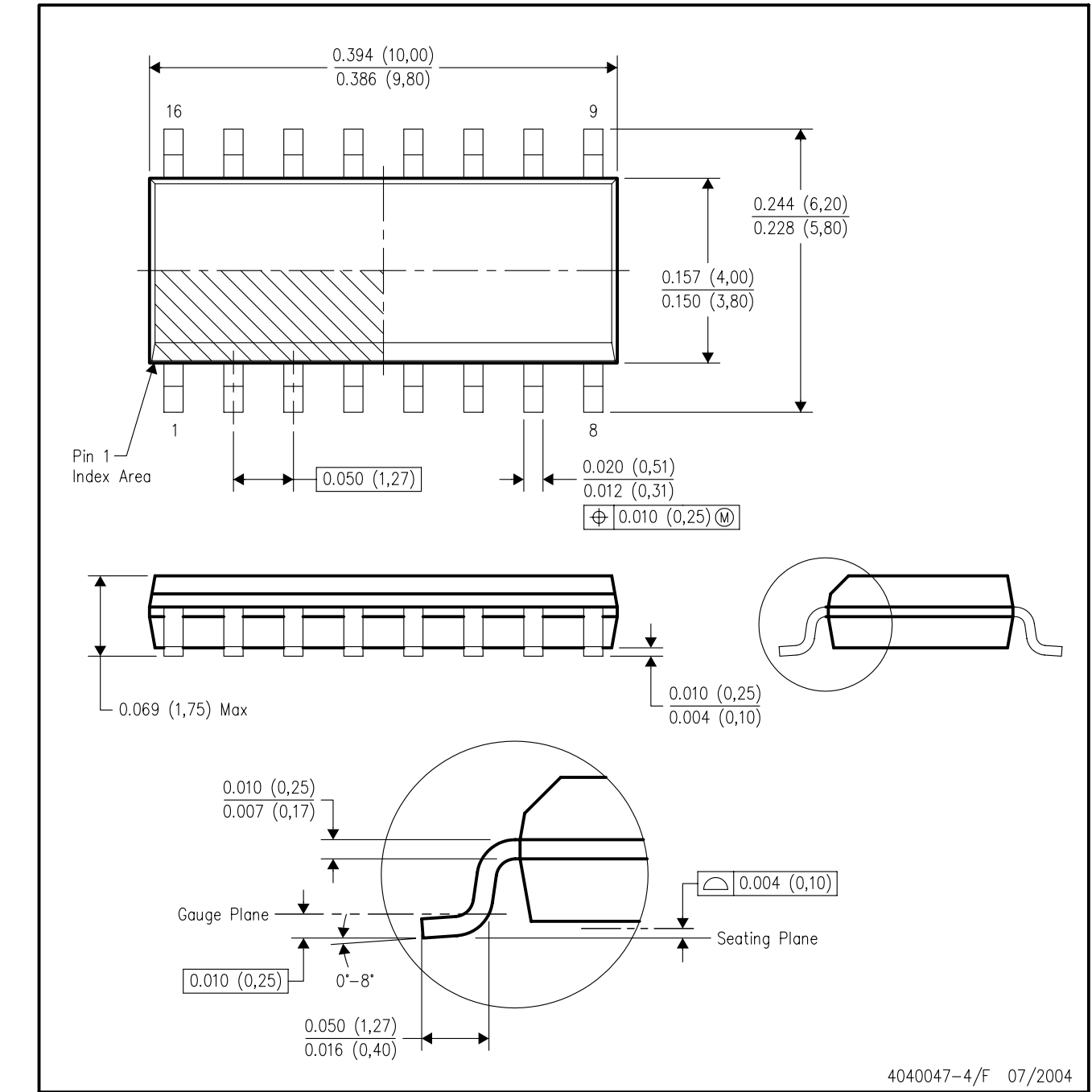
4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

## D (R-PDS0-G16) PLASTIC SMALL-OUTLINE PACKAGE

## D (R-PDS0-G16) PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/F 07/2004

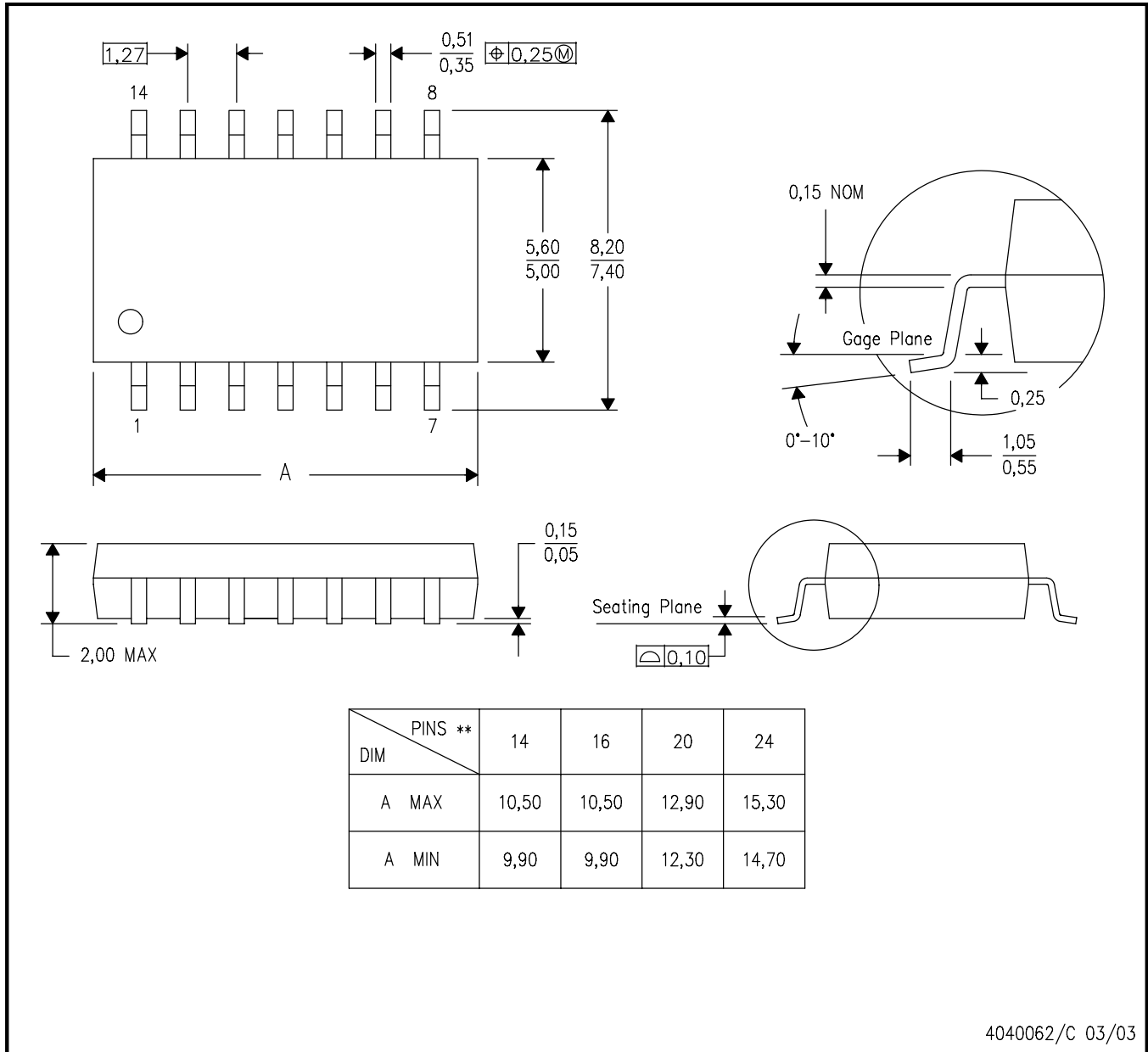
NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
D. Falls within JEDEC MS-012 variation AC.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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