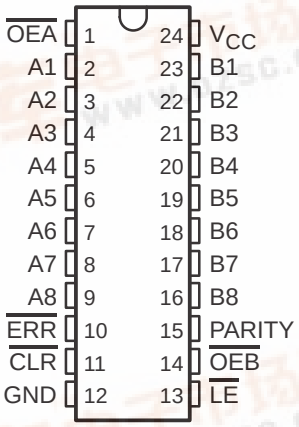
SN54ABT853, SN74ABT853
8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

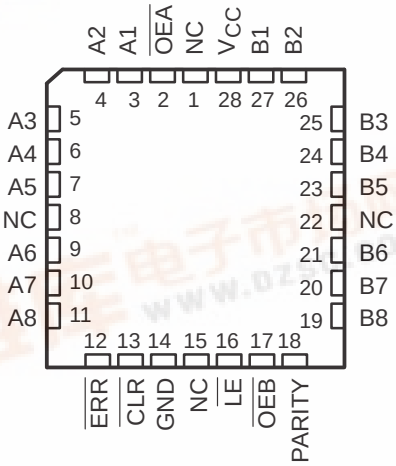
SCBS198F – FEBRUARY 1991 – REVISED OCTOBER 1997

- State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C
- High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})
- High-Impedance State During Power Up and Power Down
- Parity-Error Flag With Parity Generator/Checker
- Latch for Storage of Parity-Error Flag
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Plastic (NT) and Ceramic (JT) DIPs

SN54ABT853 . . . JT OR W PACKAGE
SN74ABT853 . . . DB, DW, NT, OR PW PACKAGE
(TOP VIEW)



SN54ABT853 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The ’ABT853 8-bit to 9-bit parity transceivers are designed for communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the open-collector parity-error ($\overline{ERR}$) output indicates whether or not an error in the B data has occurred. The output-enable ($\overline{OEA}$ and $\overline{OEB}$) inputs can be used to disable the device so that the buses are effectively isolated. The ’ABT853 transceivers provide true data at their outputs.

A 9-bit parity generator/checker generates a parity-odd (PARITY) output and monitors the parity of the I/O ports with the $\overline{ERR}$ flag. The parity-error output can be passed, sampled, stored, or cleared from the latch using the latch-enable ($\overline{LE}$) and clear ($\overline{CLR}$) control inputs. When both $\overline{OEA}$ and $\overline{OEB}$ are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

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description (continued)

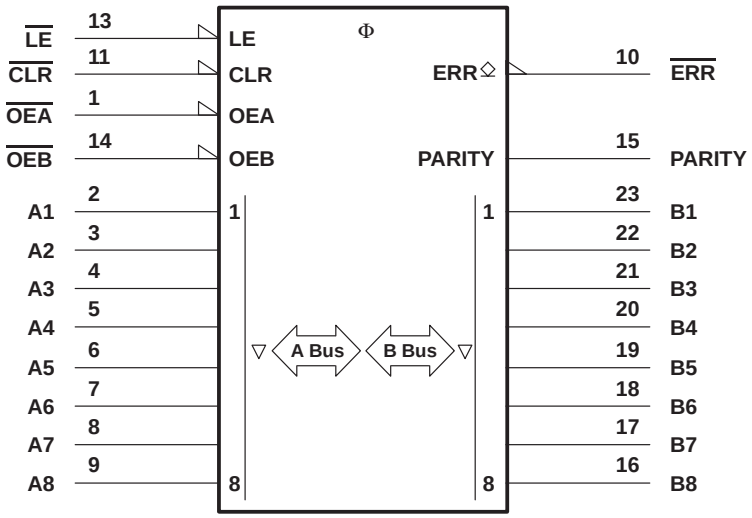
The SN54ABT853 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT853 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS						OUTPUTS AND I/Os				FUNCTION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	LE	Ai Σ OF H	Bi† Σ OF H	A	B	PARITY	$\overline{ERR}$‡	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A data to B bus and generate parity
H	L	X	L	NA	Odd Even	B	NA	NA	H L	B data to A bus and check parity
H	L	H	H	NA	X	X	NA	NA	NC	Store error flag
X	X	L	H	X	X	X	NA	NA	H	Clear error flag register
H	H	H L X X	H H L L	X X L Odd H Even	X	Z	Z	Z	NC H H L	Isolation§ (parity check)
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A data to B bus and generate inverted parity

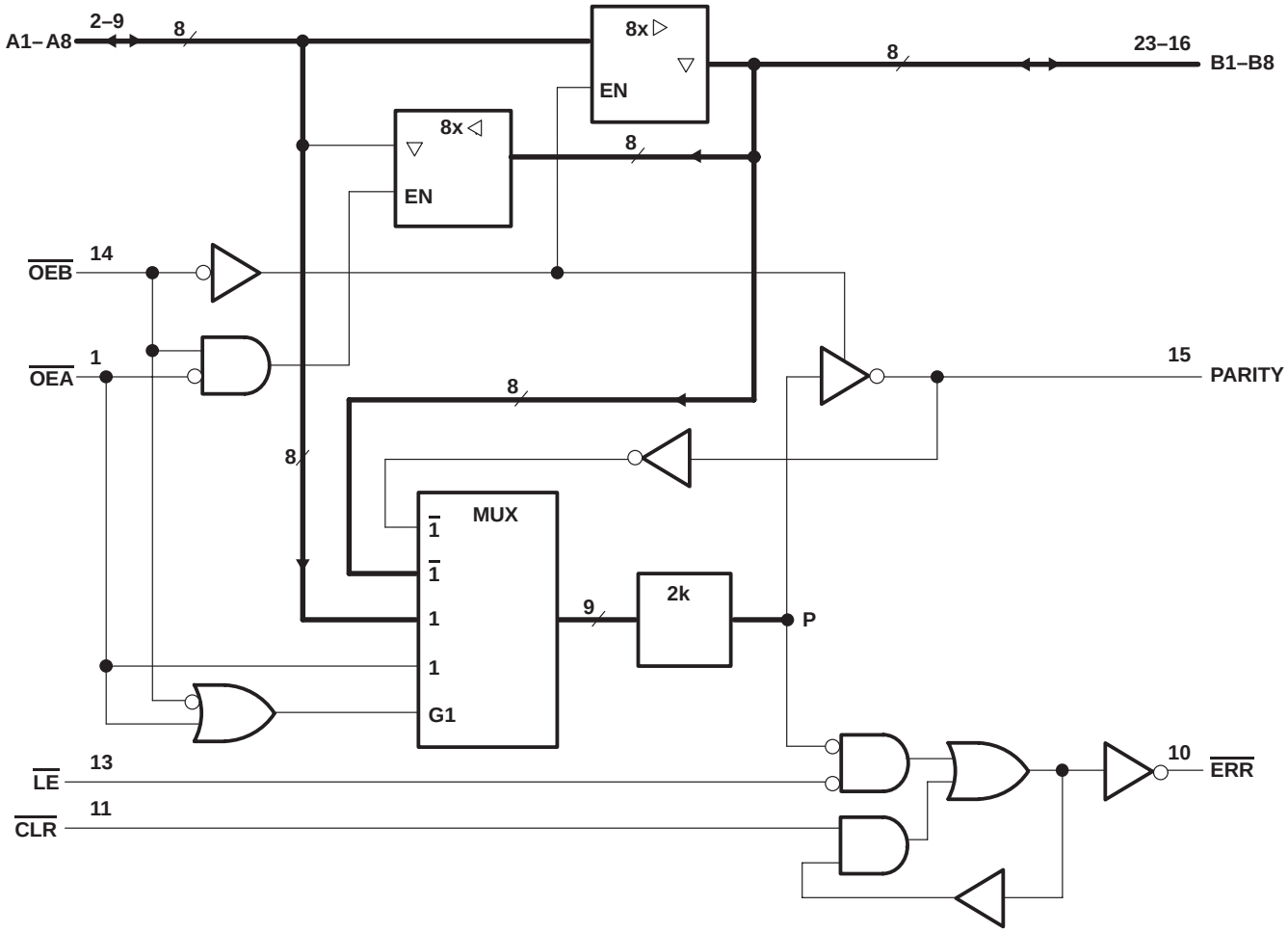
NA = not applicable, NC = no change, X = don't care
† Summation of high-level inputs includes PARITY along with Bi inputs.
‡ Output states shown assume $\overline{ERR}$ was previously high.
§ In this mode, $\overline{ERR}$ (when clocked) shows inverted parity of the A bus.

logic symbol¶



¶ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, NT, PW, and W packages.

logic diagram (positive logic)



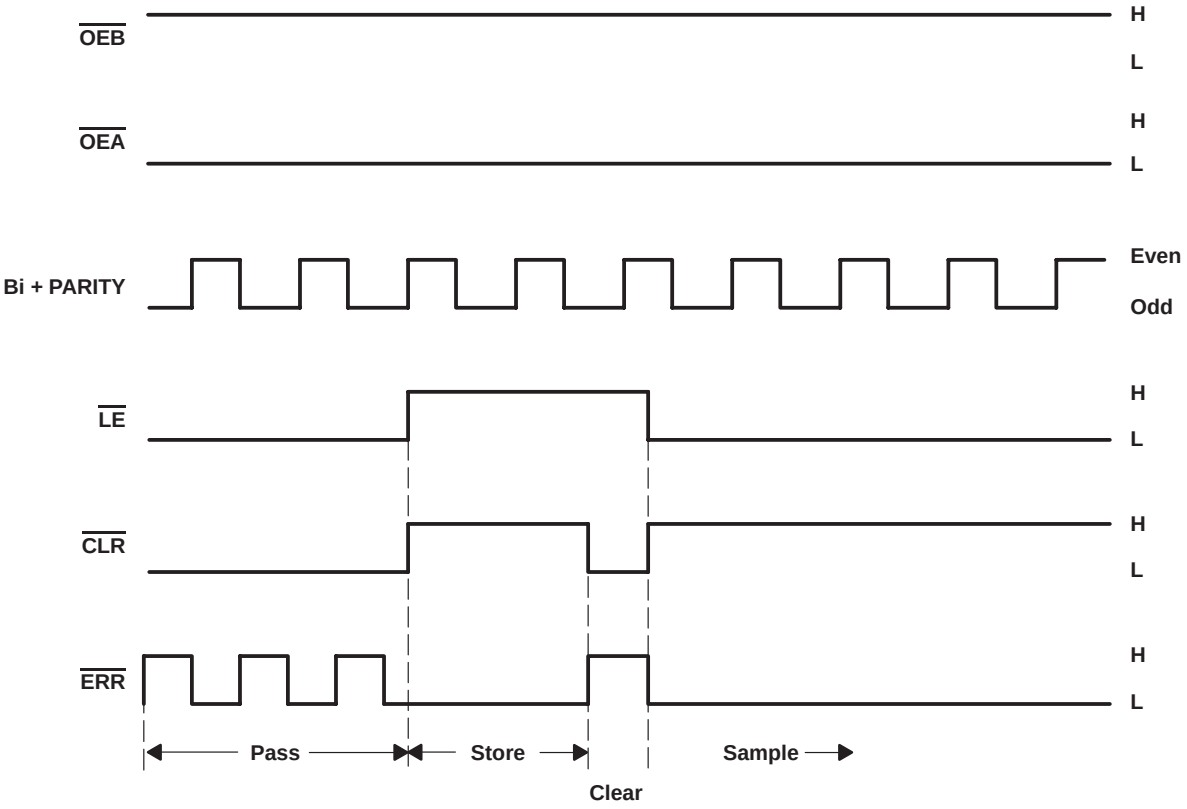
Pin numbers shown are for the DB, DW, JT, NT, PW, and W packages.

ERROR-FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT PRESTATE	OUTPUT $\overline{ERR}$	FUNCTION
$\overline{CLR}$	LE	POINT P	$\overline{ERR}_{N-1}$†		
L	L	L	X	L	Pass
		H		H	
H	L	L	X	L	Sample
		X	L	L	
		H	H	H	
L	H	X	X	H	Clear
H	H	X	L	L	Store
			H	H	

† The state of $\overline{ERR}$ before changes at $\overline{CLR}$, $\overline{LE}$, or point P

error-flag waveforms



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I: Except I/O ports (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT853 . . . . . 96 mA
SN74ABT853 . . . . . 128 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . . –18 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package . . . . . 104°C/W
DW package . . . . . 81°C/W
N package . . . . . 67°C/W
PW package . . . . . 120°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

			SN54ABT853		SN74ABT853		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_{OH}	High-level output voltage	$\overline{ERR}$		5.5		5.5	V
I_{OH}	High-level output current	Except $\overline{ERR}$		–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		μs/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A = 25°C			SN54ABT853		SN74ABT853		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2		–1.2		–1.2	V
V_{OH}	All outputs except $\overline{ERR}$	V_{CC} = 4.5 V,	I_{OH} = –3 mA	2.5			2.5		2.5		V
		V_{CC} = 5 V,	I_{OH} = –3 mA	3			3		3		
		V_{CC} = 4.5 V	I_{OH} = –24 mA	2			2				
			I_{OH} = –32 mA	2*					2		
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 24 mA			0.55		0.55			V
			I_{OL} = 64 mA			0.55*				0.55	
V_{hys}					100						mV
I_{OH}	$\overline{ERR}$	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			50		50		50	µA
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = V_{CC} or GND			±1		±1		±1	µA
	A or B ports					±100		±100		±100	
I_{OZPU}‡		V_{CC} = 0 to 2.1 V, V_O = 0.5 V to 2.7 V, $\overline{OE}$ = X				±50		±50		±50	µA
I_{OZPD}‡		V_{CC} = 2.1 V to 0, V_O = 0.5 V to 2.7 V, $\overline{OE}$ = X				±50		±50		±50	µA
I_{OZH}§		V_{CC} = 5.5 V,	V_O = 2.7 V			10		10		10	µA
I_{OZL}§		V_{CC} = 5.5 V,	V_O = 0.5 V			–10		–10		–10	µA
I_{off}		V_{CC} = 0,	V_I or V_O ≤ 4.5 V			±100				±100	µA
I_{CEX}		V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶		V_{CC} = 5.5 V,	V_O = 2.5 V	–50	–100	–200#	–50	–200#	–50	–200#	mA
I_{CC}	A or B ports	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		1	250		450		250	µA
			Outputs low		24	38		38		38	mA
			Outputs disabled		0.5	250		450		250	µA
ΔI_{CC}‖	Data inputs	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			50		50		50	µA
	Control inputs	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	Control inputs	V_I = 2.5 V or 0.5 V			4.5						pF
C_{io}	A or B ports	V_O = 2.5 V or 0.5 V			10.5						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at V_{CC} = 5 V.
‡ This parameter is characterized, but not production tested.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This data sheet limit can vary among suppliers.
‖ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			V_{CC} = 5 V, T_A = 25°C		SN54ABT853		SN74ABT853		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{LE}$ high or low	3.5		3.5		3.5		ns
		$\overline{CLR}$ low	4		4		4		
t_{su}	Setup time	B or PARITY before $\overline{LE}\downarrow$	9.4†		10.2		9.4†		ns
		$\overline{CLR}$ before $\overline{LE}\downarrow$	2		2		2		
t_h	Hold time	B or PARITY after $\overline{LE}\downarrow$	0		0		0		ns
		$\overline{CLR}$ after $\overline{LE}\downarrow$	3		3		3		

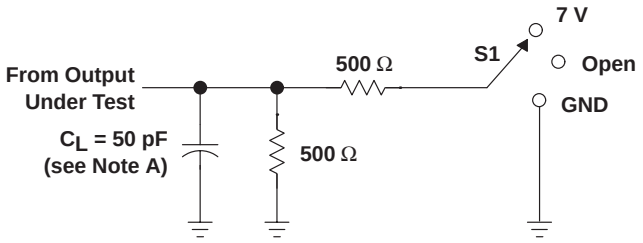
† This data sheet limit can vary among suppliers.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT853		SN74ABT853		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.2		4.8	1.2	6.4	1.2	5.3	ns
t_{PHL}			1		4.8†	1	5.4	1	5.3†	
t_{PLH}	A	PARITY	2.1		9.5	2.1	13.3	2.1	11.2	ns
t_{PHL}			2.5		9.7	2.5	11	2.5	11	
t_{PLH}	$\overline{OE}$	PARITY	1.8		8.5	1.8	13.6	1.8	10.5	ns
t_{PHL}			2.3		8.6	2.3	11.7	2.3	10	
t_{PLH}	$\overline{CLR}$	$\overline{ERR}$	1		5.5	1	6.3	1	6.2	ns
t_{PLH}	$\overline{LE}$	ERR	1.8		5.1	1.8	6.1	1.8	6	ns
t_{PHL}			1†		5.8	1†	6.7	1	6.6	
t_{PLH}	B or PARITY	ERR	2		10.1	2	11.8	2	11.7	ns
t_{PHL}			2.2†		11.5	2.2†	12.9	2.2†	12.8	
t_{PZH}	$\overline{OE}$	A or B or PARITY	1		5.8†	1	8.8	1	6.7†	ns
t_{PZL}			1.5†		5.8	1.5†	9.8	1.5†	6.7	
t_{PHZ}	$\overline{OE}$	A or B or PARITY	1.8†		7.3	1.8†	9.5	1.8†	7.9	ns
t_{PLZ}			2.1†		7.2	2.1†	8.2	2.1†	8.1	

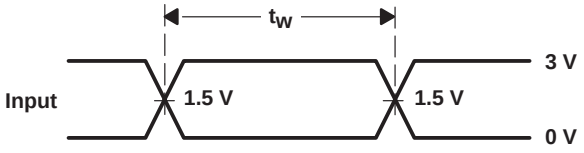
† This data sheet limit can vary among suppliers.

PARAMETER MEASUREMENT INFORMATION

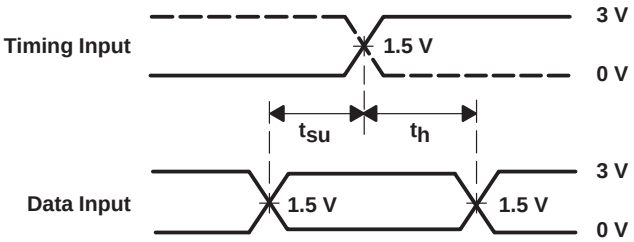


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

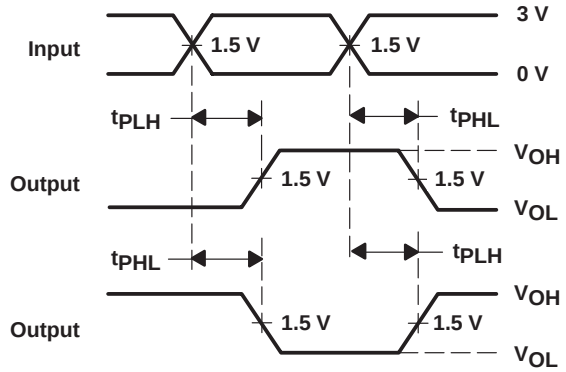
LOAD CIRCUIT



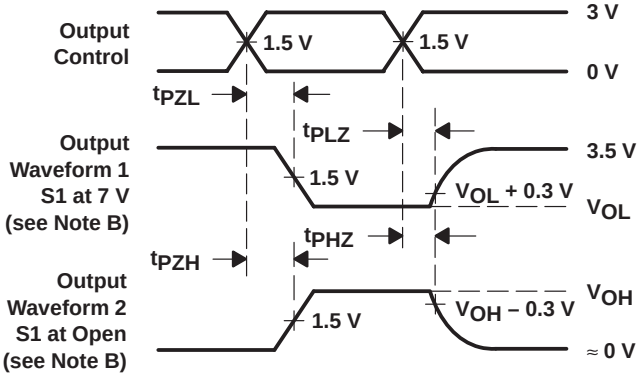
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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