



July 1998

## 54ABT16373

### 16-Bit Transparent Latch with TRI-STATE® Outputs

#### General Description

The ABT16373 contains sixteen non-inverting latches with TRI-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is low, the data that meets the setup time is latched. Data appears on the bus when the Output Enable ( $\overline{OE}$ ) is LOW. When  $\overline{OE}$  is HIGH, the outputs are in high Z state.

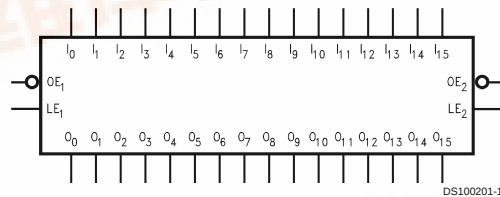
#### Features

- Separate control logic for each byte
- 16-bit version of the ABT373
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Guaranteed latch-up protection
- Standard Microcircuit Drawing (SMD) 5962-9320001

#### Ordering Code:

| Military        | Package Number | Package Description |
|-----------------|----------------|---------------------|
| 54ABT16373W-QML | WA48A          | 48-Lead Cerpack     |

#### Logic Symbol

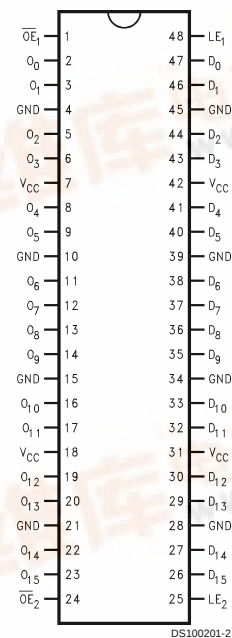


#### Pin Description

| Pin Names         | Description                      |
|-------------------|----------------------------------|
| $\overline{OE}_n$ | Output Enable Input (Active Low) |
| $LE_n$            | Latch Enable Input               |
| $D_0-D_{15}$      | Data Inputs                      |
| $O_0-O_{15}$      | Outputs                          |

#### Connection Diagram

Pin Assignment for Cerpack



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## Functional Description

The ABT16373 contains sixteen D-type latches with TRI-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable ( $LE_n$ ) input is HIGH, data on the  $D_n$  enters the latches. In this condition the latches are transparent, i.e., a latch output will change states each time its D input changes. When  $LE_n$  is LOW, the latches store information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of  $LE_n$ . The TRI-STATE standard outputs are controlled by the Output Enable ( $\overline{OE}_n$ ) input. When  $\overline{OE}_n$  is LOW, the standard outputs are in the 2-state mode. When  $\overline{OE}_n$  is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

## Truth Tables

| Inputs |                   |           | Outputs    |
|--------|-------------------|-----------|------------|
| $LE_1$ | $\overline{OE}_1$ | $D_0-D_7$ | $O_0-O_7$  |
| X      | H                 | X         | Z          |
| H      | L                 | L         | L          |
| H      | L                 | H         | H          |
| L      | L                 | X         | (Previous) |

| Inputs |                   |              | Outputs      |
|--------|-------------------|--------------|--------------|
| $LE_2$ | $\overline{OE}_2$ | $D_8-D_{15}$ | $O_8-O_{15}$ |
| X      | H                 | X            | Z            |
| H      | L                 | L            | L            |
| H      | L                 | H            | H            |
| L      | L                 | X            | (Previous)   |

H = High Voltage Level

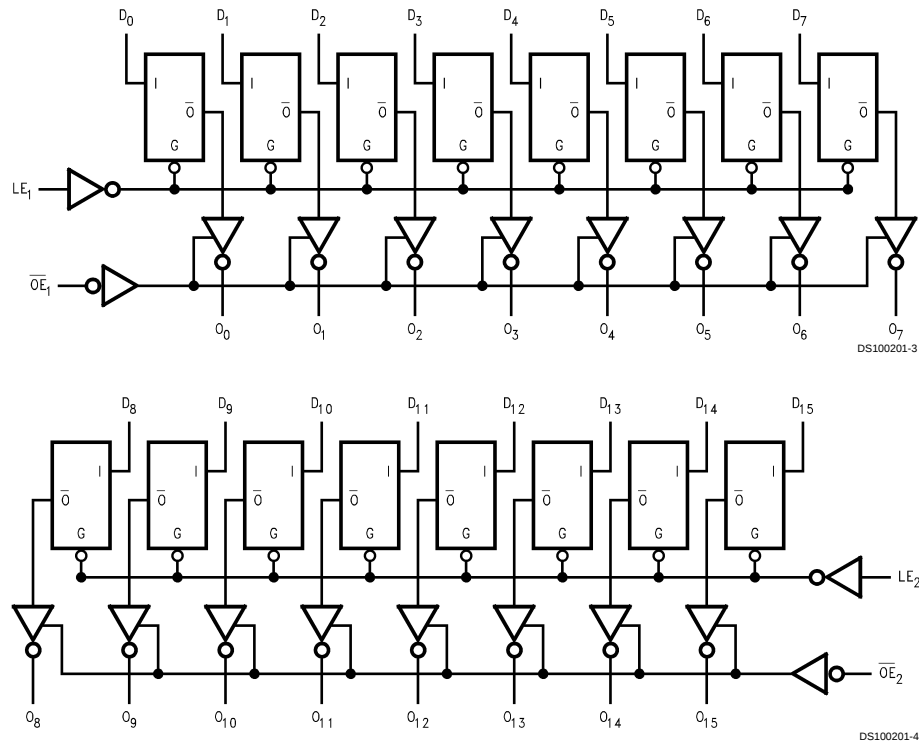
L = Low Voltage Level

X = Immaterial

Z = High Impedance

Previous = previous output prior to HIGH to LOW transition of LE

## Logic Diagrams



## Absolute Maximum Ratings (Note 1)

|                                                                  |                                      |
|------------------------------------------------------------------|--------------------------------------|
| Storage Temperature                                              | –65°C to +150°C                      |
| Ambient Temperature under Bias                                   | –55°C to +125°C                      |
| Junction Temperature under Bias                                  |                                      |
| Ceramic                                                          | –55°C to +175°C                      |
| V <sub>CC</sub> Pin Potential to Ground Pin                      | –0.5V to +7.0V                       |
| Input Voltage (Note 2)                                           | –0.5V to +7.0V                       |
| Input Current (Note 2)                                           | –30 mA to +5.0 mA                    |
| Voltage Applied to Any Output in the Disabled or Power-Off State | –0.5V to +5.5V                       |
| in the HIGH State                                                | –0.5V to V <sub>CC</sub>             |
| Current Applied to Output in LOW State (Max)                     | twice the rated I <sub>OL</sub> (mA) |
| DC Latchup Source Current: $\overline{OE}$ Pin                   | –350 mA                              |

(Across Comm Operating Range) Other Pins –500 mA  
Over Voltage Latchup (I/O) 10V

## Recommended Operating Conditions

|                              |                         |
|------------------------------|-------------------------|
| Free Air Ambient Temperature |                         |
| Military                     | –55°C to +125°C         |
| Supply Voltage               |                         |
| Military                     | +4.5V to +5.5V          |
| Minimum Input Edge Rate      | ( $\Delta V/\Delta t$ ) |
| Data Input                   | 50 mV/ns                |
| Enable Input                 | 20 mV/ns                |

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

| Symbol           | Parameter                         | ABT16373          |      |      | Units      | V <sub>CC</sub> | Conditions                                                                                                |
|------------------|-----------------------------------|-------------------|------|------|------------|-----------------|-----------------------------------------------------------------------------------------------------------|
|                  |                                   | Min               | Typ  | Max  |            |                 |                                                                                                           |
| V <sub>IH</sub>  | Input HIGH Voltage                | 2.0               |      |      | V          |                 | Recognized HIGH Signal                                                                                    |
| V <sub>IL</sub>  | Input LOW Voltage                 |                   | 0.8  |      | V          |                 | Recognized LOW Signal                                                                                     |
| V <sub>CD</sub>  | Input Clamp Diode Voltage         |                   | –1.2 |      | V          | Min             | I <sub>IN</sub> = –18 mA                                                                                  |
| V <sub>OH</sub>  | Output HIGH Voltage               | 54ABT             | 2.5  |      |            |                 | I <sub>OH</sub> = –3 mA                                                                                   |
|                  |                                   | 54ABT             | 2.0  |      |            |                 | I <sub>OH</sub> = –24 mA                                                                                  |
| V <sub>OL</sub>  | Output LOW Voltage                | 54ABT             | 0.55 |      | V          | Min             | I <sub>OL</sub> = 48 mA                                                                                   |
| I <sub>IH</sub>  | Input HIGH Current                |                   | 5    |      | μA         | Max             | V <sub>IN</sub> = 2.7V (Note 4)                                                                           |
|                  |                                   |                   | 5    |      |            |                 | V <sub>IN</sub> = V <sub>CC</sub>                                                                         |
| I <sub>BVI</sub> | Input HIGH Current Breakdown Test |                   | 7    |      | μA         | Max             | V <sub>IN</sub> = 7.0V                                                                                    |
| I <sub>IL</sub>  | Input LOW Current                 |                   | –5   |      | μA         | Max             | V <sub>IN</sub> = 0.5V (Note 4)                                                                           |
|                  |                                   |                   | –5   |      |            |                 | V <sub>IN</sub> = 0.0V                                                                                    |
| V <sub>ID</sub>  | Input Leakage Test                | 4.75              |      |      | V          | 0.0             | I <sub>ID</sub> = 1.9 μA<br>All Other Pins Grounded                                                       |
| I <sub>OZH</sub> | Output Leakage Current            |                   | 50   |      | μA         | 0 – 5.5V        | V <sub>OUT</sub> = 2.7V; $\overline{OE}$ = 2.0V                                                           |
| I <sub>OZL</sub> | Output Leakage Current            |                   | –50  |      | μA         | 0 – 5.5V        | V <sub>OUT</sub> = 0.5V; $\overline{OE}$ = 2.0V                                                           |
| I <sub>OS</sub>  | Output Short-Circuit Current      | –100              | –275 |      | mA         | Max             | V <sub>OUT</sub> = 0.0V                                                                                   |
| I <sub>CEX</sub> | Output High Leakage Current       |                   | 50   |      | μA         | Max             | V <sub>OUT</sub> = V <sub>CC</sub>                                                                        |
| I <sub>ZZ</sub>  | Bus Drainage Test                 |                   | 100  |      | μA         | 0.0             | V <sub>OUT</sub> = 5.5V; All Others GND                                                                   |
| I <sub>CCH</sub> | Power Supply Current              |                   | 2.0  |      | mA         | Max             | All Outputs HIGH                                                                                          |
| I <sub>CCL</sub> | Power Supply Current              |                   | 85   |      | mA         | Max             | All Outputs LOW                                                                                           |
| I <sub>CCZ</sub> | Power Supply Current              |                   | 2.0  |      | mA         | Max             | $\overline{OE}$ = V <sub>CC</sub><br>All Others at V <sub>CC</sub> or GND                                 |
| I <sub>CCT</sub> | Additional I <sub>CC</sub> /Input | Outputs Enabled   | 2.5  |      | mA         |                 | V <sub>I</sub> = V <sub>CC</sub> – 2.1V                                                                   |
|                  |                                   | Outputs TRI-STATE | 2.5  |      | mA         | Max             | Enable Input V <sub>I</sub> = V <sub>CC</sub> – 2.1V                                                      |
|                  |                                   | Outputs TRI-STATE | 2.5  |      | mA         |                 | Data Input V <sub>I</sub> = V <sub>CC</sub> – 2.1V<br>All Others at V <sub>CC</sub> or GND                |
| I <sub>CCD</sub> | Dynamic I <sub>CC</sub>           | No Load           |      | 0.15 | mA/<br>MHz | Max             | Outputs Open, LE = V <sub>CC</sub><br>$\overline{OE}$ = GND, (Note 3)<br>One Bit Toggling, 50% Duty Cycle |

**Note 3:** For 8 bits toggling, I<sub>CCD</sub> < 0.8 mA/MHz.

**Note 4:** Guaranteed, but not tested.

## AC Electrical Characteristics

| Symbol    | Parameter           | 54ABT                                                                                                                  |     | Units |
|-----------|---------------------|------------------------------------------------------------------------------------------------------------------------|-----|-------|
|           |                     | $T_A = -55^{\circ}\text{C to } +125^{\circ}\text{C}$<br>$V_{CC} = 4.5\text{V to } 5.5\text{V}$<br>$C_L = 50\text{ pF}$ |     |       |
|           |                     | Min                                                                                                                    | Max |       |
| $t_{PLH}$ | Propagation Delay   | 1.4                                                                                                                    | 6.5 | ns    |
| $t_{PHL}$ | $D_n$ to $O_n$      | 1.4                                                                                                                    | 6.5 |       |
| $t_{PLH}$ | Propagation Delay   | 1.7                                                                                                                    | 7.0 | ns    |
| $t_{PHL}$ | LE to $O_n$         | 1.4                                                                                                                    | 6.3 |       |
| $t_{PZH}$ | Output Enable Time  | 1.1                                                                                                                    | 6.8 | ns    |
| $t_{PZL}$ |                     | 1.5                                                                                                                    | 6.8 |       |
| $t_{PHZ}$ | Output Disable Time | 1.5                                                                                                                    | 8.5 | ns    |
| $t_{PLZ}$ |                     | 1.6                                                                                                                    | 8.0 |       |

## AC Operating Requirements

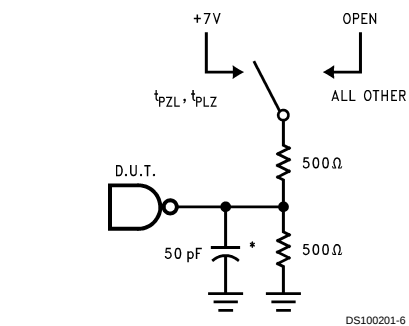
| Symbol          | Parameter               | 54ABT                                                                                                                  |     | Units |
|-----------------|-------------------------|------------------------------------------------------------------------------------------------------------------------|-----|-------|
|                 |                         | $T_A = -55^{\circ}\text{C to } +125^{\circ}\text{C}$<br>$V_{CC} = 4.5\text{V to } 5.5\text{V}$<br>$C_L = 50\text{ pF}$ |     |       |
|                 |                         | Min                                                                                                                    | Max |       |
|                 |                         |                                                                                                                        |     |       |
| $t_s(\text{H})$ | Setup Time, HIGH        | 2.4                                                                                                                    |     | ns    |
| $t_s(\text{L})$ | or LOW $D_n$ to LE      | 2.4                                                                                                                    |     |       |
| $t_h(\text{H})$ | Hold Time, HIGH         | 2.2                                                                                                                    |     | ns    |
| $t_h(\text{L})$ | or LOW $D_n$ to LE      | 2.2                                                                                                                    |     |       |
| $t_w(\text{H})$ | Pulse Width,<br>LE HIGH | 3.3                                                                                                                    |     | ns    |

## Capacitance

| Symbol             | Parameter          | Typ | Units | Conditions<br>( $T_A = 25^{\circ}\text{C}$ ) |
|--------------------|--------------------|-----|-------|----------------------------------------------|
| $C_{IN}$           | Input Capacitance  | 5   | pF    | $V_{CC} = 0\text{V}$                         |
| $C_{OUT}$ (Note 5) | Output Capacitance | 11  | pF    | $V_{CC} = 5.0\text{V}$                       |

**Note 5:**  $C_{OUT}$  is measured at frequency  $f = 1\text{ MHz}$ , per MIL-STD-883B, Method 3012.

## AC Loading



\*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

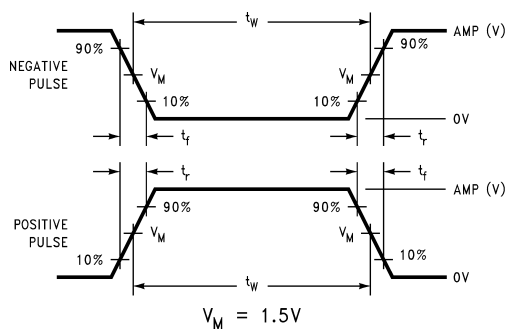


FIGURE 2. Test Input Signal Levels

| Amplitude | Rep. Rate | $t_w$  | $t_r$  | $t_f$  |
|-----------|-----------|--------|--------|--------|
| 3.0V      | 1 MHz     | 500 ns | 2.5 ns | 2.5 ns |

FIGURE 3. Test Input Signal Requirements

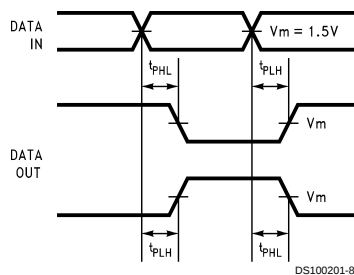


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

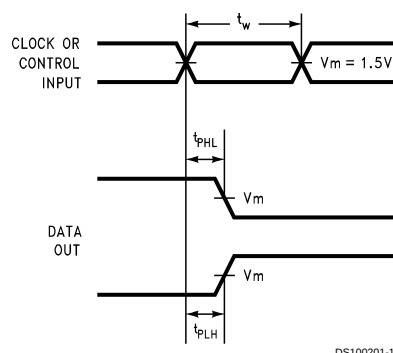


FIGURE 5. Propagation Delay, Pulse Width Waveforms

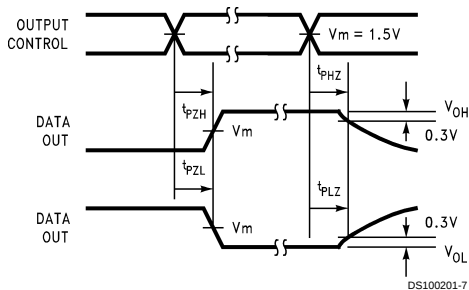


FIGURE 6. TRI-STATE Output HIGH and LOW Enable and Disable Times

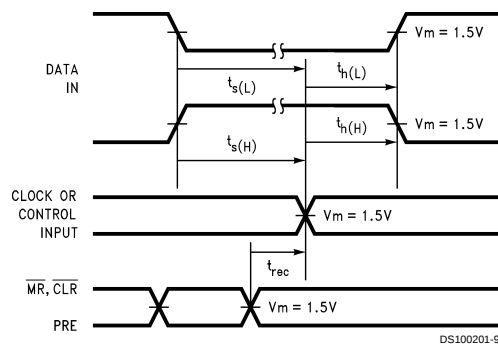
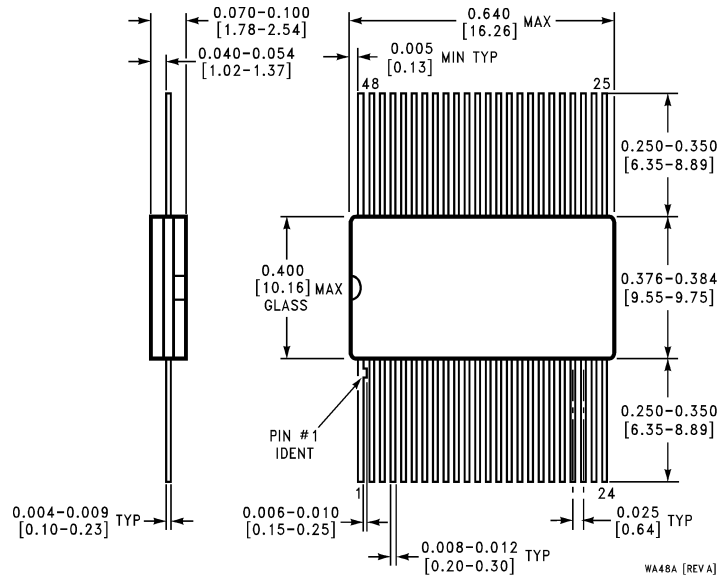


FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

## Physical Dimensions inches (millimeters) unless otherwise noted



**48-Lead Cerpack**  
**NS Package Number WA48A**

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