



July 1998

54ABT16500

18-Bit Universal Bus Transceivers with TRI-STATE® Outputs

General Description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable ($\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$), latch-enable ($\overline{\text{LEAB}}$ and $\overline{\text{LEBA}}$), and clock ($\overline{\text{CLKAB}}$ and $\overline{\text{CLKBA}}$) inputs. For A-to-B data flow, the device operates in the transparent mode when $\overline{\text{LEAB}}$ is high. When $\overline{\text{LEAB}}$ is low, the A data is latched if $\overline{\text{CLKAB}}$ is held at a high or low logic level. If $\overline{\text{LEAB}}$ is low, the A bus data is stored in the latch/flip-flop on the high-to-low transition of $\overline{\text{CLKAB}}$. Output-enable $\overline{\text{OEAB}}$ is active-high. When $\overline{\text{OEAB}}$ is high, the outputs are active. When $\overline{\text{OEAB}}$ is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{CLKBA}}$. The output enables are complementary ($\overline{\text{OEAB}}$ is active high and $\overline{\text{OEBA}}$ is active low).

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Features

- Combines D-Type latches and D-Type flip-flops for operation in transparent, latched, or clocked mode
- Flow-through architecture optimizes PCB layout
- Guaranteed latch-up protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Standard Microcircuit Drawing (SMD) 5962-9687001

Ordering Code

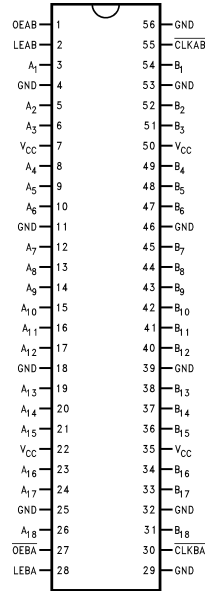
Military	Package Number	Package Description
54ABT16500W-QML	WA56A	56-Lead Cerpac

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Connection Diagram

Pin Assignment for Cerpack



DS100225-1

Function Table (Note 1)

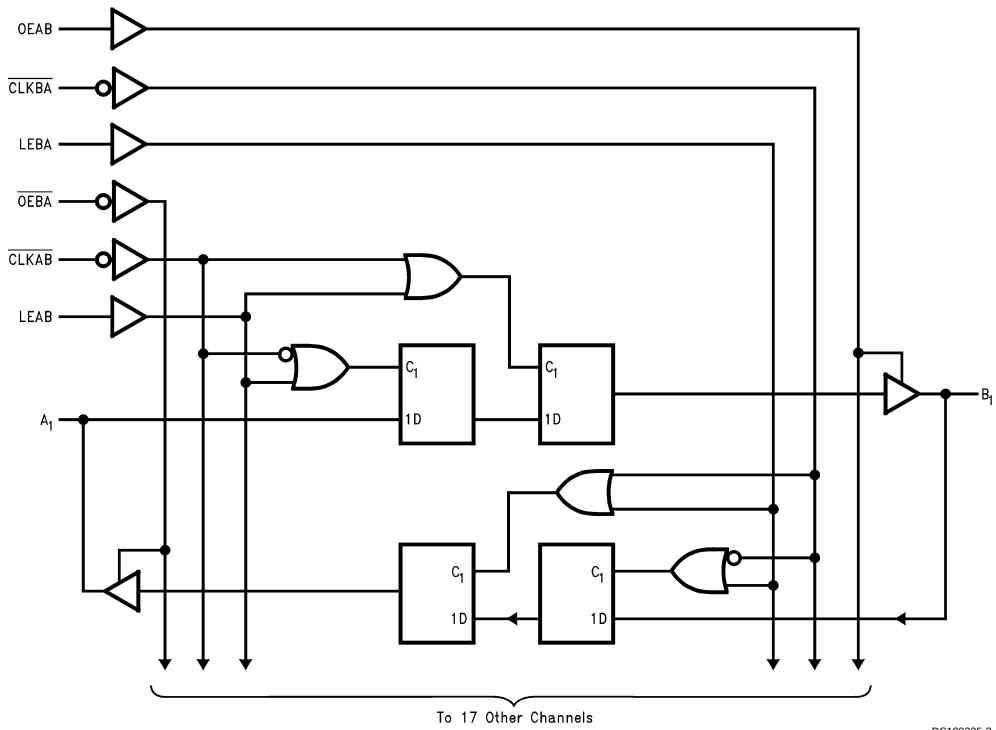
Inputs				Output
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B ₀ (Note 2)
H	L	L	X	B ₀ (Note 3)

Note 1: A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{CLKBA}}$.

Note 2: Output level before the indicated steady-state input conditions were established.

Note 3: Output level before the indicated steady-state input conditions were established, provided that $\overline{\text{CLKAB}}$ was low before $\overline{\text{LEAB}}$ went low.

Logic Diagram



DS100225-2

Absolute Maximum Ratings (Note 4)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
V _{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 4)	−0.5V to +7.0V
Input Current (Note 4)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V _{CC}
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
DC Latchup Source Current	−500 mA

Over Voltage Latchup (I/O)

10V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

Note 4: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 5: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	ABT16500			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage		0.8		V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage		−1.2		V	Min	I _{IN} = −18 mA
V _{OH}	Output HIGH Voltage	54ABT	2.5		V	Min	I _{OH} = −3 mA
			2.0		V	Min	I _{OH} = −24 mA
V _{OL}	Output LOW Voltage	54ABT		0.55	V	Min	I _{OL} = 48 mA
I _{IH}	Input HIGH Current			5	μA	Max	V _{IN} = 2.7V (Note 6)
				5			V _{IN} = V _{CC}
I _{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V _{IN} = 7.0V
I _{IL}	Input LOW Current			−5	μA	Max	V _{IN} = 0.5V (Note 6)
				−5			V _{IN} = 0.0V
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{IH} + I _{OZH}	Output Leakage Current			50	μA	0 – 5.5V	V _{OUT} = 2.7V; $\overline{\text{OE}}$, OE = 2.0V
I _{IL} + I _{OZL}	Output Leakage Current			−50	μA	0 – 5.5V	V _{OUT} = 0.5V; $\overline{\text{OE}}$, OE = 2.0V
I _{OS}	Output Short-Circuit Current	−100	−275		mA	Max	V _{OUT} = 0V
I _{CEx}	Output High Leakage Current		50		μA	Max	V _{OUT} = V _{CC}
I _{ZZ}	Bus Drainage Test		100		μA	0.0	V _{OUT} = 5.5V; All Others GND
I _{CCH}	Power Supply Current		1.0		mA	Max	All Outputs HIGH
I _{CCL}	Power Supply Current		68		μA	Max	An or Bn Outputs Low
I _{CCZ}	Power Supply Current		1.0		mA	Max	$\overline{\text{OE}}_n$ = V _{CC} , All Others at V _{CC} or GND
I _{CCT}	Additional I _{CC} /Input		2.5		mA	Max	V _I = V _{CC} − 2.1V All Others at V _{CC} or GND
I _{CCD}	Dynamic I _{CC} (Note 6)	No Load		0.23	mA/ MHz	Max	Outputs Open Transparent Mode One Bit Toggling, 50% Duty Cycle

Note 6: Guaranteed, but not tested.

DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units	V _{CC}	Conditions C _L = 50 pF; R _L = 500Ω
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}		1.1	V	5.0	T _A = 25°C (Note 7)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}		-1.7	V	5.0	T _A = 25°C (Note 7)

Note 7: Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

AC Electrical Characteristics

Symbol	Parameter	54ABT		Units	Fig. No.
		T _A = –55°C to +125°C V _{CC} = 4.5V–5.5V C _L = 50 pF			
		Min	Max		
f _{max}	Maximum Clock Frequency	150		MHz	
t _{PLH}	Propagation Delay	1.0	6.5	ns	Figure 4
t _{PHL}	A or B to B or A	1.0	7.0		
t _{PLH}	Propagation Delay	1.0	7.0	ns	Figure 4
t _{PHL}	LEAB or LEBA to B or A	1.0	7.8		
t _{PLH}	Propagation Delay	1.0	7.5	ns	Figure 4
t _{PHL}	CLKAB or CLKBA to B or A	1.0	8.0		
t _{PZH}	Propagation Delay	1.0	6.3	ns	Figure 6
t _{PZL}	OEAB or $\overline{\text{OEBA}}$ to B or A	1.0	6.5		
t _{PHZ}	Propagation Delay	1.0	7.2	ns	Figure 6
t _{PLZ}	OEAB or $\overline{\text{OEBA}}$ to B or A	1.0	6.8		

AC Operating Requirements

Symbol	Parameter	54ABT		Units	Fig. No.
		T _A = –55°C to +125°C V _{CC} = 4.5V–5.5V C _L = 50 pF			
		Min	Max		
t _s (H)	Setup Time, A to CLKAB	4.5		ns	Figure 7
t _s (L)		4.5			
t _h (H)	Hold Time, A to CLKAB	0		ns	Figure 7
t _h (L)		0			
t _s (H)	Setup Time, B to CLKBA	4.0		ns	Figure 7
t _s (L)		4.0			
t _h (H)	Hold Time, B to CLKBA	0		ns	Figure 7
t _h (L)		0			
t _s (H)	Setup Time, A to LEAB	1.5		ns	Figure 7
t _s (L)	or B to LEBA, CLK High	1.5			
t _h (H)	Hold Time, A to LEAB	1.5		ns	Figure 7
t _h (L)	or B to LEBA, CLK High	1.5			
t _s (H)	Setup Time, A to LEAB	4.5		ns	Figure 7
t _s (L)	or B to LEBA, CLK Low	4.5			
t _h (H)	Hold Time, A to LEAB	1.5		ns	Figure 7
t _h (L)	or B to LEBA, CLK Low	1.5			
t _w (H)	Pulse Width, LEAB or LEBA, High	3.3		ns	Figure 5
t _w (L)		3.3			

AC Operating Requirements (Continued)

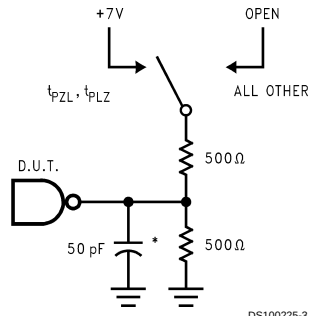
Symbol	Parameter	54ABT	Units	Fig. No.
		$T_A = -55^{\circ}\text{C to } +125^{\circ}\text{C}$ $V_{CC} = 4.5\text{V} - 5.5\text{V}$ $C_L = 50\text{ pF}$		
		Min Max		
$t_w(\text{H})$	Pulse Width, $\overline{\text{CLKAB}}$	3.3	ns	Figure 5
$t_w(\text{L})$	or $\overline{\text{CLKBA}}$, High or Low	3.3		

Capacitance

Symbol	Parameter	Typ	Units	Conditions, $T_A = 25^{\circ}\text{C}$
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0.0\text{V}$
C_{IO} (Note 8)	Output Capacitance	11.0	pF	$V_{CC} = 5.0\text{V}$

Note 8: C_{IO} is measured at frequency $f = 1\text{ MHz}$ per MIL-STD-883B, Method 3012.

AC Loading



*Includes jig and probe capacitance.

FIGURE 1. Standard AC Test Load

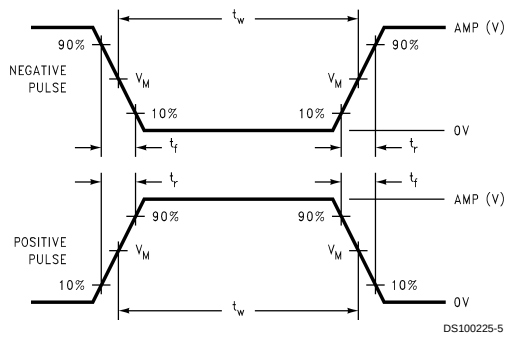


FIGURE 2. $V_M = 1.5V$

Input Pulse Requirements

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

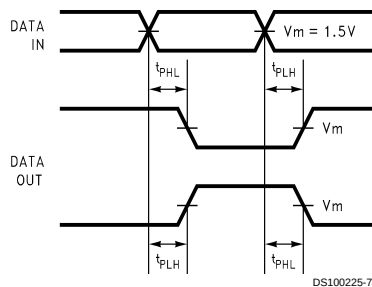


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

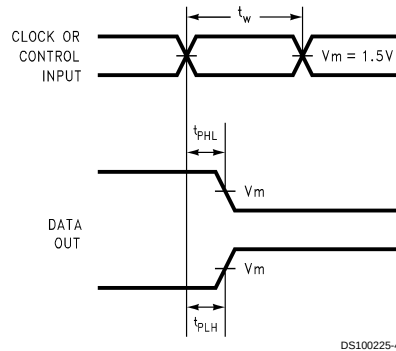


FIGURE 5. Propagation Delay, Pulse Width Waveforms

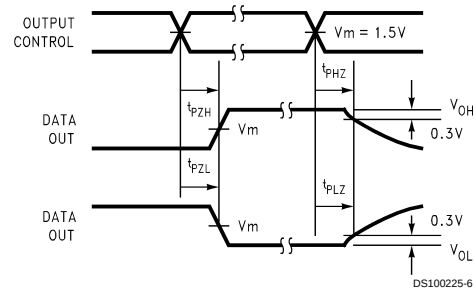


FIGURE 6. TRI-STATE Output HIGH and LOW Enable and Disable Times

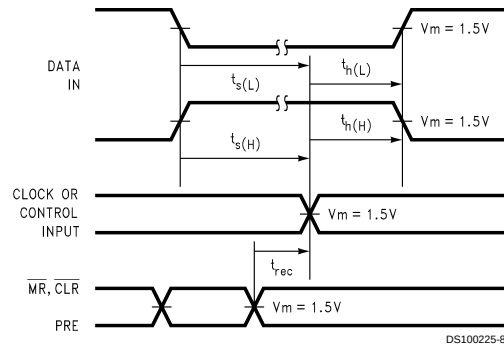
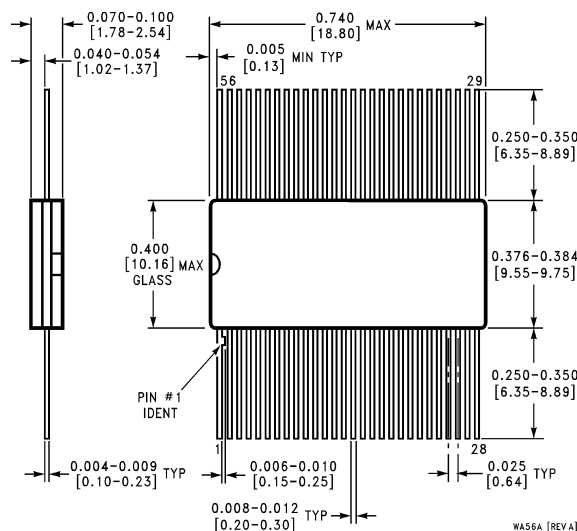


FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Cerpack
NS Package Number WA56A

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