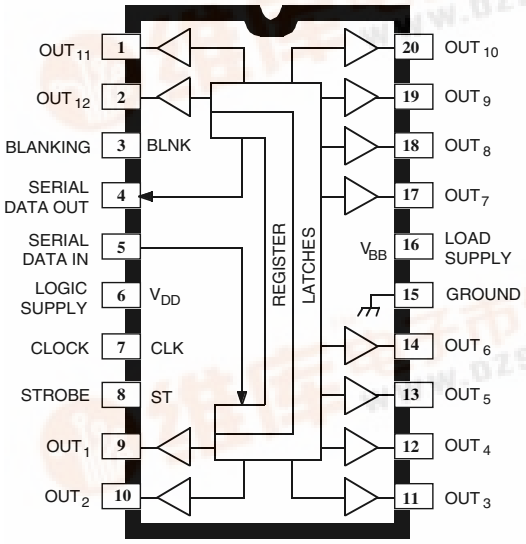
5811

Data Sheet
26182.20B

BiMOS II 12-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS



Dwg. PP-029-5

ABSOLUTE MAXIMUM RATINGS
at T_A = 25°C

Logic Supply Voltage, V_{DD} ..... **15 V**
Driver Supply Voltage, V_{BB} ..... **60 V**
Continuous Output Current,
I_{OUT} ..... **-40 mA to +25 mA**
Input Voltage Range,
V_{IN} ..... **-0.3 V to V_{DD} + 0.3 V**
Package Power Dissipation,
P_D ..... **See Graph**
Operating Temperature Range,
T_A ..... **-20°C to +85°C**
Storage Temperature Range,
T_S ..... **-55°C to +150°C**

Designed primarily for use with vacuum-fluorescent displays, the UCN5811A smart power BiMOS II driver features low-output saturation voltages and high output switching speed. These devices contain CMOS shift registers, data latches, and control circuitry, and bipolar high-speed sourcing outputs with DMOS active pull-down circuitry. The high-speed shift register and data latches allow direct interface with microprocessor-based systems. A CMOS serial data output enables cascade connections in applications requiring additional drive lines.

The UCN5811A features 60 V and -40 mA output ratings, allowing it to be used in many other peripheral power driver applications. It can be used as an improved replacement tor the SN75512B. The Allegro devices do not require special power-up sequencing.

The UCN5811A has been designed with BiMOS II logic for improved data entry rates. With a 5 V supply, it will operate to at least 3.3 MHz. At 12 V, higher speeds are possible. Use of this device with TTL may require the use of appropriate pull-up resistors to ensure a proper input logic high.

This device is supplied in a 20-pin plastic dual in-line package. It can be operated over the ambient temperature range of -20°C to +85°C. Copper lead frames and low output saturation voltages allow all outputs to be operated at 25 mA continuously at ambient temperatures of up to 76°C.

FEATURES

- To 3.3 MHz Data Input Rate
- Low-Power CMOS Logic and Latches
- High-Speed Source Drivers
- Active Pull-Downs
- Low-Output Saturation Voltages
- Improved Replacement for SN75512B

Always order by complete part number: **UCN5811A** .

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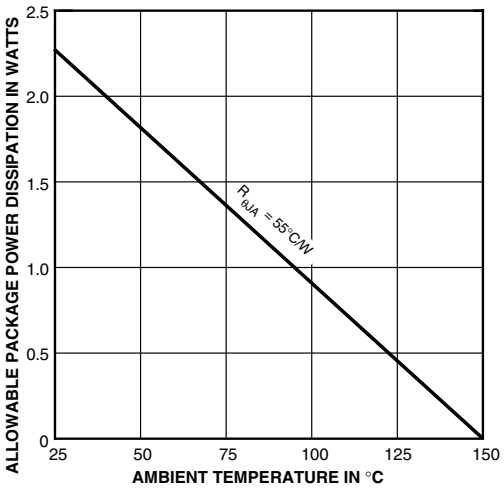
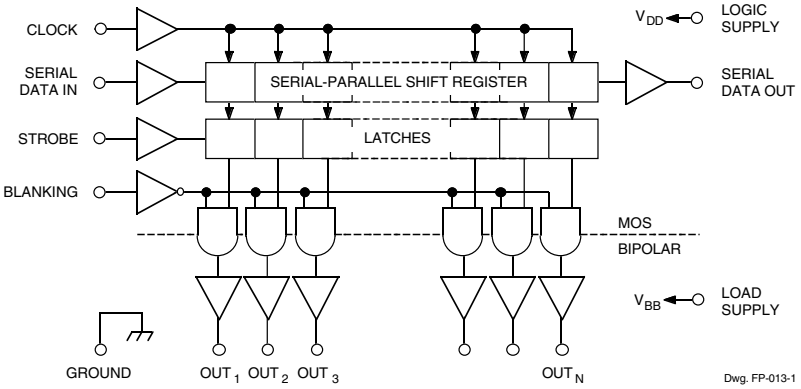


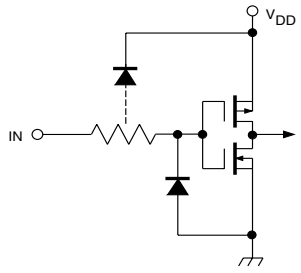
Dwg. GS-004-1

FUNCTIONAL BLOCK DIAGRAM



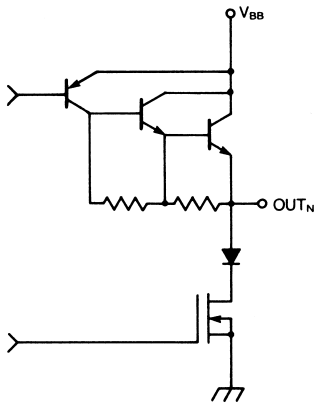
Dwg. FP-013-1

TYPICAL INPUT CIRCUIT



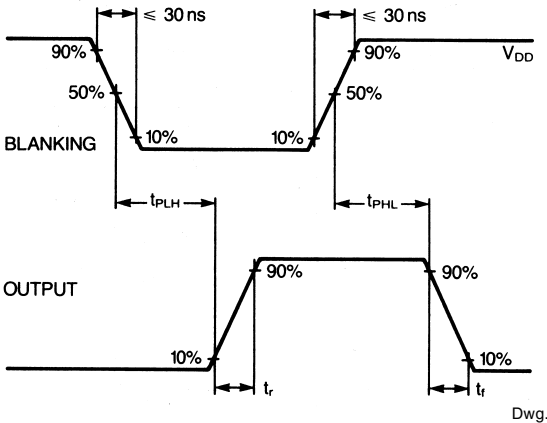
Dwg. EP-010-5

TYPICAL OUTPUT DRIVER



Dwg. W-182

TIMING WAVESHAPES



Dwg. W-184

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 60 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits @ V_{DD} = 5 V			Limits @ V_{DD} = 12 V			Units
			Mln.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{OUT} = 0 V, T_A = +70°C	—	-5.0	-15	—	-5.0	-15	µA
Output Voltage	$V_{OUT(H)}$	I_{OUT} = -25 mA, V_{BB} = 60 V	58	58.5	—	58	58.5	—	V
	$V_{OUT(L)}$	I_{OUT} = 1 mA	—	2.0	3.0	—	—	—	V
		I_{OUT} = 2 mA	—	—	—	—	2.0	3.0	V
Output Pull-Down Current	$I_{OUT(L)}$	V_{OUT} = 10 V to V_{BB}	2.5	4.0	—	—	—	—	mA
		V_{OUT} = 40 V to V_{BB}	—	—	—	15	18	—	mA
Input Voltage	$V_{IN(1)}$		3.5	—	5.3	10.5	—	12.3	V
	$V_{IN(0)}$		-0.3	—	+0.8	-0.3	—	+0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = V_{DD}	—	0.05	0.5	—	0.1	1.0	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	-0.05	-0.5	—	-1.0	-1.0	µA
Serial Data Output Voltage	$V_{OUT(H)}$	I_{OUT} = -200 µA	4.5	4.7	—	11.7	11.8	—	V
	$V_{OUT(L)}$	I_{OUT} = 200 µA	—	200	250	—	100	200	mV
Maximum Clock Frequency	f_{clk}		3.3*	—	—	—	—	—	MHz
Supply Current	$I_{DD(H)}$	All Outputs High	—	3.0	5.0	—	15	20	mA
	$I_{DD(L)}$	All Outputs Low	—	2.5	4.0	—	7.0	10	mA
	$I_{BB(H)}$	Outputs High, No Load	—	7.5	12	—	7.5	12	mA
	$I_{BB(L)}$	Outputs Low	—	10	100	—	10	100	µA
Blanking to Output Delay	t_{PHL}	C_L = 30 pF	—	300	550	—	125	150	ns
	t_{PLH}	C_L = 30 pF	—	250	450	—	170	200	ns
Output Fall Time	t_f	C_L = 30 pF	—	1000	1250	—	250	300	ns
Output Rise Time	t_r	C_L = 30 pF	—	150	170	—	150	170	ns

Negative current is defined as coming out of (sourcing) the specified device pin.
* Operation at a clock frequency greater than the specified minimum value is possible but not warranteed.

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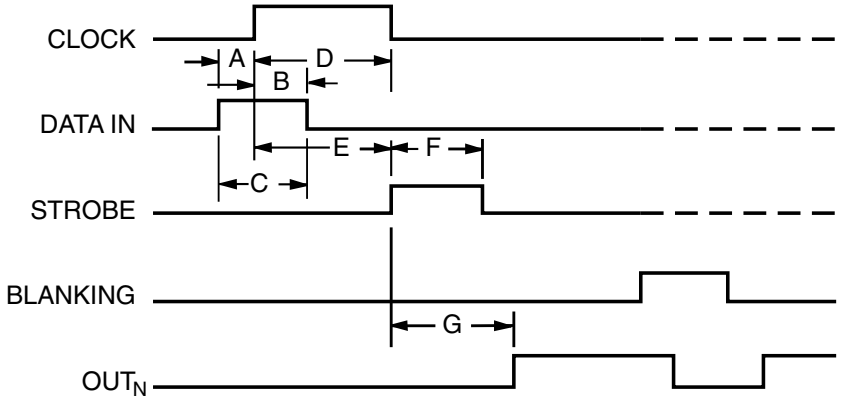
BiMOS II 12-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS



Dwg. No. 12,649A

TIMING REQUIREMENTS

(T_A = +25°C, V_{DD} = 5 V, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) ..... **75 ns**

B. Minimum Data Active Time After Clock Pulse (Data Hold Time) ..... **75 ns**

C. Minimum Data Pulse Width ..... **150 ns**

D. Minimum Clock Pulse Width ..... **150 ns**

E. Minimum Time Between Clock Activation and Strobe ..... **300 ns**

F. Minimum Strobe Pulse Width ..... **100 ns**

G. Typical Time Between Strobe Activation and Output Transistion ..... **500 ns**

Timing is representative of a 3.3 MHz clock. Higher speeds may be attainable with increased supply voltage; operation at high temperatures will reduce the specified maximum clock frequency.

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, the output source drivers are disabled (OFF); the DMOS sink drivers are ON, the information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

TRUTH TABLE

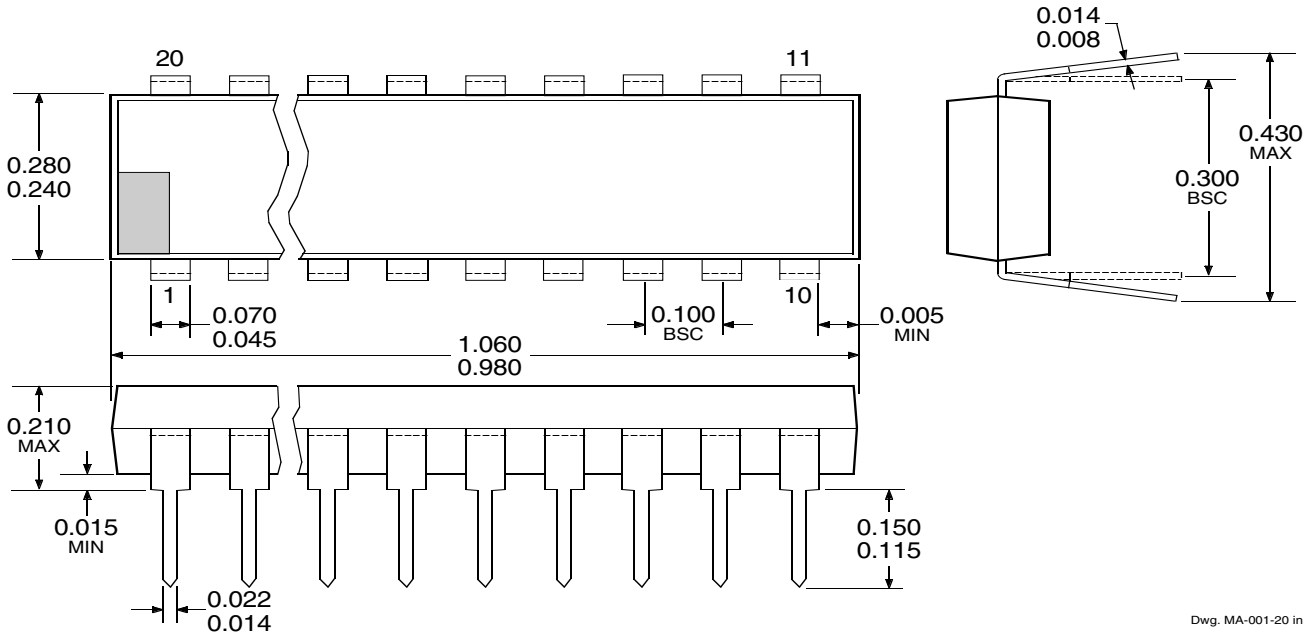
Serial Data Input	Clock Input	Shift Register Contents I_1 I_2 I_3 ... I_{N-1} I_N	Serial Data Output	Strobe Input	Latch Contents I_1 I_2 I_3 ... I_{N-1} I_N	Blanking	Output Contents I_1 I_2 I_3 ... I_{N-1} I_N
H	⌐	H R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
L	⌐	L R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
X	⌐	R_1 R_2 R_3 ... R_{N-1} R_N	R_N				
		X X X ... X X	X	L	R_1 R_2 R_3 ... R_{N-1} R_N		
		P_1 P_2 P_3 ... P_{N-1} P_N	P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N	L	P_1 P_2 P_3 ... P_{N-1}
P_N					X X X ... X X	H	L L L ... L L

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

115 Northeast Cutoff, Box 15036

UCN5811A

Dimensions in Inches
(controlling dimensions)



NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.
3. Lead thickness is measured at seating plane or below.
4. Supplied in standard sticks/tubes of 18 devices.

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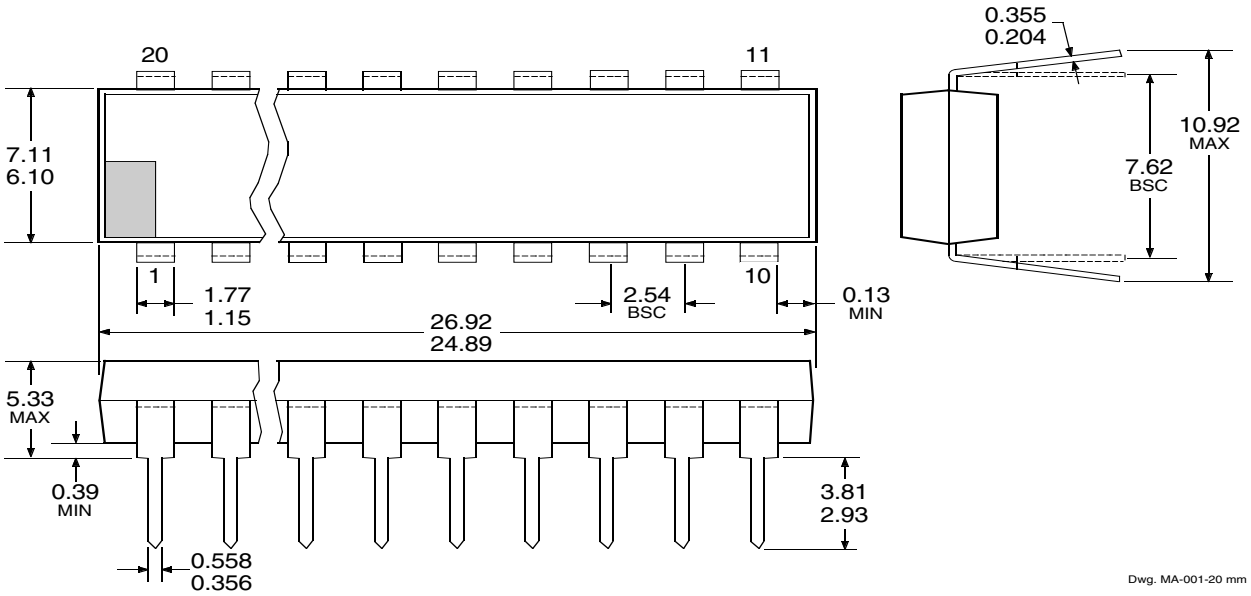
BiMOS II 12-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS

UCN5811A

Dimensions in Millimeters
(for reference only)



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BiMOS II 12-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS

POWER INTERFACE DRIVERS

Function	Output Ratings*		Part Number†
SERIAL-INPUT LATCHED DRIVERS			
8-Bit (saturated drivers)	-120 mA	50 V‡	5895
8-Bit	350 mA	50 V	5821
8-Bit	350 mA	80 V	5822
8-Bit	350 mA	50 V‡	5841
8-Bit	350 mA	80 V‡	5842
8-Bit (constant-current LED driver)	75 mA	17 V	6275
8-Bit (DMOS drivers)	250 mA	50 V	6595
8-Bit (DMOS drivers)	350 mA	50 V‡	6A595
8-Bit (DMOS drivers)	100 mA	50 V	6B595
10-Bit (active pull-downs)	-25 mA	60 V	5810-F and 6809/10
12-Bit (active pull-downs)	-25 mA	60 V	5811 and 6811
16-Bit (constant-current LED driver)	75 mA	17 V	6276
20-Bit (active pull-downs)	-25 mA	60 V	5812-F and 6812
32-Bit (active pull-downs)	-25 mA	60 V	5818-F and 6818
32-Bit	100 mA	30 V	5833
32-Bit (saturated drivers)	100 mA	40 V	5832
PARALLEL-INPUT LATCHED DRIVERS			
4-Bit	350 mA	50 V‡	5800
8-Bit	-25 mA	60 V	5815
8-Bit	350 mA	50 V‡	5801
8-Bit (DMOS drivers)	100 mA	50 V	6B273
8-Bit (DMOS drivers)	250 mA	50 V	6273
SPECIAL-PURPOSE DEVICES			
Unipolar Stepper Motor Translator/Driver	1.25 A	50 V‡	5804
Addressable 8-Bit Decoder/DMOS Driver	250 mA	50 V	6259
Addressable 8-Bit Decoder/DMOS Driver	350 mA	50 V‡	6A259
Addressable 8-Bit Decoder/DMOS Driver	100 mA	50 V	6B259
Addressable 28-Line Decoder/Driver	450 mA	30 V	6817

* Current is maximum specified test condition, voltage is maximum rating. See specification for sustaining voltage limits. Negative current is defined as coming out of (sourcing) the output.

† Complete part number includes additional characters to indicate operating temperature range and package style.

‡ Internal transient-suppression diodes included for inductive-load protection.