

FAIRCHILD
SEMICONDUCTOR™

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74ACT258 Quad 2-Input Multiplexer with 3-STATE Outputs

General Description

The ACT258 is a quad 2-input multiplexer with 3-STATE outputs. Four bits of data from two sources can be selected using a common data select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable (\overline{OE}) input, allowing the outputs to interface directly with bus-oriented systems.

Features

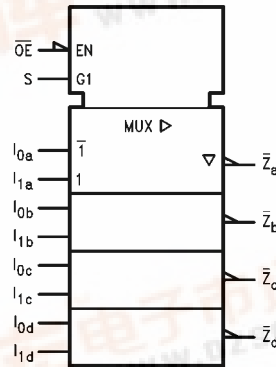
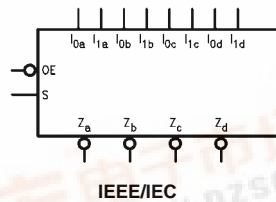
- I_{CC} and I_{OZ} reduced by 50%
- Multiplexer expansion by tying outputs together
- Inverting 3-STATE outputs
- Outputs source/sink 24 mA
- TTL-compatible inputs

Ordering Code:

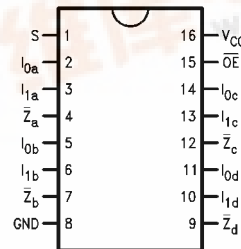
| Order Number | Package Number | Package Description |
|--------------|----------------|---|
| 74ACT258SC | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body |
| 74ACT258SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE 11, 5.3mm Wide |
| 74ACT258MTC | MTC16 | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74ACT258PC | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Pin Descriptions

| Pin Names | Description |
|---------------------------------|--------------------------------|
| S | Common Data Select Input |
| \overline{OE} | 3-STATE Output Enable Input |
| $I_{0a}-I_{0d}$ | Data Inputs from Source 0 |
| $I_{1a}-I_{1d}$ | Data Inputs from Source 1 |
| $\overline{Z}_a-\overline{Z}_d$ | 3-STATE Inverting Data Outputs |

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74ACT258 Quad 2-Input Multiplexer with 3-STATE Outputs



Truth Table

| Output Enable | Select Input | Data Inputs | | Outputs |
|-----------------|--------------|-------------|-------|----------------|
| \overline{OE} | S | I_0 | I_1 | \overline{Z} |
| H | X | X | X | Z |
| L | H | X | L | H |
| L | H | X | H | L |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance

Functional Description

The ACT258 is a quad 2-input multiplexer with 3-STATE outputs. It selects four bits of data from two sources under control of a common Select input (S). When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in inverted form. The ACT258 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{OE} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S})$$

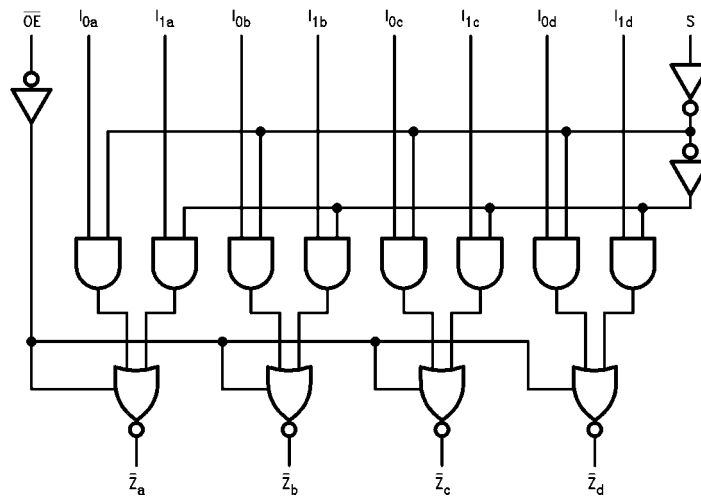
$$\overline{Z}_b = \overline{OE} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$

$$\overline{Z}_c = \overline{OE} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S})$$

$$\overline{Z}_d = \overline{OE} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

When the Output Enable input (\overline{OE}) is HIGH, the outputs are forced to a high impedance state. If the outputs of the 3-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-STATE devices whose outputs are tied together are designed so there is no overlap.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

| | |
|---|--------------------------|
| Supply Voltage (V_{CC}) | -0.5V to +7.0V |
| DC Input Diode Current (I_{IK}) | |
| $V_I = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | +20 mA |
| DC Input Voltage (V_I) | -0.5V to $V_{CC} + 0.5V$ |
| DC Output Diode Current (I_{OK}) | |
| $V_O = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | +20 mA |
| DC Output Voltage (V_O) | -0.5V to $V_{CC} + 0.5V$ |
| DC Output Source or Sink Current (I_O) | ± 50 mA |
| DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND}) | ± 50 mA |
| Storage Temperature (T_{STG}) | -65°C to +150°C |
| Junction Temperature (T_J) | |
| PDIP | 140°C |

Recommended Operating Conditions

| | |
|---|----------------|
| Supply Voltage (V_{CC}) | 4.5V to 5.5V |
| Input Voltage (V_I) | 0V to V_{CC} |
| Output Voltage (V_O) | 0V to V_{CC} |
| Operating Temperature (T_A) | -40°C to +85°C |
| Minimum Input Edge Rate ($\Delta V/\Delta t$) | |
| V_{IN} from 0.8V to 2.0V | |
| V_{CC} @ 4.5V, 5.5V | 125 mV/ns |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics

| Symbol | Parameter | V_{CC} (V) | $T_A = +25^\circ\text{C}$ | | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ | | Units | Conditions |
|-----------|--------------------------------------|-----------------|---------------------------|-------------------|---|---------|--|------------|
| | | | Typ | Guaranteed Limits | | | | |
| V_{IH} | Minimum HIGH Level Input Voltage | 4.5 | 1.5 | 2.0 | 2.0 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| | | 5.5 | 1.5 | 2.0 | 2.0 | | | |
| V_{IL} | Maximum LOW Level Input Voltage | 4.5 | 1.5 | 0.8 | 0.8 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| | | 5.5 | 1.5 | 0.8 | 0.8 | | | |
| V_{OH} | Minimum HIGH Level Output Voltage | 4.5 | 4.49 | 4.4 | 4.4 | V | $I_{OUT} = -50 \mu A$ | |
| | | 5.5 | 5.49 | 5.4 | 5.4 | | | |
| | | 4.5 | | 3.86 | 3.76 | V | $V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA (Note 2)}$ | |
| | | 5.5 | | 4.86 | 4.76 | | | |
| V_{OL} | Maximum LOW Level Output Voltage | 4.5 | 0.001 | 0.1 | 0.1 | V | $I_{OUT} = 50 \mu A$ | |
| | | 5.5 | 0.001 | 0.1 | 0.1 | | | |
| | | 4.5 | | 0.36 | 0.44 | V | $V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA (Note 2)}$ | |
| | | 5.5 | | 0.36 | 0.44 | | | |
| I_{IN} | Maximum Input Leakage Current | 5.5 | | ± 0.1 | ± 1.0 | μA | $V_I = V_{CC}, GND$ | |
| I_{OZ} | Maximum 3-STATE Current | 5.5 | | ± 0.25 | ± 2.5 | μA | $V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$ | |
| I_{CCT} | Maximum I_{CC} /Input | 5.5 | 0.6 | | 1.5 | mA | $V_I = V_{CC} - 2.1V$ | |
| I_{OLD} | Minimum Dynamic | 5.5 | | | 75 | mA | $V_{OLD} = 1.65V$ Max | |
| | Output Current (Note 3) | 5.5 | | | -75 | mA | $V_{OHD} = 3.85V$ Min | |
| I_{CC} | Maximum Quiescent Supply Current | 5.5 | | 4.0 | 40.0 | μA | $V_{IN} = V_{CC}$ or GND | |

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

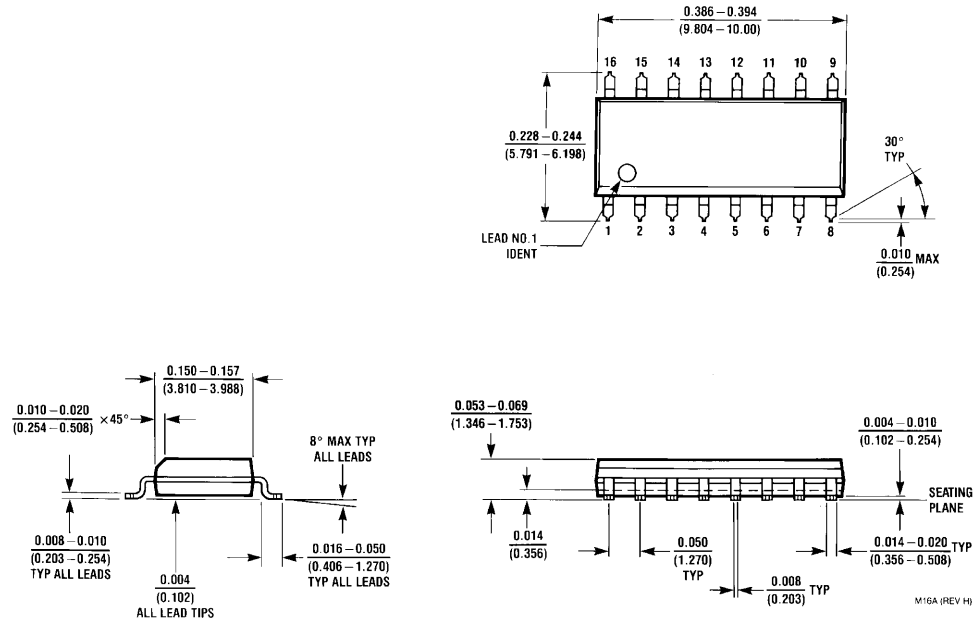
| AC Electrical Characteristics | | | | | | | | |
|-------------------------------|--|------------------------------------|--|-----|------|---|------|-------|
| Symbol | Parameter | V _{CC} (V) (Note 4) | T _A = +25°C C _L = 50 pF | | | T _A = -40°C to +85°C C _L = 50 pF | | Units |
| | | | Min | Typ | Max | Min | Max | |
| t _{PLH} | Propagation Delay I _n to \bar{Z}_n | 5.0 | 2.0 | 6.5 | 8.5 | 1.5 | 9.5 | ns |
| t _{PHL} | Propagation Delay I _n to \bar{Z}_n | 5.0 | 2.0 | 5.5 | 7.5 | 1.5 | 8.0 | ns |
| t _{PLH} | Propagation Delay S to \bar{Z}_n | 5.0 | 3.0 | 7.5 | 10.5 | 2.0 | 11.5 | ns |
| t _{PHL} | Propagation Delay S to \bar{Z}_n | 5.0 | 1.5 | 7.0 | 9.5 | 1.5 | 11.0 | ns |
| t _{PZH} | Output Enable Time | 5.0 | 2.0 | 6.5 | 8.5 | 1.5 | 9.5 | ns |
| t _{PZL} | Output Enable Time | 5.0 | 2.0 | 6.5 | 8.5 | 1.5 | 9.5 | ns |
| t _{PHZ} | Output Disable Time | 5.0 | 1.5 | 7.0 | 9.0 | 1.0 | 10.0 | ns |
| t _{PLZ} | Output Disable Time | 5.0 | 2.0 | 6.0 | 8.0 | 1.5 | 9.0 | ns |

Note 4: Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

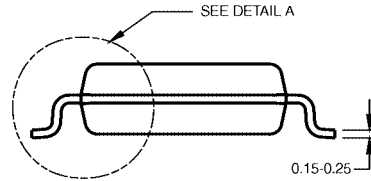
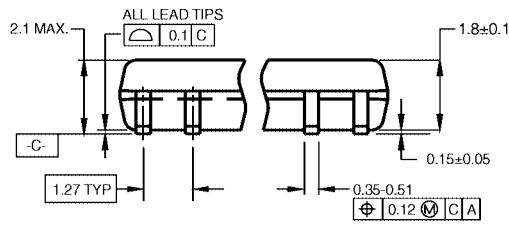
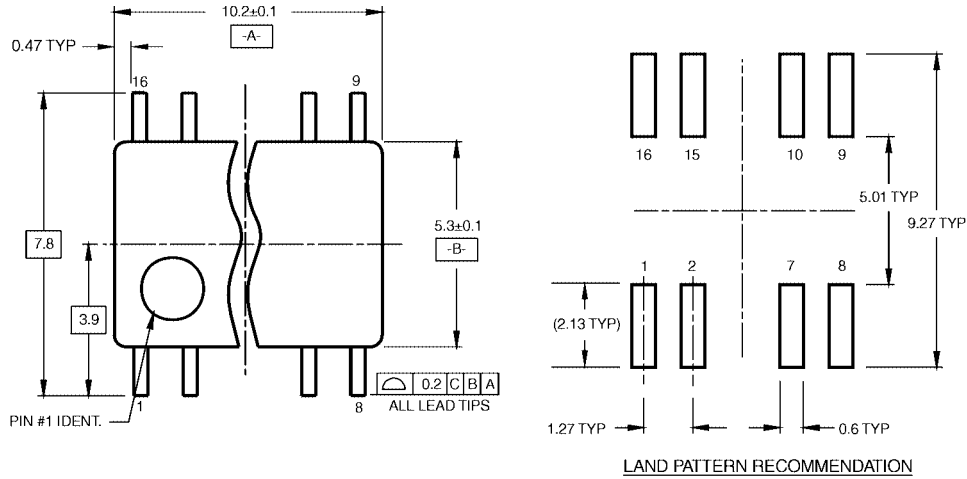
| Symbol | Parameter | Typ | Units | Conditions |
|-----------------|-------------------------------|------|-------|------------------------|
| C _{IN} | Input Capacitance | 4.5 | pF | V _{CC} = OPEN |
| C _{PD} | Power Dissipation Capacitance | 55.0 | pF | V _{CC} = 5.0V |

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body Package Number M16A

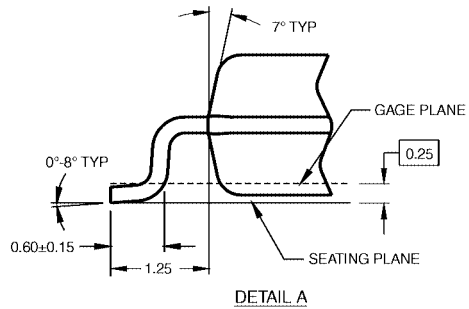
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

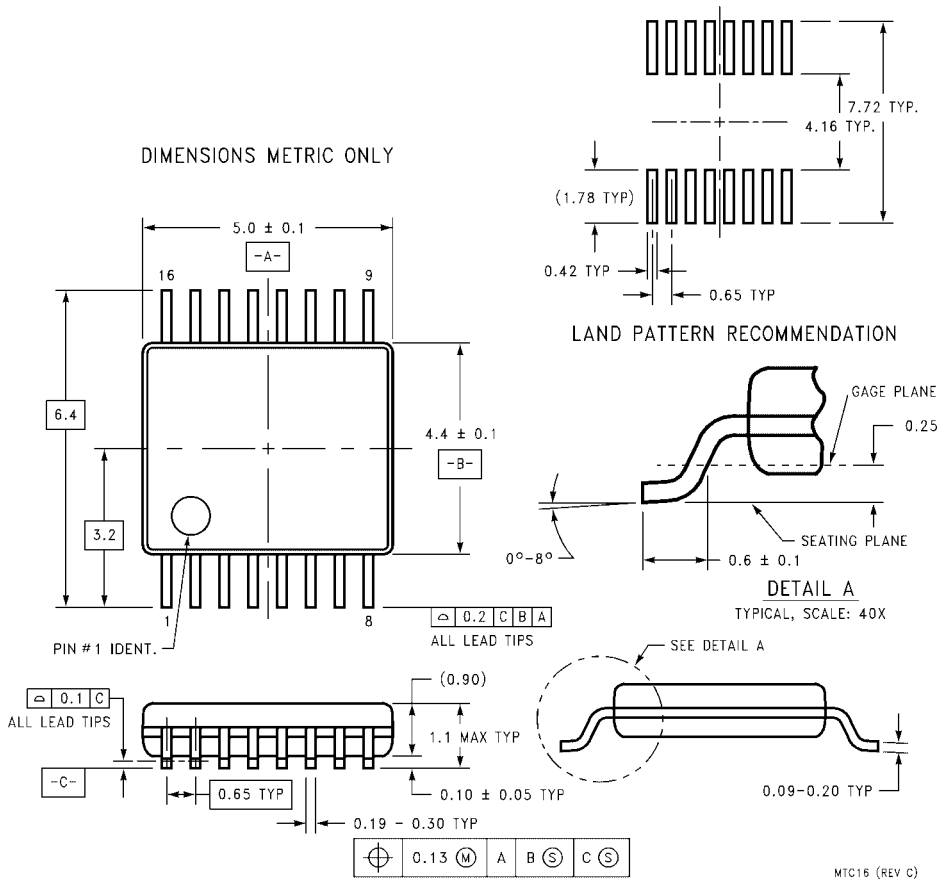
- NOTES:
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1



**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
 Package Number M16D**

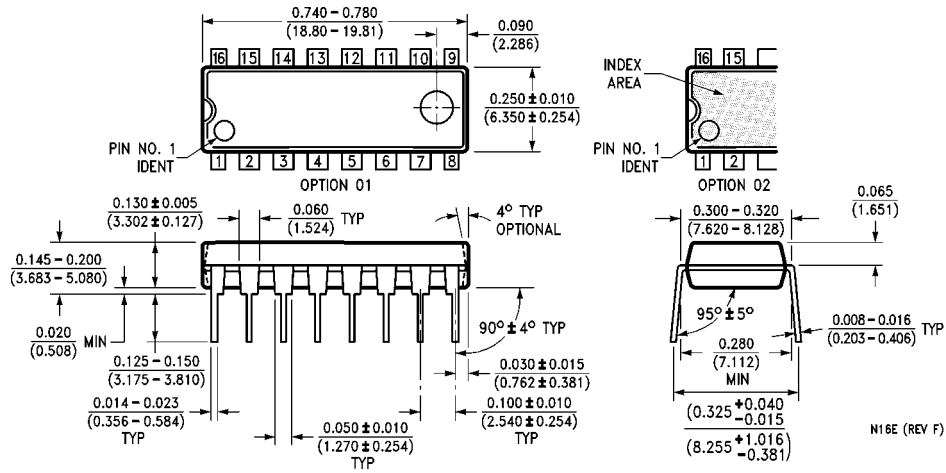
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16**

MTC16 (REV C)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

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