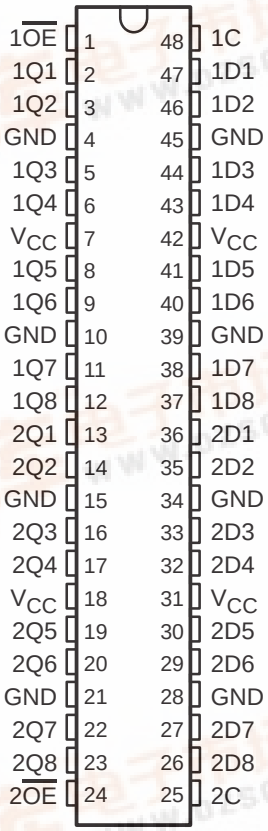
SN54ACT16373, 74ACT16373
16-BIT D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SCAS122C – MARCH 1990 – REVISED SEPTEMBER 1996

- Members of the Texas Instruments *Widebus*™ Family
- Inputs Are TTL-Voltage Compatible
- 3-State Bus Driving True Outputs
- Full Parallel Access for Loading
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- *EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Shrink Small-Outline (DL) 300-mil Packages Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings

SN54ACT16373 . . . WD PACKAGE
74ACT16373 . . . DL PACKAGE
(TOP VIEW)



description

The SN54ACT16373 and 74ACT16373 are 16-bit D-type transparent latches with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. These devices can be used as two 8-bit latches or one 16-bit latch. The Q outputs of the latches follow the data (D) inputs if enable C is taken high. When C is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines in a bus-organized system without need for interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

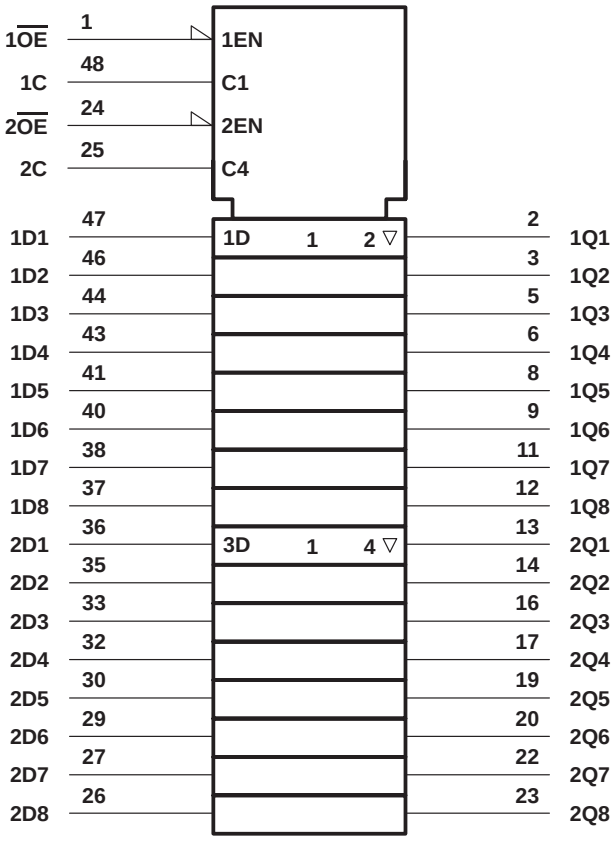
The 74ACT16373 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ACT16373 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT16373 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

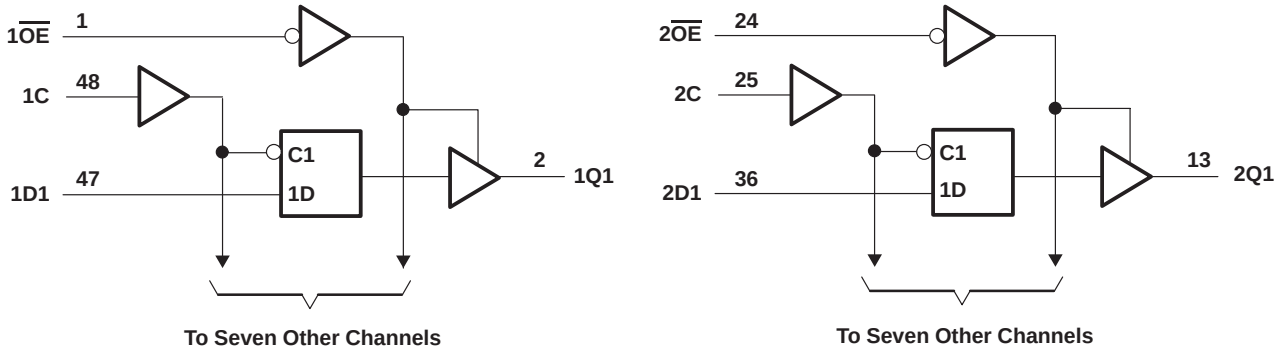
INPUTS			OUTPUT
$\overline{OE}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±400 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DL package . . . . . 1.2 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

		SN54ACT16373		74ACT16373		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage (see Note 4)	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTES: 3. Unused inputs should be tied to V_{CC} through a pullup resistor of approximately 5 kΩ or greater to prevent them from floating.
4. All V_{CC} and GND pins must be connected to the proper voltage supply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54ACT16373		74ACT16373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = –24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = –50 mA†	5.5 V				3.85				
	I_{OH} = –75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_o	$V_I = V_{CC}$ or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		T_A = 25°C		SN54ACT16373		74ACT16373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	4		4		1		ns
t_{su}	Setup time, data before LE↓	1		1		1		ns
t_h	Hold time, data after LE↓	5		5		5		ns

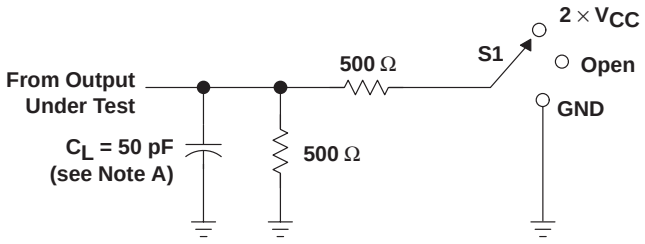
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			SN54ACT16373		74ACT16373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	3.8	7.9	9.4	3.8	11.8	3.8	11.1	ns
t_{PHL}			3.1	8.2	9.7	3.1	13	3.1	12.3	
t_{PLH}	LE	Q	4.6	9.3	10.8	4.6	13.7	4.6	12.8	ns
t_{PHL}			4.5	9.1	10.5	4.5	13	4.5	12.2	
t_{PZH}	$\overline{OE}$	Q	3.1	8	9.5	3.1	13	3.1	12.1	ns
t_{PZL}			3.8	9.4	11.1	3.8	15.1	3.8	14.2	
t_{PHZ}	$\overline{OE}$	Q	5.3	8.6	9.9	5.3	11	5.3	10.7	ns
t_{PLZ}			4.3	7.4	8.7	4.3	9.8	4.3	9.4	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

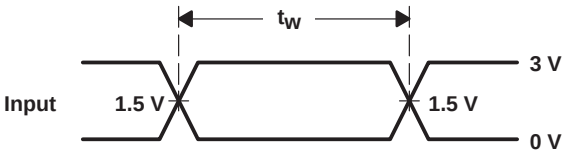
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 1 MHz	43	pF
		Outputs disabled		4.5	

PARAMETER MEASUREMENT INFORMATION

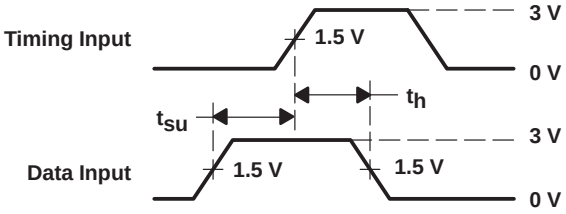


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

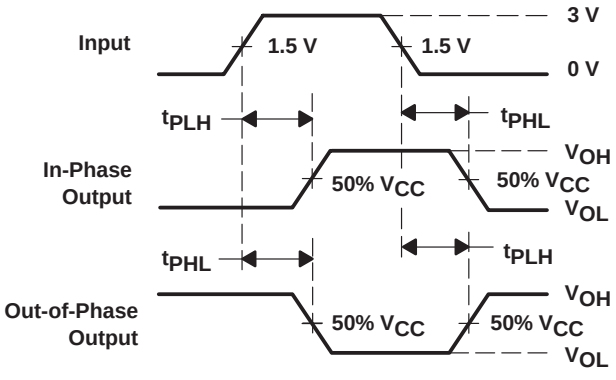
LOAD CIRCUIT



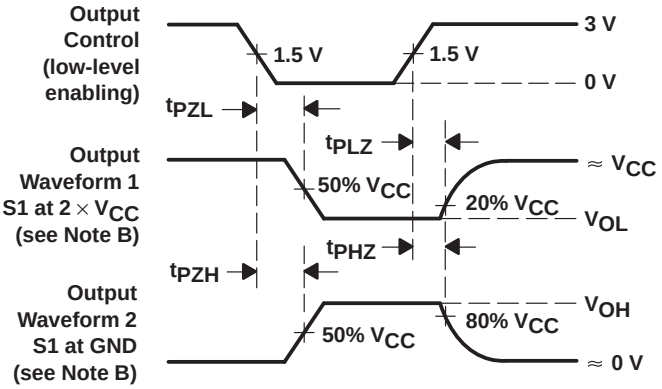
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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