





SLLS533B - MAY 2002 - REVISED MAY 2003

## **HIGH OUTPUT RS-485 TRANSCEIVERS**

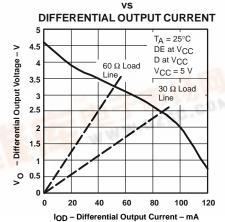
#### **FEATURES**

- Minimum Differential Output Voltage of 2.5 V Into a 54-Ω Load
- Open-Circuit, Short-Circuit, and Idle-Bus Failsafe Receiver
- 1/8<sup>th</sup> Unit-Load Option Available (Up to 256 Nodes on the Bus)
- Bus-Pin ESD Protection Exceeds 16 kV HBM
- Driver Output Slew Rate Control Options
- Electrically Compatible With ANSI TIA/EIA-485-A Standard
- Low-Current Standby Mode . . . 1 μA Typical
- Glitch-Free Power-Up and Power-Down Protection for Hot-Plugging Applications
- Pin Compatible With Industry Standard SN75176

### **APPLICATIONS**

- Data Transmission Over Long or Lossy Lines or Electrically Noisy Environments
- Profibus Line Interface
- Industrial Process Control Networks
- Point-of-Sale (POS) Networks
- Electric Utility Metering
- Building Automation
- Digital Motor Control

# DIFFERENTIAL OUTPUT VOLTAGE

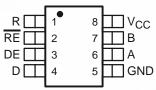


### DESCRIPTION

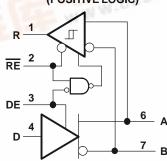
SN65HVD05. SN75HVD05, SN65HVD06, SN75HVD06, SN65HVD07, and SN75HVD07 combine a 3-state differential line driver and differential line receiver. They are designed for balanced data interoperate transmission and with **ANSI** TIA/EIA-485-A and ISO 8482E standard-compliant devices. The driver is designed to provide a differential output voltage greater than that required by these standards for increased noise margin. The drivers and receivers have active-high and active-low enables respectively, which can be externally connected together to function as direction control.

The driver differential outputs and receiver differential inputs connect internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or not powered. These devices feature wide positive and negative common-mode voltage ranges, making them suitable for party-line applications.

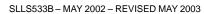
### D OR P PACKAGE (TOP VIEW)



# LOGIC DIAGRAM (POSITIVE LOGIC)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.







 $These devices have {\it limited built-in ESD protection}. The {\it leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.}$ 

# ORDERING INFORMATION(1)

							(ED AS
SIGNALING RATE	UNIT LOAD	DRIVER OUTPUT SLOPE CONTROL	Т <sub>А</sub>	PART NUMBER(2)		PLASTIC DUAL-IN-LINE PACKAGE (PDIP)	SMALL OUTLINE IC (SOIC) PACKAGE
40 Mbps	1/2	No		SN65HVD05D	SN65HVD05P	65HVD05	VP05
10 Mbps	1/8	Yes	-40°C to 85°C	SN65HVD06D	SN65HVD06P	65HVD06	VP06
1 Mbps	1/8	Yes		SN65HVD07D	SN65HVD07P	65HVD07	VP07
40 Mbps	1/2	No		SN75HVD05D	SN75HVD05P	75HVD05	VN05
10 Mbps	1/8	Yes	−0°C to 70°C	SN75HVD06D	SN75HVD06P	75HVD06	VN06
1 Mbps	1/8	Yes		SN75HVD07D	SN75HVD07P	75HVD07	VN07

<sup>(1)</sup> For the most current specification and package information, refer to our web site at www.ti.com.

### PACKAGE DISSIPATION RATINGS (SEE FIGURE 12 AND FIGURE 13)

PACKAGE	T <sub>A</sub> ≤ 25°C POWER RATING	DERATING FACTOR <sup>(1)</sup> ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING
D(2)	710 mW	5.7 mW/°C	455 mW	369 mW
D(3)	1282 mW	10.3 mW/°C	821 mW	667 mW
Р	1000 mW	8.0 mW/°C	640 mW	520 mW

<sup>(1)</sup> This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

### ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1) (2)

			SN65HVD05, SN65HVD06, SN65HVD07 SN75HVD05, SN75HVD06, SN75HVD07
Supply voltage range, VC	C		-0.3 V to 6 V
Voltage range at A or B			–9 V to 14 V
Input voltage range at D,	DE, R or RE		-0.5 V to V <sub>CC</sub> + 0.5 V
Voltage input range, transient pulse, A and B, through 100 $\Omega$ (see Figure 11)			−50 V to 50 V
	Human body model(3)	A, B, and GND	16 kV
Electrostatic discharge		All pins	4 kV
	Charged-device model (4)	All pins	1 kV
Continuous total power dissipation			See Dissipation Rating Table
Storage temperature range, T <sub>Stg</sub>		−65°C to 150°C	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260°C

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

<sup>(2)</sup> The D package is available taped and reeled. Add an R suffix to the device type (i.e., SN65HVD05DR).

<sup>(2)</sup> Tested in accordance with the Low-K thermal metric definitions of EIA/JESD51-3

<sup>(3)</sup> Tested in accordance with the High-K thermal metric definitions of EIA/JESD51-7

<sup>(2)</sup> All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

<sup>(3)</sup> Tested in accordance with JEDEC Standard 22, Test Method A114-A.

<sup>(4)</sup> Tested in accordance with JEDEC Standard 22, Test Method C101.



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### RECOMMENDED OPERATING CONDITIONS

		MIN	NOM MAX	UNIT
Supply voltage, V <sub>CC</sub>		4.5	5.5	V
Voltage at any bus terminal (separately or co	mmon mode) V <sub>I</sub> or V <sub>IC</sub>	<sub>-7</sub> (1)	12	V
High-level input voltage, VIH	D, DE, RE	2		V
Low-level input voltage, V <sub>IL</sub>	D, DE, RE		0.8	V
Differential input voltage, V <sub>ID</sub> (see Figure 7)		-12	12	V
High-level output current, IOH	Driver	-100		
	Receiver	-8		mA
	Driver		100	
Low-level output current, IOL	Receiver		8	mA
	SN65HVD05			
	SN65HVD06	-40	85	°C
	SN65HVD07			
Operating free-air temperature, T <sub>A</sub>	SN75HVD05			
	SN75HVD06	0	70	°C
	SN75HVD07			

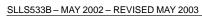
<sup>(1)</sup> The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

### **DRIVER ELECTRICAL CHARACTERISTICS**

over operating free-air temperature range unless otherwise noted (1)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT	
VIK	Input clamp voltage		I <sub>I</sub> = -18 mA		-1.5			V
		No Load				VCC		
VOD	Differential output voltage		$R_L$ = 54 Ω, See Figure 1		2.5			V
			$V_{\text{test}} = -7 \text{ V to } 12 \text{ V}, \text{ See}$	Figure 2	2.2			
Δ V <sub>OD</sub>	Change in magnitude of di output voltage	fferential	See Figure 1 and Figure 2		-0.2		0.2	V
V <sub>OC</sub> (SS)	Steady-state common-moo	de output	- See Figure 3		2.2		3.3	V
ΔVOC(SS)	Change in steady-state common-mode output volta	age			-0.1		0.1	V
	HVD05				600			
VOC(PP)	Peak-to-peak common- mode output voltage	HVD06	See Figure 3		500			mV
()	HVD0		1			900		
loz	High-impedance output cu	rrent	See receiver input current	S				
1.	lanut aumant	D			-100		0	
IĮ	Input current	DE			0		100	μΑ
los	Short-circuit output current	t	$-7 \text{ V} \le \text{V}_{\text{O}} \le 12 \text{ V}$		-250		250	mA
C <sub>(diff)</sub>	Differential output capacita	ince	$V_{ID} = 0.4 \sin(4E6\pi t) + 0.5$	5 V, DE at 0 V		16		pF
			RE at V <sub>CC</sub> , D & DE at V <sub>CC</sub> , No load	Receiver disabled and driver enabled		9	15	mA
I <sub>CC</sub> Supply current			RE at V <sub>CC</sub> , D at V <sub>CC</sub> DE at 0 V, No load	Receiver disabled and driver disabled (standby)		1	5	μА
			RE at 0 V, D & DE at V <sub>CC</sub> , No load	Receiver enabled and driver enabled		9	15	mA

<sup>(1)</sup> All typical values are at 25°C and with a 5-V supply.





### DRIVER SWITCHING CHARACTERISTICS NIL

over operating free-air temperature range unless otherwise noted

	PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT	
		HVD05			6.5	11		
<sup>t</sup> PLH	Propagation delay time, low-to-high-level output	HVD06			27	40	ns	
		HVD07			250	400		
		HVD05			6.5	11		
<sup>t</sup> PHL	Propagation delay time, high-to-low-level output	HVD06			27	40	ns	
		HVD07			250	400		
		HVD05	$R_L = 54 \Omega$	2.7	3.6	6		
t <sub>r</sub>	Differential output signal rise time	HVD06	$C_{L} = 50 \text{ pF},$	18	28	55	ns	
		HVD07	See Figure 4	150	300	450		
		HVD05		2.7	3.6	6		
tf	Differential output signal fall time	HVD06		18	28	55	ns	
		HVD07		150	300	450		
		HVD05				2	ns	
tsk(p)	Pulse skew ( tpHL - tpLH )	HVD06				2.5		
3K(p) (11 TIE		HVD07				10		
		HVD05				3.5		
t <sub>sk(pp)</sub> (2)	Part-to-part skew	HVD06				14	ns	
OK(PP)( )	•	HVD07				100	0	
		HVD05				25		
<sup>t</sup> PZH1	Propagation delay time, high-impedance-to-high-level output	HVD06				45	ns	
1 200		HVD07	RE at 0 V,			250	1	
		HVD05	R <sub>L</sub> = 110 Ω, See Figure 5	25		25		
<sup>t</sup> PHZ	Propagation delay time, high-level-to-high-impedance output	HVD06	_ See i iguie 5	60		ns		
		HVD07		250				
		HVD05				15		
<sup>t</sup> PZL1	Propagation delay time, high-impedance-to-low-level output	HVD06	_			45	ns	
1 21	11.3m	HVD07	RE at 0 V,	200				
		HVD05	R <sub>L</sub> = 110 Ω, See Figure 6			14		
<sup>t</sup> PLZ	Propagation delay time, low-level-to-high-impedance output	HVD06	_ See Figure 0	90		ns		
,		HVD07		550		-		
<sup>t</sup> PZH2	Propagation delay time, standby-to-high-level output	I	$\frac{\text{RL}}{\text{RE}}$ = 110 $\Omega$ , RE at 3 V, See Figure 5			6	μs	
<sup>†</sup> PZL2	Propagation delay time, standby-to-low-level output		$\frac{R_L}{RE}$ = 110 $\Omega$ , RE at 3 V, See Figure 6			6	μs	

 <sup>(1)</sup> All typical values are at 25°C and with a 5-V supply.
 (2) t<sub>Sk(pp)</sub> is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.



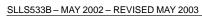
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# RECEIVER ELECTRICAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

	PARAMETER			TEST CONDITIONS	}	MIN	TYP(1)	MAX	UNIT
V <sub>IT+</sub>	Positive-going input thr voltage	eshold	I <sub>O</sub> = -8 mA					-0.01	V
VIT-	Negative-going input th voltage	reshold	I <sub>O</sub> = 8 mA			-0.2			V
V <sub>hys</sub>	Hysteresis voltage (V <sub>I</sub>	- <sub>+</sub> – V <sub>IT</sub> –)					35		mV
VIK	Enable-input clamp vol	age	I <sub>I</sub> = -18 mA			-1.5			V
Vон	High-level output voltaç	je	$V_{ID} = 200 \text{ mV},$	$I_{OH} = -8 \text{ mA},$	See Figure 7	4			V
VOL	Low-level output voltag	е	$V_{ID} = -200 \text{ mV},$	I <sub>OL</sub> = 8 mA,	See Figure 7			0.4	V
loz	High-impedance-state current	output	$V_O = 0$ or $V_{CC}$	RE at V <sub>CC</sub>		-1		1	μΑ
				$V_A$ or $V_B = 12 V$			0.23	0.5	
		Other input	$V_A$ or $V_B = 12 V$ ,	VCC = 0 V		0.3	0.5		
	HVD05 at 0 V $V_A$ or $V_B = -7$ V		-0.4	-0.13		mA			
	Dura immust ausmaust			$V_A$ or $V_B = -7 V$ ,	VCC = 0 V	-0.4	-0.15		
l <sub>l</sub>	Bus input current	Bus input current		V <sub>A</sub> or V <sub>B</sub> = 12 V			0.06	0.1	
		HVD06,	Otherinput	$V_A$ or $V_B = 12 V$ ,	ACC = 0 A		0.08	08 0.13	4
		HVD07	at 0 V	$V_A$ or $V_B = -7 V$		-0.1	-0.05		mA
				$V_A$ or $V_B = -7 V$ ,	VCC = 0 V	-0.05	-0.03		
lн	High-level input curren	, RE	V <sub>IH</sub> = 2 V	•		-60	-26.4		μΑ
IIL	Low-level input current	, RE	V <sub>IL</sub> = 0.8 V			-60	-27.4		μΑ
C <sub>(diff)</sub>	Differential input capac	tance	V <sub>I</sub> = 0.4 sin (4E6	πt) + 0.5 V, DE at 0	) V		16		pF
	I <sub>CC</sub> Supply current		RE at 0 V, D & DE at 0 V, No load	Receiver enabled a	nd driver disabled		5	10	mA
Icc			RE at V <sub>CC</sub> , DE at 0 V, D at V <sub>CC</sub> , No load	Receiver disabled a (standby)	and driver disabled		1	5	μΑ
			RE at 0 V, D & DE at V <sub>CC</sub> , No load	Receiver enabled a	nd driver enabled		9	15	mA

<sup>(1)</sup> All typical values are at 25°C and with a 5-V supply.





### **RECEIVER SWITCHING CHARACTERISTICS**

over operating free-air temperature range unless otherwise noted

	PARAMETER		TEST CONDITIONS	MIN TYP(1)	MAX	UNIT
tPLH	Propagation delay time, low-to-high-level output 1/2 UL	HVD05		14.6	25	ns
tPHL	Propagation delay time, high-to-low-level output 1/2 UL	HVD05		14.6	25	ns
4	Depression delections less to high level estant 4/0111	HVD06		55	70	
<sup>t</sup> PLH	Propagation delay time, low-to-high-level output 1/8 UL	HVD07	$V_{ID} = -1.5 \text{ V to } 1.5 \text{ V},$	55	70	ns
4	Depression delections high to level out out 4/0111	HVD06	C <sub>L</sub> = 15 pF,	55	70	
<sup>t</sup> PHL	Propagation delay time, high-to-low-level output 1/8 UL	HVD07	See Figure 8	55	70	ns
		HVD05			2	
tsk(p)	Pulse skew ( tpHL - tpLH )	HVD06			4.5	ns
		HVD07			4.5	
		HVD05			6.5	
t <sub>sk(pp)</sub> (2)	Part-to-part skew	ew HVD06			14	ns
,		HVD07			14	
t <sub>r</sub>	Output signal rise time		C <sub>L</sub> = 15 pF,	2	3	20
t <sub>f</sub>	Output signal fall time		See Figure 8	2	3	ns
<sup>t</sup> PZH1	Output enable time to high level				10	
tPZL1	tPZL1 Output enable time to low level		C <sub>L</sub> = 15 pF, DE at 3 V.		10	
tPHZ Output disable time from high level		See Figure 9		15	ns	
tPLZ	tPLZ Output disable time from low level				15	
tPZH2	Propagation delay time, standby-to-high-level output		C <sub>L</sub> = 15 pF, DE at 0,		6	_
tPZL2	Propagation delay time, standby-to-low-level output	_	See Figure 10		6	μs

 <sup>(1)</sup> All typical values are at 25°C and with a 5-V supply.
 (2) t<sub>Sk(pp)</sub> is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.



### PARAMETER MEASUREMENT INFORMATION

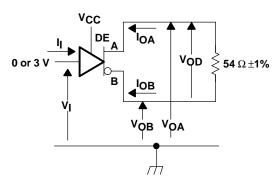
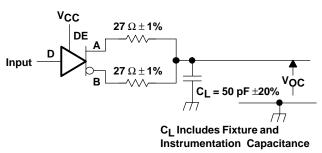
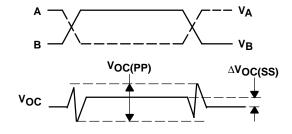


Figure 1. Driver V<sub>OD</sub> Test Circuit and Voltage and Current Definitions

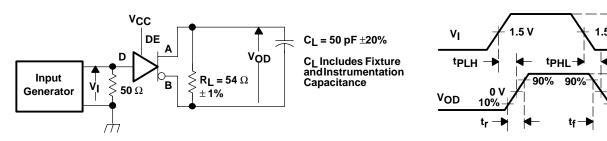
Figure 2. Driver V<sub>OD</sub> With Common-Mode Loading Test Circuit





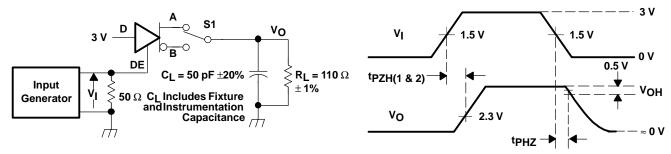
Input: PRR = 500 kHz, 50% Duty Cycle, $t_r$ <6ns,  $t_f$ <6ns,  $Z_O$  = 50  $\Omega$ 

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



Generator: PRR = 500 kHz, 50% Duty Cycle,  $t_{\Gamma}$  <6 ns,  $t_{f}$  <6 ns,  $Z_{O}$  = 50  $\Omega$ 

Figure 4. Driver Switching Test Circuit and Voltage Waveforms



Generator: PRR = 100 kHz, 50% Duty Cycle,  $t_r$  <6 ns,  $t_f$  <6 ns,  $Z_0$  = 50  $\Omega$ 

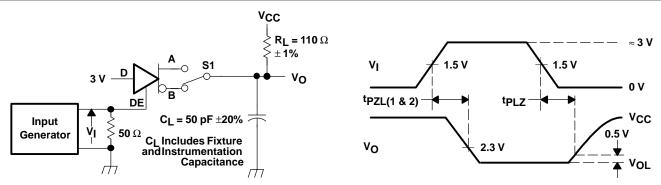
Figure 5. Driver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms

3 V

0 V

10%





Generator: PRR = 100 kHz, 50% Duty Cycle,  $t_{f}$  <6 ns,  $t_{f}$  <6 ns,  $Z_{o}$  = 50  $\Omega$ 

Figure 6. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

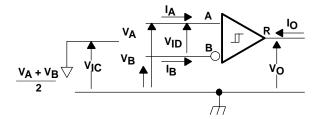


Figure 7. Receiver Voltage and Current Definitions

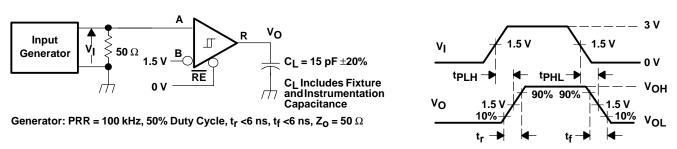


Figure 8. Receiver Switching Test Circuit and Voltage Waveforms



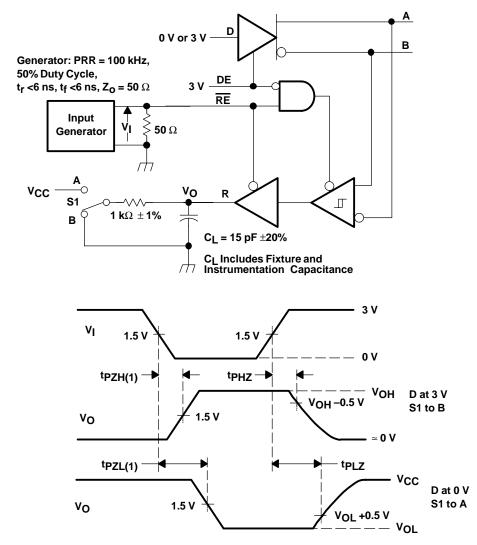


Figure 9. Receiver Enable and Disable Time Test Circuit and Voltage Waveforms With Drivers Enabled



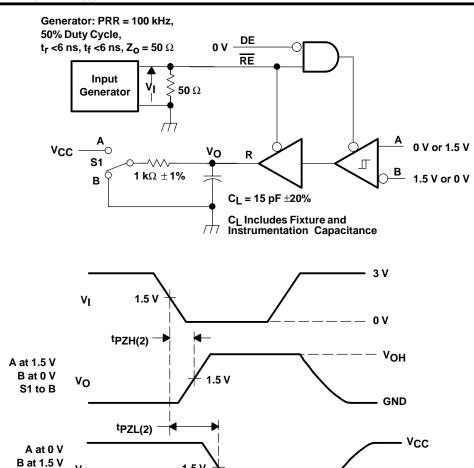


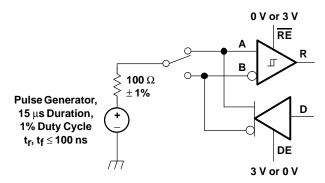
Figure 10. Receiver Enable Time From Standby (Driver Disabled)

VOL

1.5 V

۷o

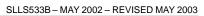
S1 to A



NOTE: This test is conducted to test survivability only. Data stability at the R output is not specified.

Figure 11. Test Circuit, Transient Over Voltage Test







### **FUNCTION TABLES**

### DRIVER

INPUT	ENABLE	OUT	PUTS
D	DE	Α	В
Н	Н	Н	L
L	Н	L	Н
X	L	Z	Z
Open X	Н	Н	L
X	Open	Z	Z

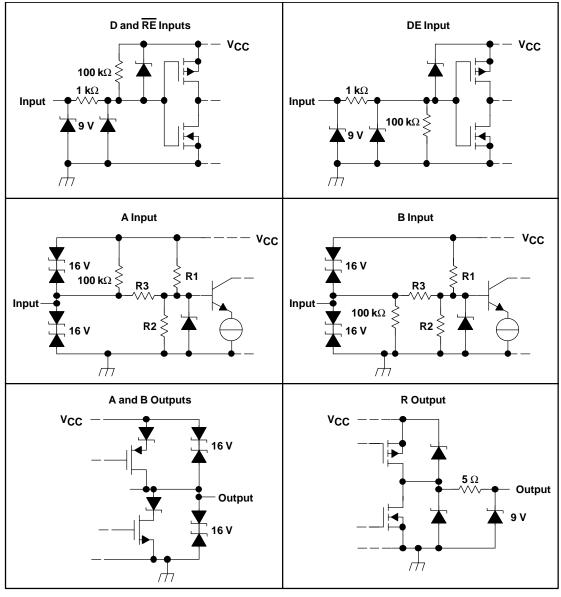
### **RECEIVER**

DIFFERENTIAL INPUTS	ENABLE	OUTPUT
$V_{ID} = V_A - V_B$	RE	R
V <sub>ID</sub> ≤ -0.2 V	L	L
$-0.2 \text{ V} < \text{V}_{\text{ID}} < -0.01 \text{ V}$	L	?
–0.01 V ≤ V <sub>ID</sub>	L	Н
X	Н	Z
Open Circuit	L	Н
Short Circuit	L	Н
X	Open	Z

H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate



# **EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS**



	R1/R2	R3
SN65HVD05	<b>9 k</b> Ω	<b>45 k</b> Ω
SN65HVD06	<b>36 k</b> Ω	<b>180 k</b> Ω
SN65HVD07	<b>36 k</b> Ω	<b>180 k</b> Ω

HVD06



### TYPICAL CHARACTERISTICS

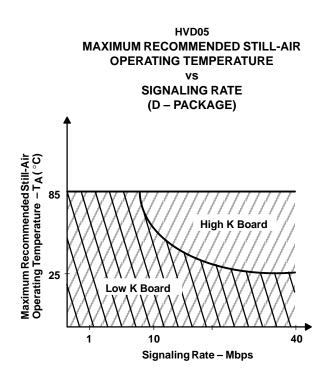
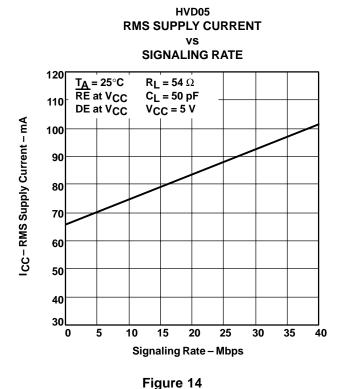


Figure 12



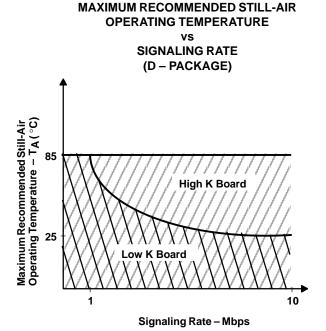


Figure 13

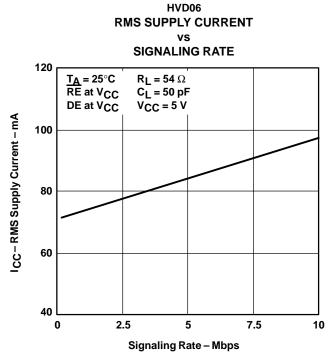


Figure 15





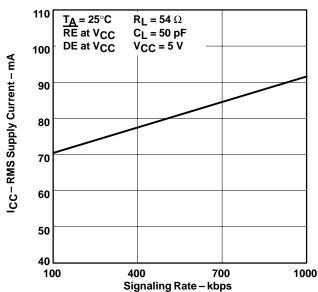


Figure 16

# DRIVER HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

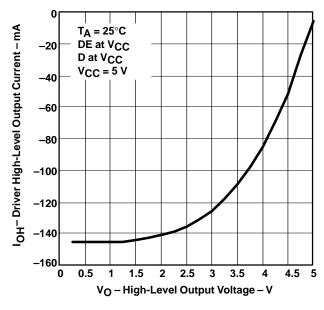


Figure 18

# BUS INPUT CURRENT vs BUS INPUT VOLTAGE

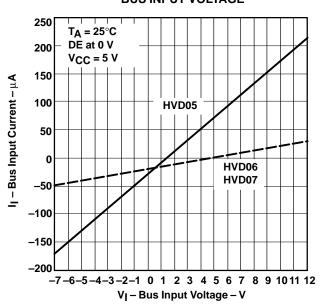


Figure 17

# DRIVER LOW-LEVEL OUTPUT CURRENT vs

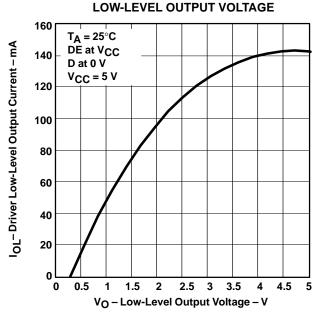
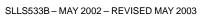
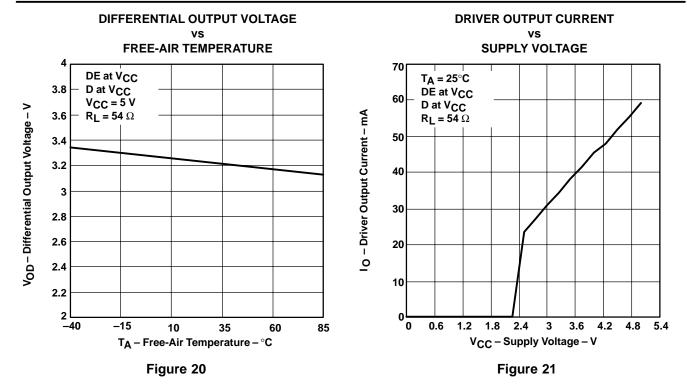
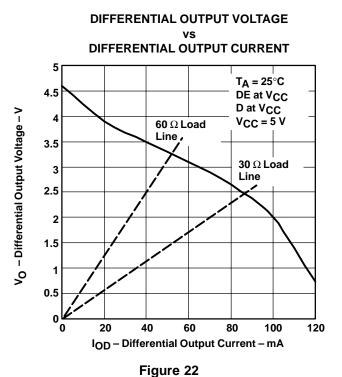


Figure 19



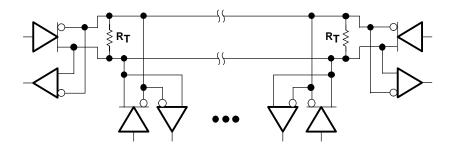








## **APPLICATION INFORMATION**



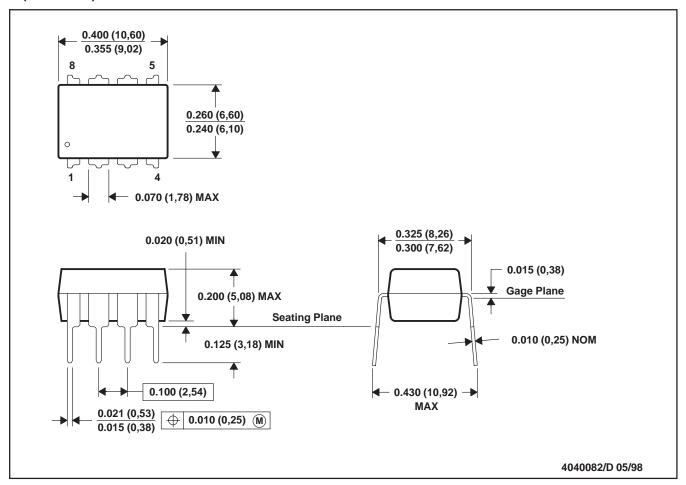
Device	Number of Devices on Bus
HVD05	64
HVD06	256
HVD07	256

NOTE: The line should be terminated at both ends with its characteristic impedance (R<sub>T</sub> = Z<sub>O</sub>). Stub lengths off the main line should be kept as short as possible.

Figure 23. Typical Application Circuit

### P (R-PDIP-T8)

### PLASTIC DUAL-IN-LINE



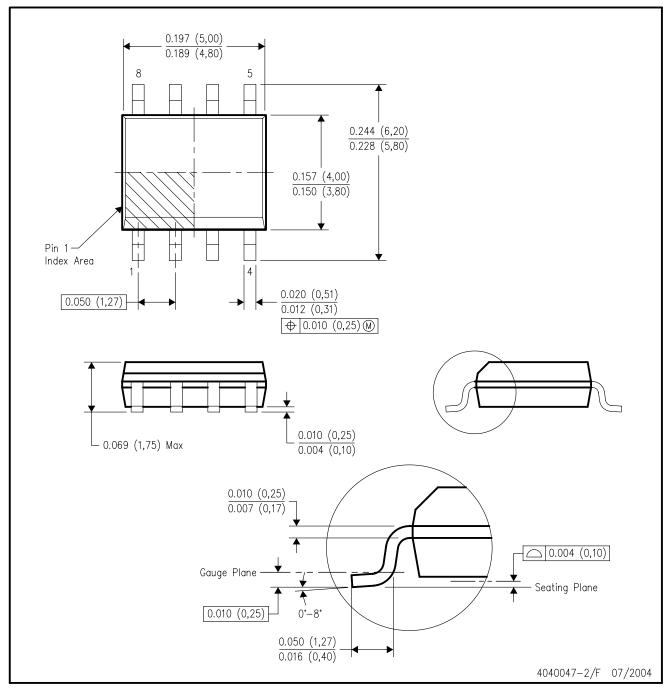
NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001



# D (R-PDSO-G8)

# PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012 variation AA.



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Post Office Box 655303 Dallas, Texas 75265