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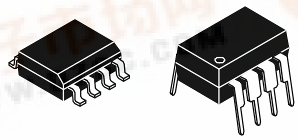


SN65HVD05, SN65HVD06, SN65HVD07
SN75HVD05, SN75HVD06, SN75HVD07

SLLS533B – MAY 2002 – REVISED MAY 2003

HIGH OUTPUT RS-485 TRANSCEIVERS

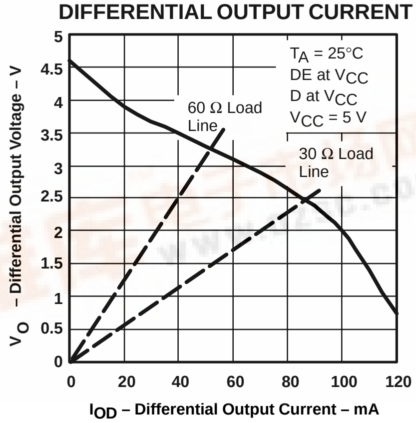
FEATURES

- **Minimum Differential Output Voltage of 2.5 V Into a 54-Ω Load**
- **Open-Circuit, Short-Circuit, and Idle-Bus Failsafe Receiver**
- **1/8th Unit-Load Option Available (Up to 256 Nodes on the Bus)**
- **Bus-Pin ESD Protection Exceeds 16 kV HBM**
- **Driver Output Slew Rate Control Options**
- **Electrically Compatible With ANSI TIA/EIA-485-A Standard**
- **Low-Current Standby Mode . . . 1 µA Typical**
- **Glitch-Free Power-Up and Power-Down Protection for Hot-Plugging Applications**
- **Pin Compatible With Industry Standard SN75176**

APPLICATIONS

- **Data Transmission Over Long or Lossy Lines or Electrically Noisy Environments**
- **Profibus Line Interface**
- **Industrial Process Control Networks**
- **Point-of-Sale (POS) Networks**
- **Electric Utility Metering**
- **Building Automation**
- **Digital Motor Control**

DIFFERENTIAL OUTPUT VOLTAGE vs DIFFERENTIAL OUTPUT CURRENT

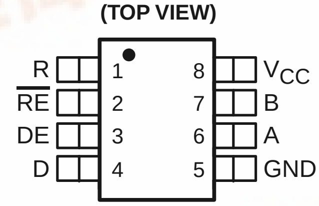


DESCRIPTION

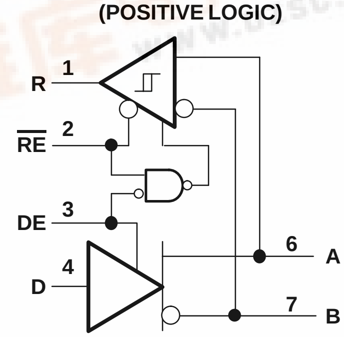
The SN65HVD05, SN75HVD05, SN65HVD06, SN75HVD06, SN65HVD07, and SN75HVD07 combine a 3-state differential line driver and differential line receiver. They are designed for balanced data transmission and interoperate with ANSI TIA/EIA-485-A and ISO 8482E standard-compliant devices. The driver is designed to provide a differential output voltage greater than that required by these standards for increased noise margin. The drivers and receivers have active-high and active-low enables respectively, which can be externally connected together to function as direction control.

The driver differential outputs and receiver differential inputs connect internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or not powered. These devices feature wide positive and negative common-mode voltage ranges, making them suitable for party-line applications.

D OR P PACKAGE (TOP VIEW)



LOGIC DIAGRAM (POSITIVE LOGIC)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

SIGNALING RATE	UNIT LOAD	DRIVER OUTPUT SLOPE CONTROL	T_A	PART NUMBER(2)		MARKED AS	
						PLASTIC DUAL-IN-LINE PACKAGE (PDIP)	SMALL OUTLINE IC (SOIC) PACKAGE
40 Mbps	1/2	No	–40°C to 85°C	SN65HVD05D	SN65HVD05P	65HVD05	VP05
10 Mbps	1/8	Yes		SN65HVD06D	SN65HVD06P	65HVD06	VP06
1 Mbps	1/8	Yes		SN65HVD07D	SN65HVD07P	65HVD07	VP07
40 Mbps	1/2	No	–0°C to 70°C	SN75HVD05D	SN75HVD05P	75HVD05	VN05
10 Mbps	1/8	Yes		SN75HVD06D	SN75HVD06P	75HVD06	VN06
1 Mbps	1/8	Yes		SN75HVD07D	SN75HVD07P	75HVD07	VN07

(1) For the most current specification and package information, refer to our web site at www.ti.com.
(2) The D package is available taped and reeled. Add an R suffix to the device type (i.e., SN65HVD05DR).

PACKAGE DISSIPATION RATINGS (SEE FIGURE 12 AND FIGURE 13)

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D(2)	710 mW	5.7 mW/°C	455 mW	369 mW
D(3)	1282 mW	10.3 mW/°C	821 mW	667 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(2) Tested in accordance with the Low-K thermal metric definitions of EIA/JESD51-3
(3) Tested in accordance with the High-K thermal metric definitions of EIA/JESD51-7

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1) (2)

			SN65HVD05, SN65HVD06, SN65HVD07 SN75HVD05, SN75HVD06, SN75HVD07
Supply voltage range, V_{CC}			–0.3 V to 6 V
Voltage range at A or B			–9 V to 14 V
Input voltage range at D, DE, R or $\overline{RE}$			–0.5 V to V_{CC} + 0.5 V
Voltage input range, transient pulse, A and B, through 100 Ω (see Figure 11)			–50 V to 50 V
Electrostatic discharge	Human body model(3)	A, B, and GND	16 kV
		All pins	4 kV
	Charged-device model(4)	All pins	1 kV
Continuous total power dissipation			See Dissipation Rating Table
Storage temperature range, T_{stg}			–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5		5.5	V
Voltage at any bus terminal (separately or common mode) V_I or V_{IC}		–7(1)		12	V
High-level input voltage, V_{IH}	D, DE, $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Figure 7)		–12		12	V
High-level output current, I_{OH}	Driver	–100			mA
	Receiver	–8			mA
Low-level output current, I_{OL}	Driver			100	mA
	Receiver			8	mA
Operating free-air temperature, T_A	SN65HVD05	–40		85	°C
	SN65HVD06				
	SN65HVD07				
	SN75HVD05	0		70	°C
	SN75HVD06				
	SN75HVD07				

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

DRIVER ELECTRICAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted(1)

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = –18 mA		–1.5			V
$\|V_{OD}\|$	Differential output voltage		No Load				V_{CC}	V
			R_L = 54 Ω, See Figure 1		2.5			V
			V_{test} = –7 V to 12 V, See Figure 2		2.2			V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage		See Figure 1 and Figure 2		–0.2		0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage		See Figure 3		2.2		3.3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage		See Figure 3		–0.1		0.1	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	HVD05	See Figure 3			600		mV
		HVD06				500		mV
		HVD07				900		mV
I_{OZ}	High-impedance output current		See receiver input currents					
I_I	Input current	D			–100		0	µA
		DE			0		100	µA
I_{OS}	Short-circuit output current		–7 V ≤ V_O ≤ 12 V		–250		250	mA
$C_{(diff)}$	Differential output capacitance		V_{ID} = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V			16		pF
I_{CC}	Supply current		$\overline{RE}$ at V_{CC}, D & DE at V_{CC}, No load	Receiver disabled and driver enabled		9	15	mA
			$\overline{RE}$ at V_{CC}, D at V_{CC} DE at 0 V, No load	Receiver disabled and driver disabled (standby)		1	5	µA
			$\overline{RE}$ at 0 V, D & DE at V_{CC}, No load	Receiver enabled and driver enabled		9	15	mA

(1) All typical values are at 25°C and with a 5-V supply.

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DRIVER SWITCHING CHARACTERISTICS NIL

over operating free-air temperature range unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	HVD05	R_L = 54 Ω, C_L = 50 pF, See Figure 4		6.5	11	ns
		HVD06			27	40	
		HVD07			250	400	
t_{PHL}	Propagation delay time, high-to-low-level output	HVD05			6.5	11	ns
		HVD06			27	40	
		HVD07			250	400	
t_r	Differential output signal rise time	HVD05		2.7	3.6	6	ns
		HVD06		18	28	55	
		HVD07		150	300	450	
t_f	Differential output signal fall time	HVD05		2.7	3.6	6	ns
		HVD06		18	28	55	
		HVD07		150	300	450	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	HVD05				2	ns
		HVD06				2.5	
		HVD07				10	
$t_{sk(pp)}$(2)	Part-to-part skew	HVD05				3.5	ns
		HVD06				14	
		HVD07				100	
t_{PZH1}	Propagation delay time, high-impedance-to-high-level output	HVD05	$\overline{RE}$ at 0 V, R_L = 110 Ω, See Figure 5			25	ns
		HVD06				45	
		HVD07				250	
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	HVD05				25	ns
		HVD06				60	
		HVD07				250	
t_{PZL1}	Propagation delay time, high-impedance-to-low-level output	HVD05	$\overline{RE}$ at 0 V, R_L = 110 Ω, See Figure 6			15	ns
		HVD06				45	
		HVD07				200	
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output	HVD05				14	ns
		HVD06				90	
		HVD07				550	
t_{PZH2}	Propagation delay time, standby-to-high-level output		R_L = 110 Ω, $\overline{RE}$ at 3 V, See Figure 5			6	µs
t_{PZL2}	Propagation delay time, standby-to-low-level output		R_L = 110 Ω, $\overline{RE}$ at 3 V, See Figure 6			6	µs

(1) All typical values are at 25°C and with a 5-V supply.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

RECEIVER ELECTRICAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		I_O = –8 mA				–0.01	V
$V_{IT–}$	Negative-going input threshold voltage		I_O = 8 mA		–0.2			V
V_{hys}	Hysteresis voltage (V_{IT+} – $V_{IT–}$)					35		mV
V_{IK}	Enable-input clamp voltage		I_I = –18 mA		–1.5			V
V_{OH}	High-level output voltage		V_{ID} = 200 mV, I_{OH} = –8 mA, See Figure 7		4			V
V_{OL}	Low-level output voltage		V_{ID} = –200 mV, I_{OL} = 8 mA, See Figure 7				0.4	V
I_{OZ}	High-impedance-state output current		V_O = 0 or V_{CC} $\overline{RE}$ at V_{CC}		–1		1	µA
I_I	Bus input current	HVD05	Other input at 0 V	V_A or V_B = 12 V		0.23	0.5	mA
				V_A or V_B = 12 V, V_{CC} = 0 V		0.3	0.5	
				V_A or V_B = –7 V	–0.4	–0.13		
				V_A or V_B = –7 V, V_{CC} = 0 V	–0.4	–0.15		
		HVD06, HVD07	Other input at 0 V	V_A or V_B = 12 V		0.06	0.1	mA
				V_A or V_B = 12 V, V_{CC} = 0 V		0.08	0.13	
				V_A or V_B = –7 V	–0.1	–0.05		
				V_A or V_B = –7 V, V_{CC} = 0 V	–0.05	–0.03		
I_{IH}	High-level input current, $\overline{RE}$		V_{IH} = 2 V		–60	–26.4		µA
I_{IL}	Low-level input current, $\overline{RE}$		V_{IL} = 0.8 V		–60	–27.4		µA
$C_{(diff)}$	Differential input capacitance		V_I = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V			16		pF
I_{CC}	Supply current		$\overline{RE}$ at 0 V, D & DE at 0 V, No load	Receiver enabled and driver disabled		5	10	mA
			$\overline{RE}$ at V_{CC}, DE at 0 V, D at V_{CC}, No load	Receiver disabled and driver disabled (standby)		1	5	µA
			$\overline{RE}$ at 0 V, D & DE at V_{CC}, No load	Receiver enabled and driver enabled		9	15	mA

(1) All typical values are at 25°C and with a 5-V supply.

RECEIVER SWITCHING CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP[(1)]	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output 1/2 UL	HVD05	V_{ID} = –1.5 V to 1.5 V, C_L = 15 pF, See Figure 8		14.6	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output 1/2 UL	HVD05			14.6	25	ns
t_{PLH}	Propagation delay time, low-to-high-level output 1/8 UL	HVD06			55	70	ns
		HVD07			55	70	
t_{PHL}	Propagation delay time, high-to-low-level output 1/8 UL	HVD06			55	70	ns
		HVD07			55	70	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} – t_{PLH}\|$)	HVD05				2	ns
		HVD06				4.5	
		HVD07				4.5	
$t_{sk(pp)}$[(2)]	Part-to-part skew	HVD05				6.5	ns
		HVD06				14	
		HVD07				14	
t_r	Output signal rise time		C_L = 15 pF, See Figure 8		2	3	ns
t_f	Output signal fall time				2	3	
t_{PZH1}	Output enable time to high level		C_L = 15 pF, DE at 3 V, See Figure 9			10	ns
t_{PZL1}	Output enable time to low level					10	
t_{PHZ}	Output disable time from high level					15	
t_{PLZ}	Output disable time from low level					15	
t_{PZH2}	Propagation delay time, standby-to-high-level output		C_L = 15 pF, DE at 0, See Figure 10			6	µs
t_{PZL2}	Propagation delay time, standby-to-low-level output					6	

(1) All typical values are at 25°C and with a 5-V supply.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

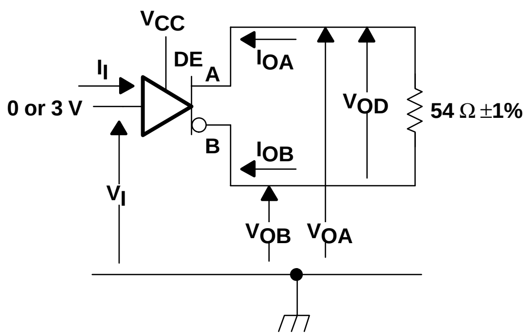


Figure 1. Driver V_{OD} Test Circuit and Voltage and Current Definitions

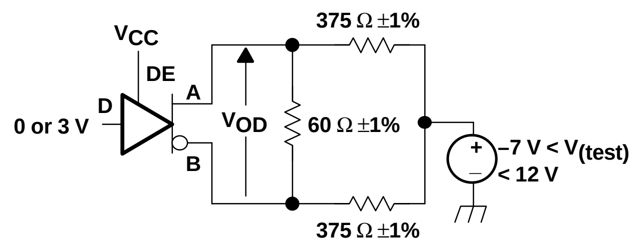
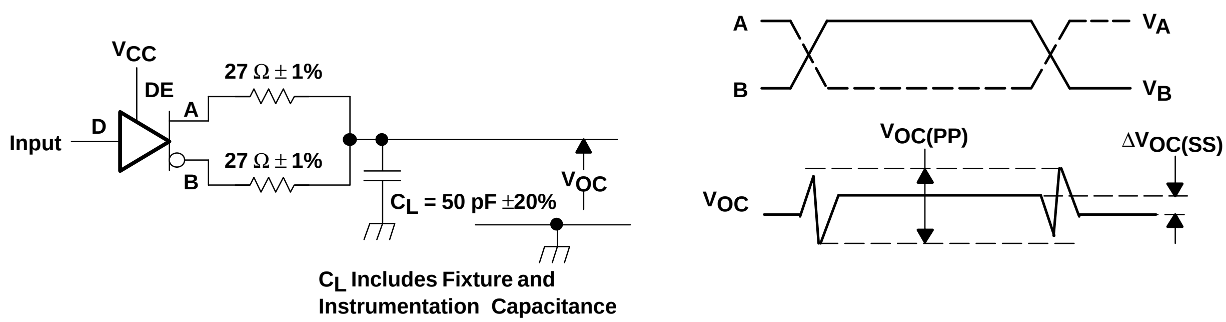
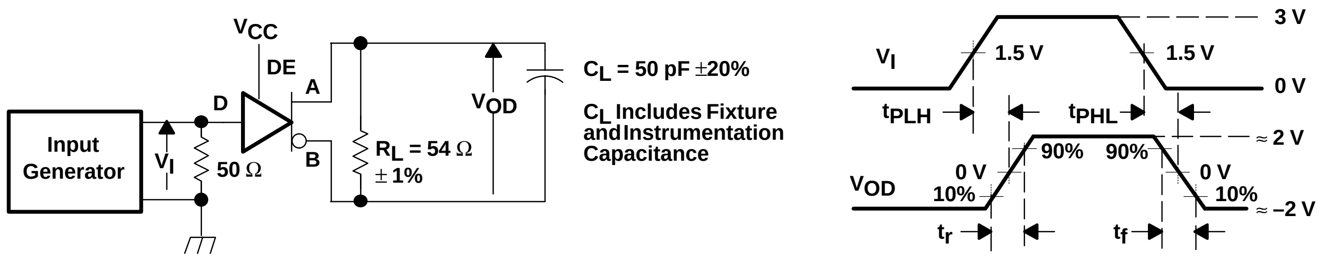


Figure 2. Driver V_{OD} With Common-Mode Loading Test Circuit



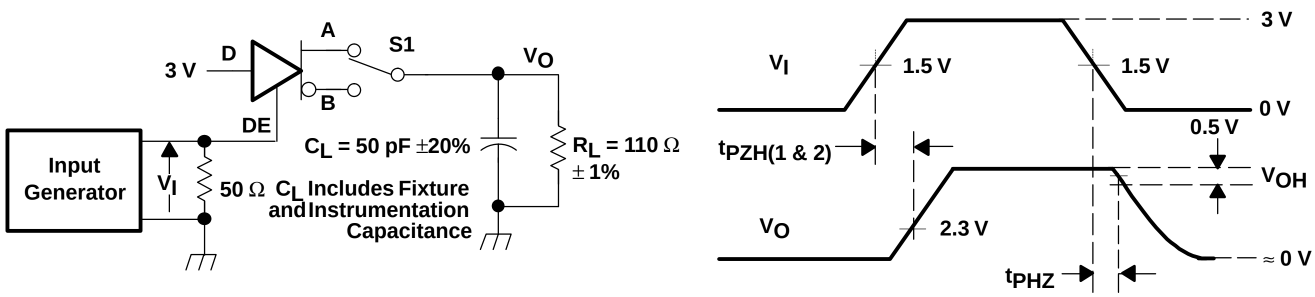
Input: PRR = 500 kHz, 50% Duty Cycle, t_r<6ns, t_f<6ns, Z_O = 50 Ω

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



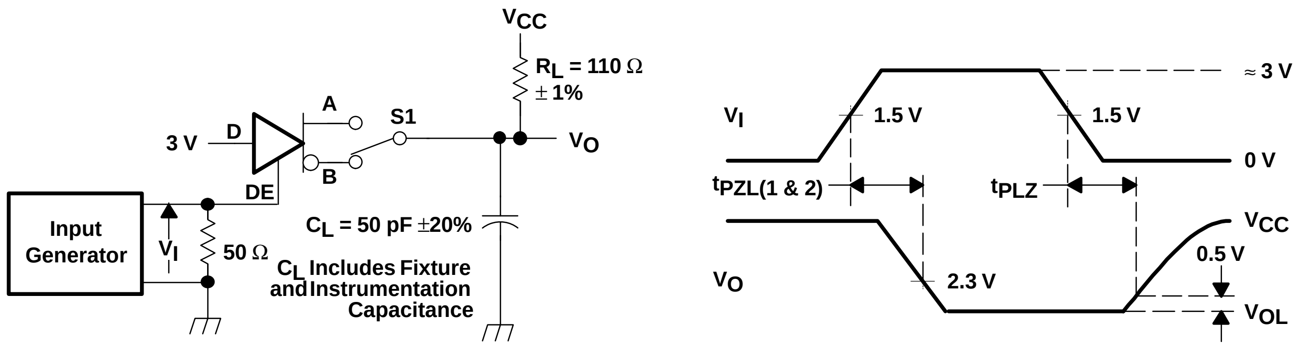
Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_O = 50 Ω

Figure 4. Driver Switching Test Circuit and Voltage Waveforms



Generator: PRR = 100 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_O = 50 Ω

Figure 5. Driver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms



Generator: PRR = 100 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_O = 50 Ω

Figure 6. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

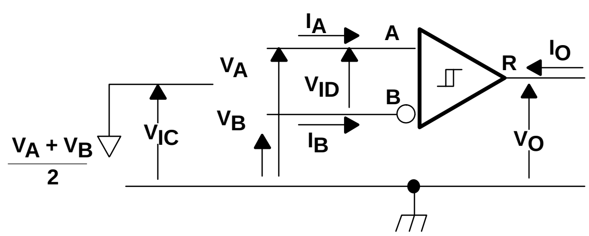
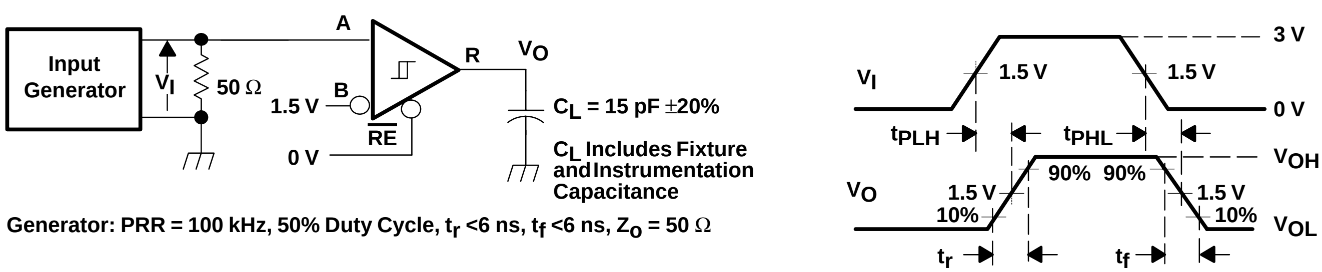


Figure 7. Receiver Voltage and Current Definitions



Generator: PRR = 100 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_O = 50 Ω

Figure 8. Receiver Switching Test Circuit and Voltage Waveforms

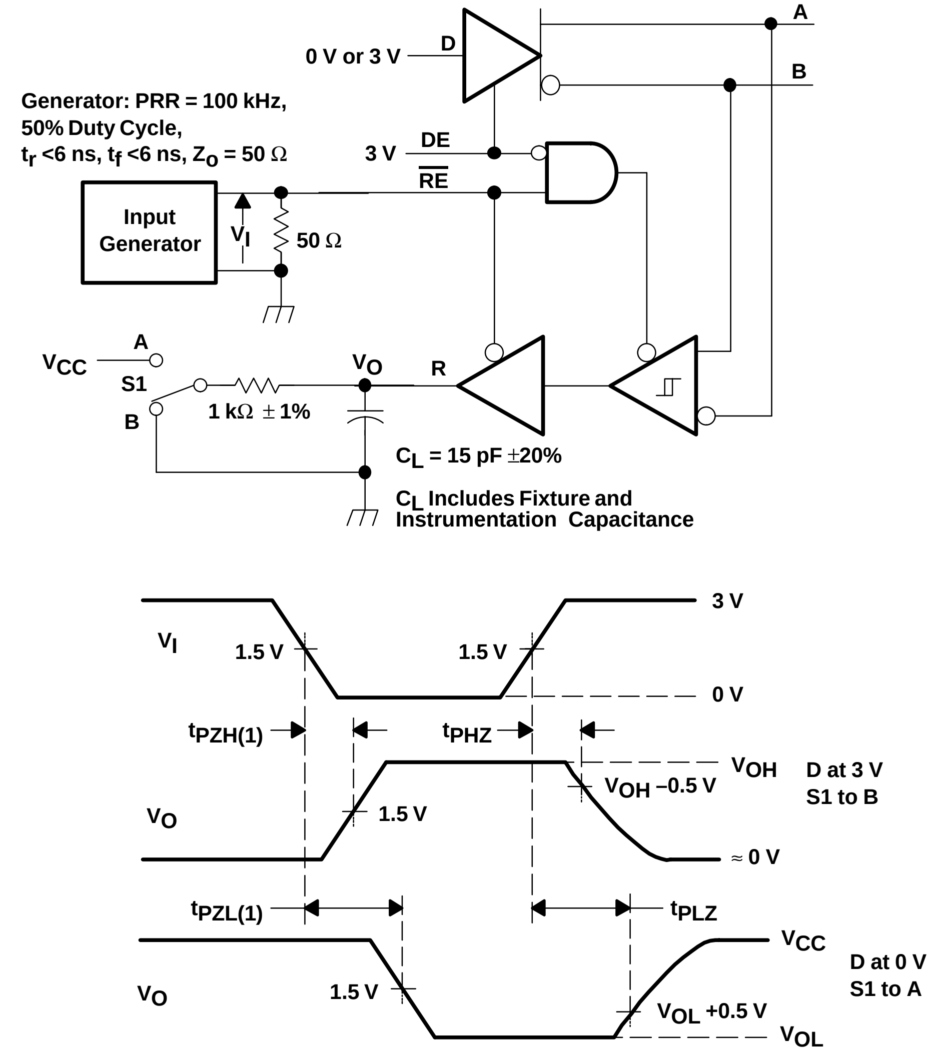


Figure 9. Receiver Enable and Disable Time Test Circuit and Voltage Waveforms With Drivers Enabled

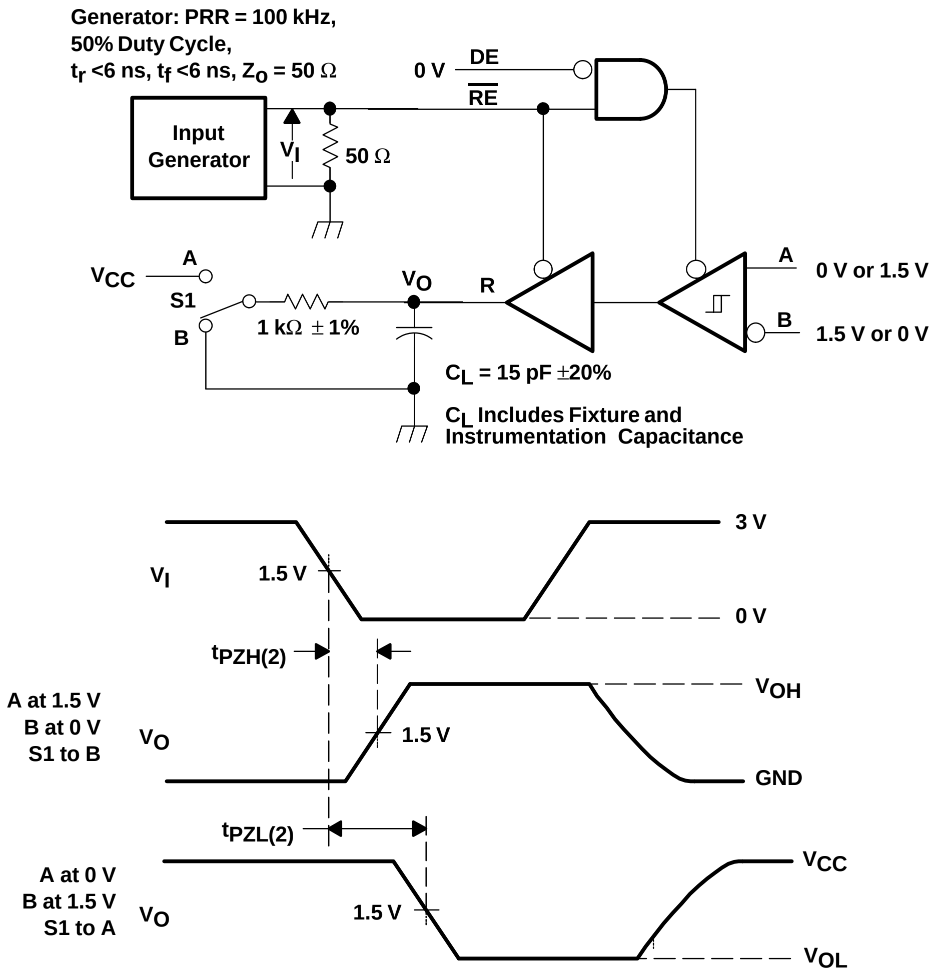
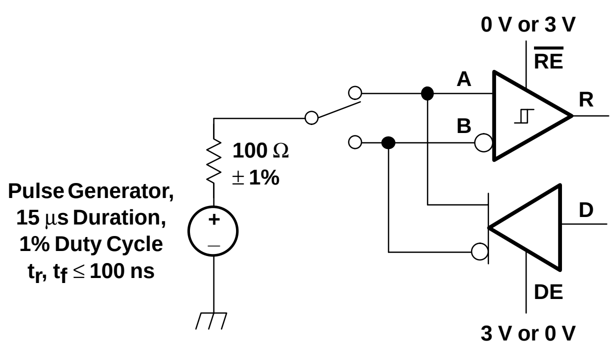


Figure 10. Receiver Enable Time From Standby (Driver Disabled)



NOTE: This test is conducted to test survivability only. Data stability at the R output is not specified.

Figure 11. Test Circuit, Transient Over Voltage Test

FUNCTION TABLES

DRIVER

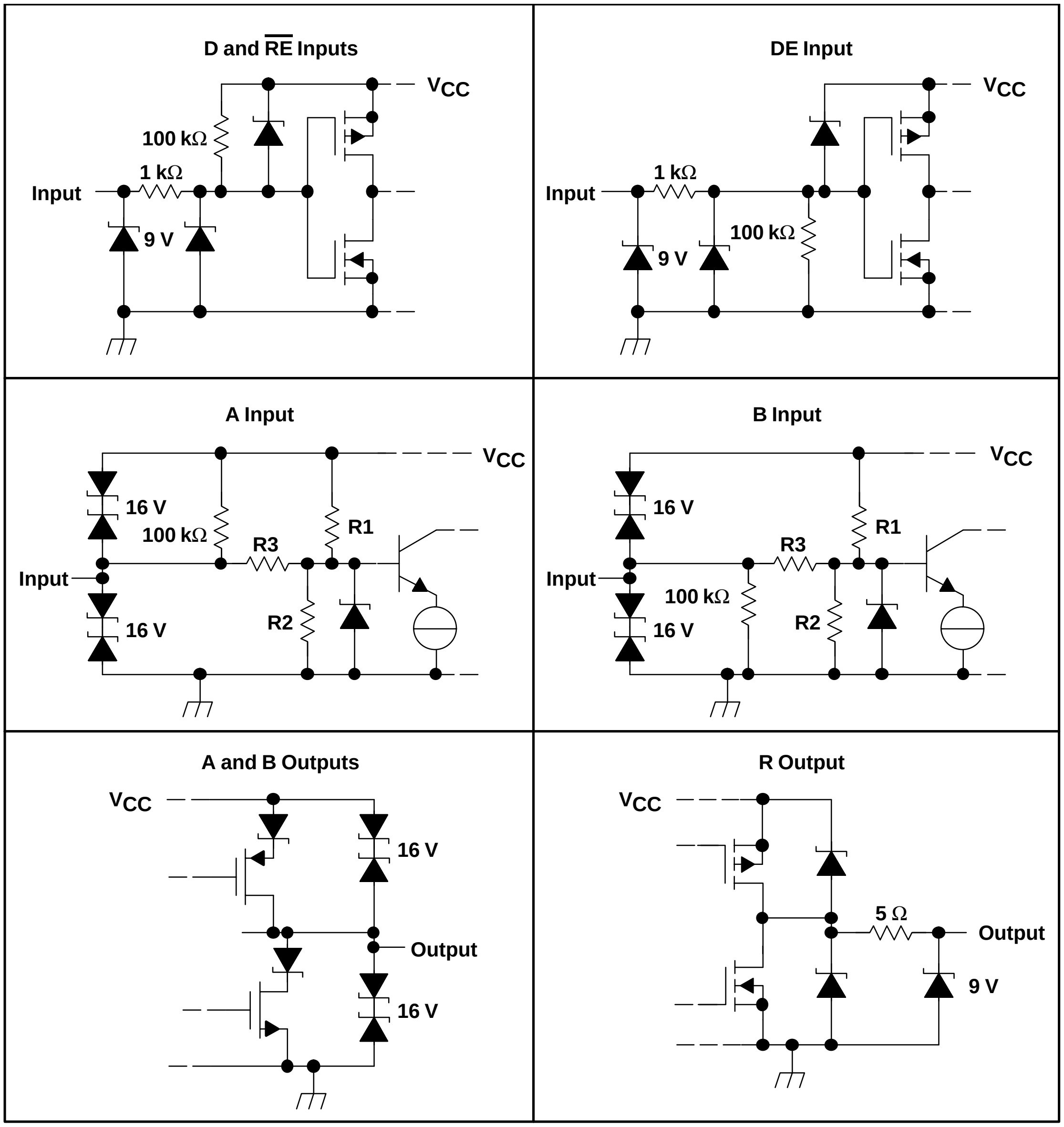
INPUT D	ENABLE DE	OUTPUTS A	OUTPUTS B
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	H	L
X	Open	Z	Z

RECEIVER

DIFFERENTIAL INPUTS $V_{ID} = V_A - V_B$	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \le -0.2$ V	L	L
-0.2 V $< V_{ID} < -0.01$ V	L	?
-0.01 V $\le V_{ID}$	L	H
X	H	Z
Open Circuit	L	H
Short Circuit	L	H
X	Open	Z

H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



	R1/R2	R3
SN65HVD05	9 kΩ	45 kΩ
SN65HVD06	36 kΩ	180 kΩ
SN65HVD07	36 kΩ	180 kΩ

TYPICAL CHARACTERISTICS

HVD05
MAXIMUM RECOMMENDED STILL-AIR OPERATING TEMPERATURE
vs
SIGNALING RATE
(D – PACKAGE)

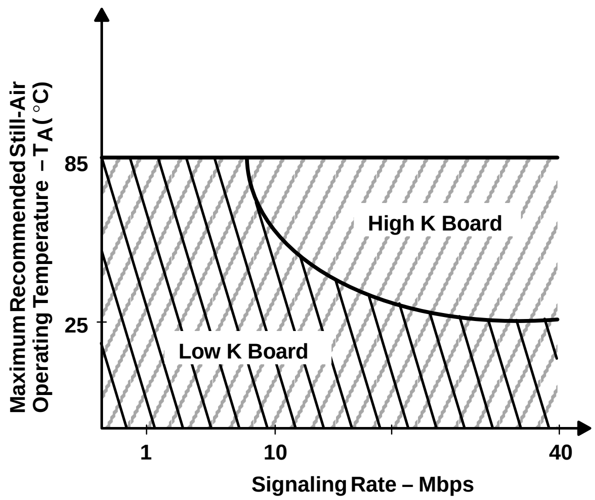


Figure 12

HVD06
MAXIMUM RECOMMENDED STILL-AIR OPERATING TEMPERATURE
vs
SIGNALING RATE
(D – PACKAGE)

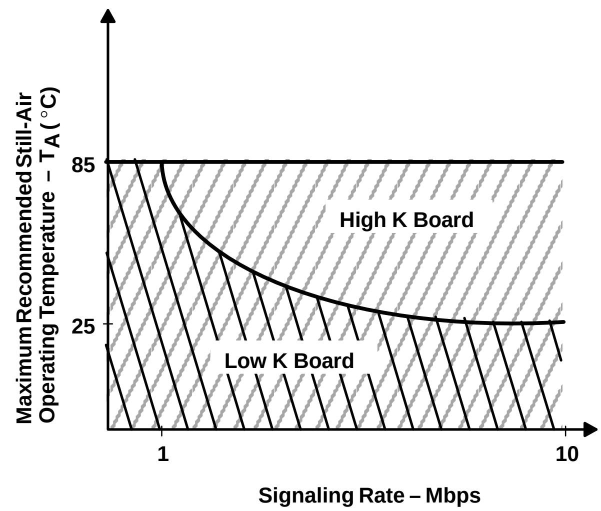


Figure 13

HVD05
RMS SUPPLY CURRENT
vs
SIGNALING RATE

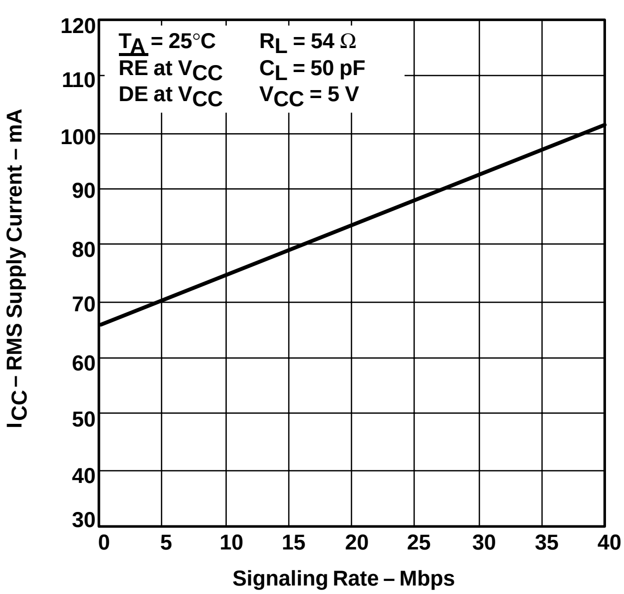


Figure 14

HVD06
RMS SUPPLY CURRENT
vs
SIGNALING RATE

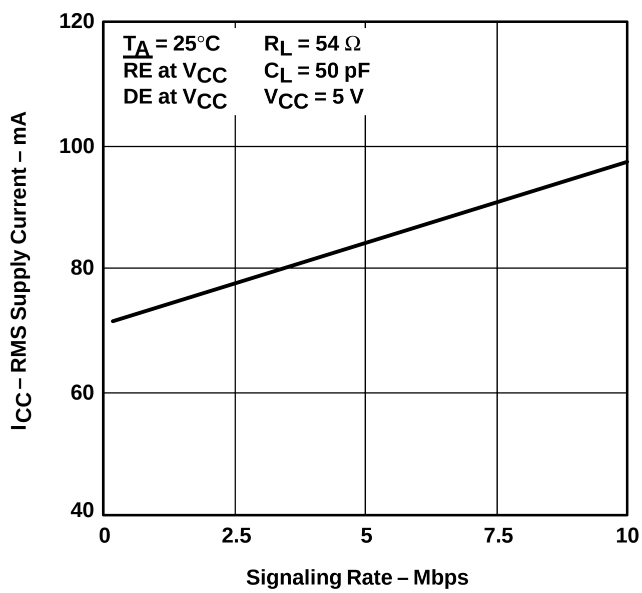


Figure 15

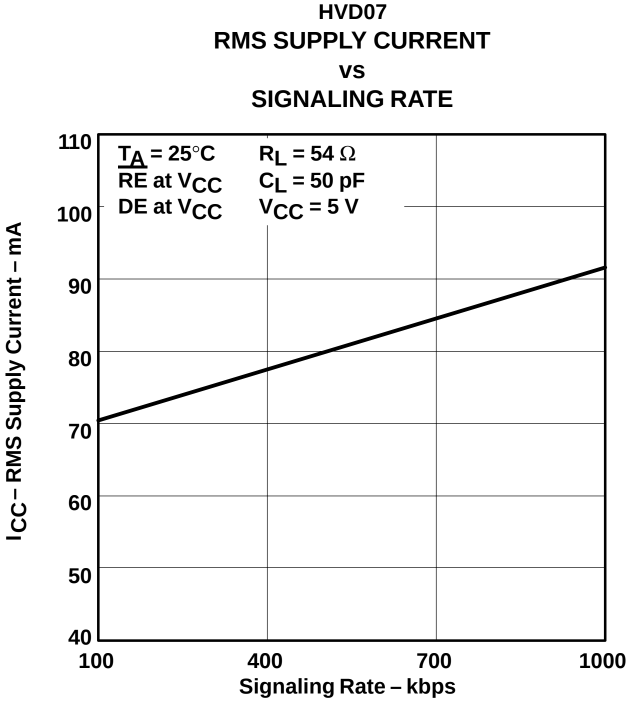


Figure 16

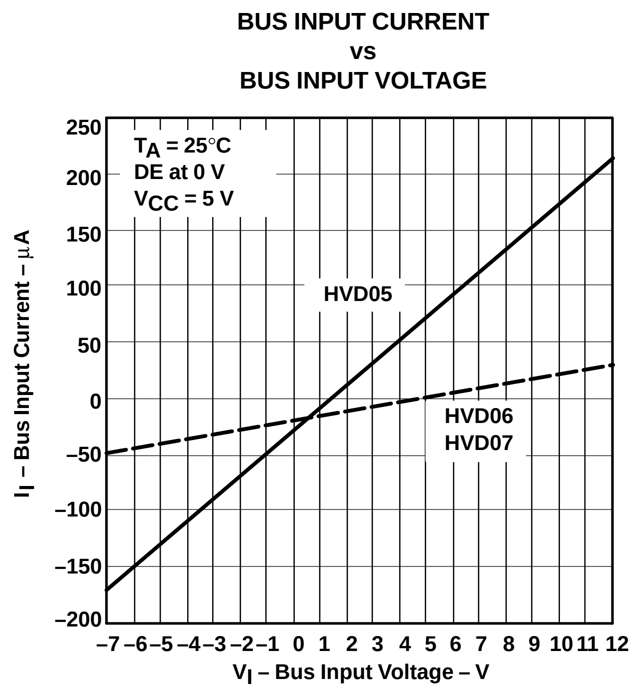


Figure 17

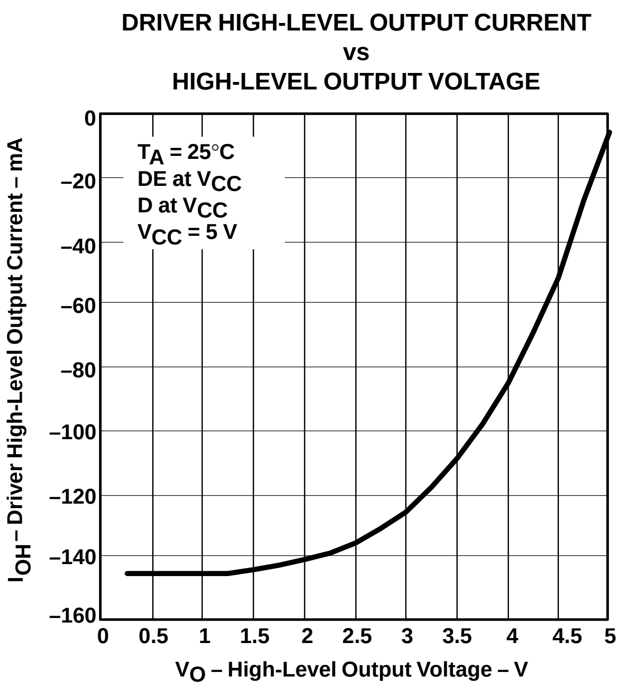


Figure 18

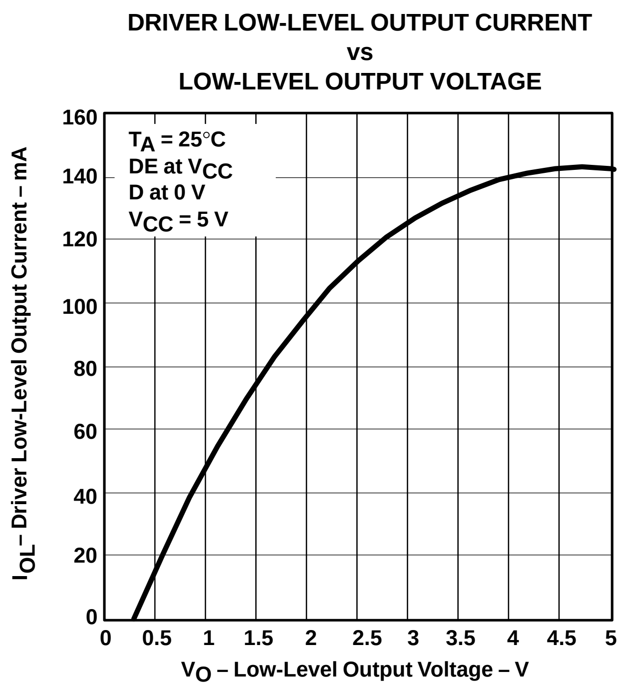


Figure 19

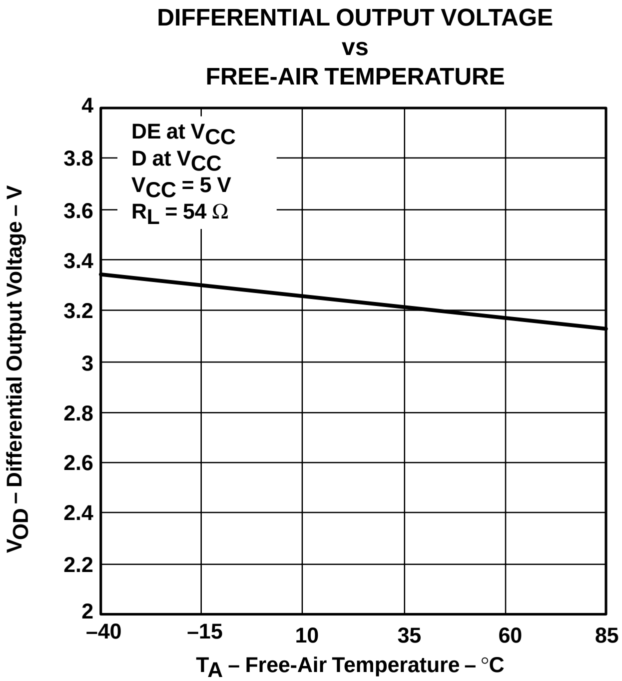


Figure 20

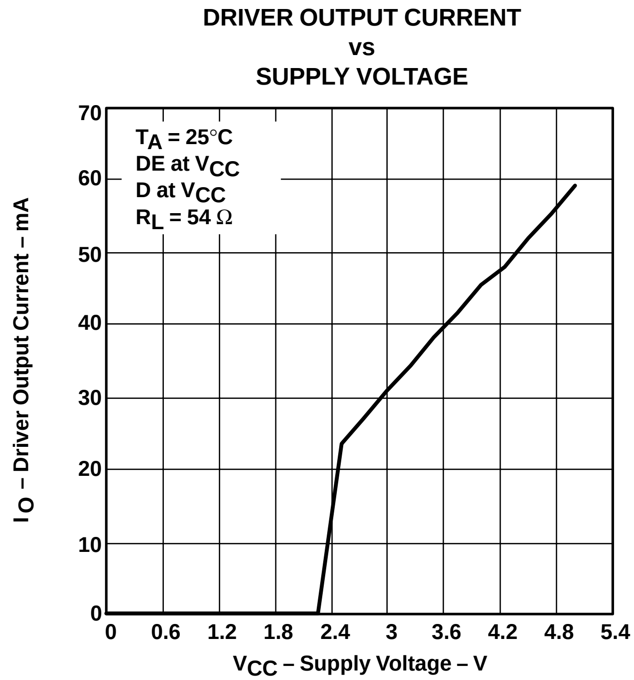


Figure 21

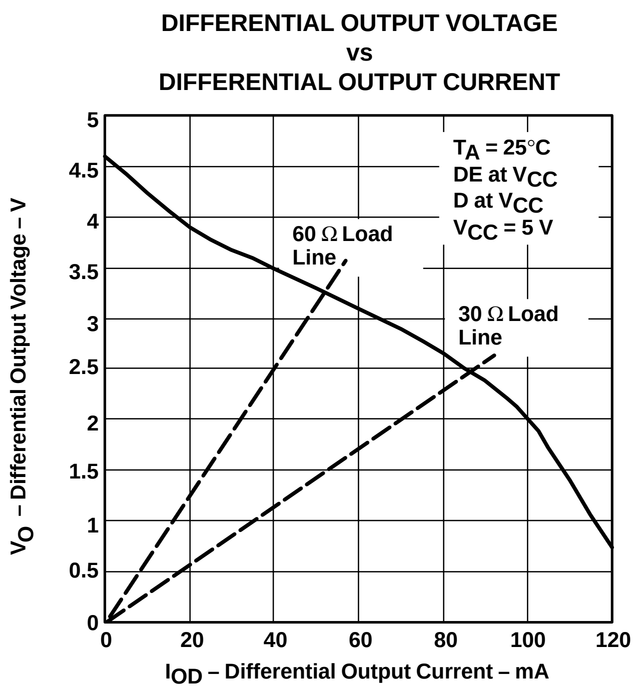
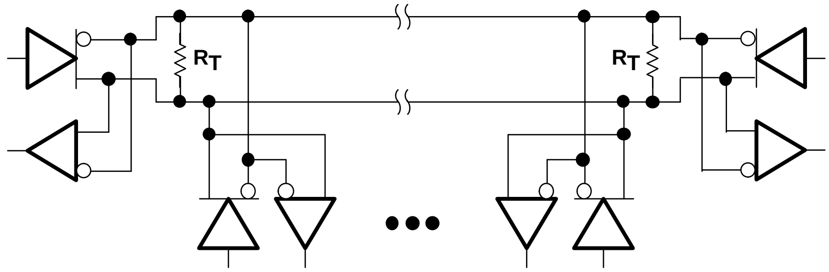


Figure 22

APPLICATION INFORMATION

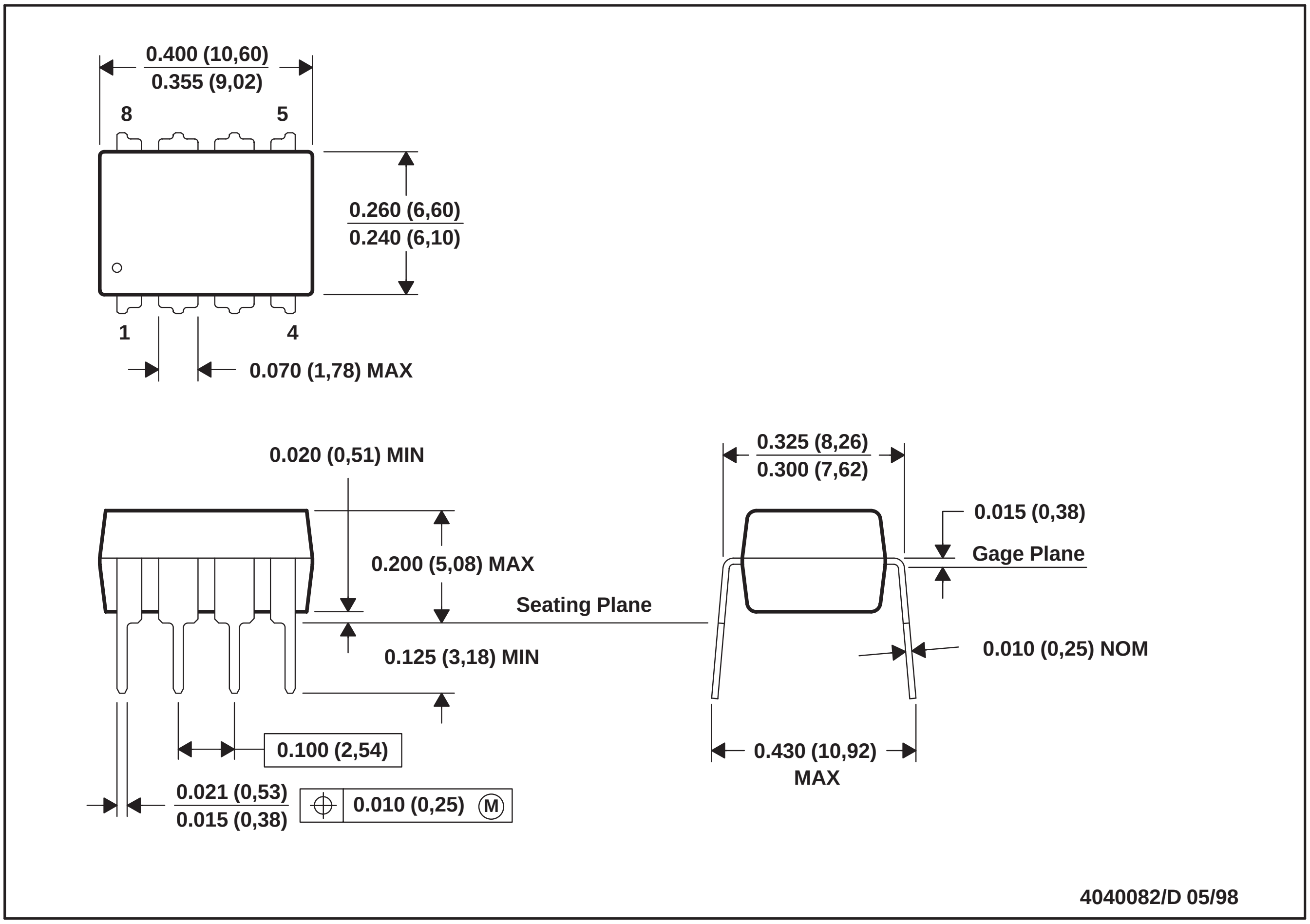


Device	Number of Devices on Bus
HVD05	64
HVD06	256
HVD07	256

NOTE: The line should be terminated at both ends with its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

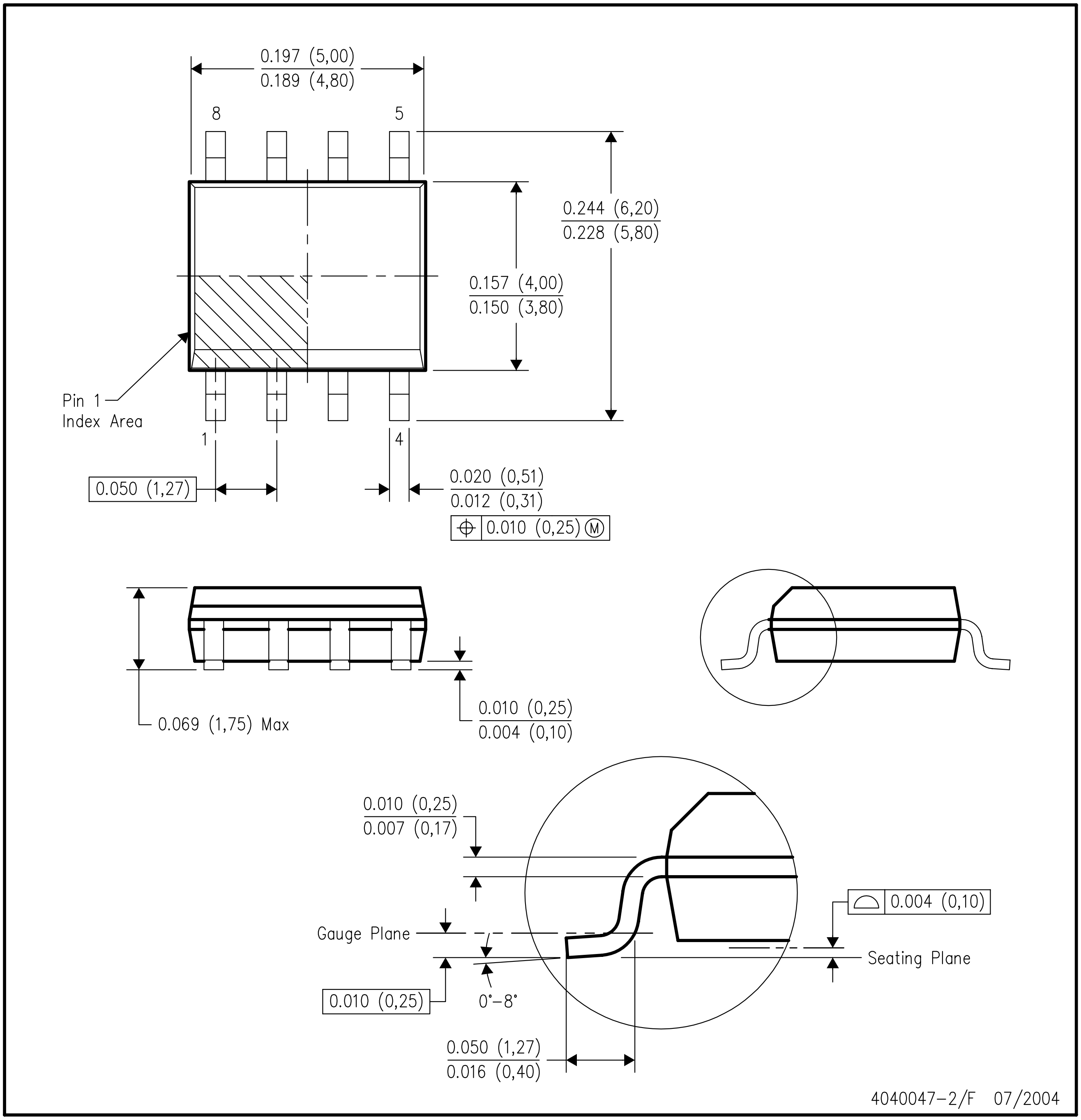
Figure 23. Typical Application Circuit

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS–012 variation AA.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

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Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
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