

QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVERS

SLLS162A – JULY 1993 – REVISED NOVEMBER 1998

- Meets or Exceeds the Standard EIA-485
- Designed for High-Speed Multipoint Transmission on Long Bus Lines in Noisy Environments
- Supports Data Rates up to and Exceeding Ten Million Transfers Per Second
- Common-Mode Output Voltage Range of -7 V to 12 V
- Positive- and Negative-Current Limiting
- Low Power Consumption . . . 1.5 mA Max (Output Disabled)
- Functionally Interchangeable With SN75174

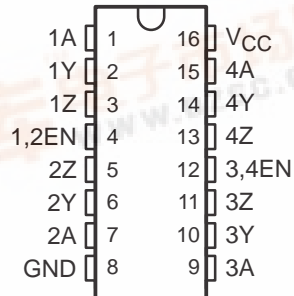
description

The SN65LBC174 and SN75LBC174 are monolithic, quadruple, differential line drivers with 3-state outputs. Both devices are designed to meet the requirements of the Electronics Industry Association Standard EIA-485. These devices are optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. Each driver features wide positive and negative common-mode output voltage ranges, current limiting, and thermal-shutdown protection, making it suitable for party-line applications in noisy environments. Both devices are designed using LinBiCMOS™, facilitating ultra-low power consumption and inherent robustness.

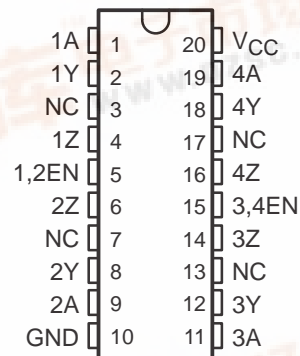
Both the SN65LBC174 and SN75LBC174 provide positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. These devices offer optimum performance when used with the SN75LBC173 or SN75LBC175 quadruple line receivers. The SN65LBC174 and SN75LBC174 are available in the 16-terminal DIP package (N) and the 20-terminal wide-body small outline intergrated circuit (SOIC) package (DW).

The SN75LBC174 is characterized for operation over the commercial temperature range of 0°C to 70°C . The SN65LBC174 is characterized over the industrial temperature range of -40°C to 85°C .

N PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each driver)

INPUT	ENABLE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = high level, L = low level,
X = irrelevant, Z = high impedance (off)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

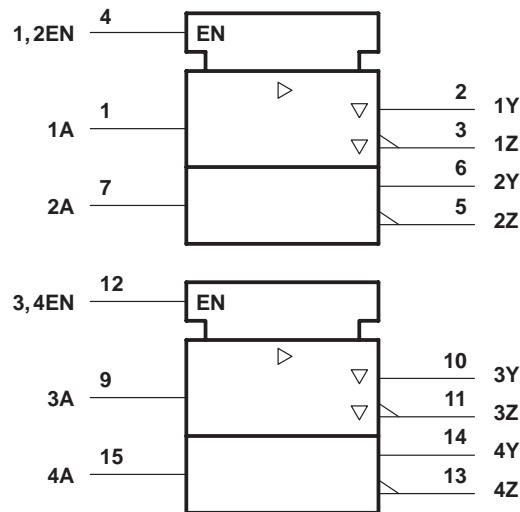


SN65LBC174, SN75LBC174

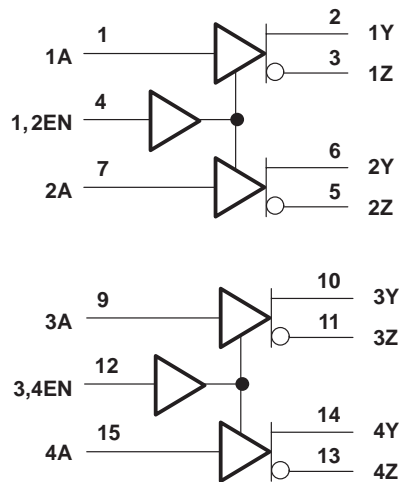
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logic symbol†

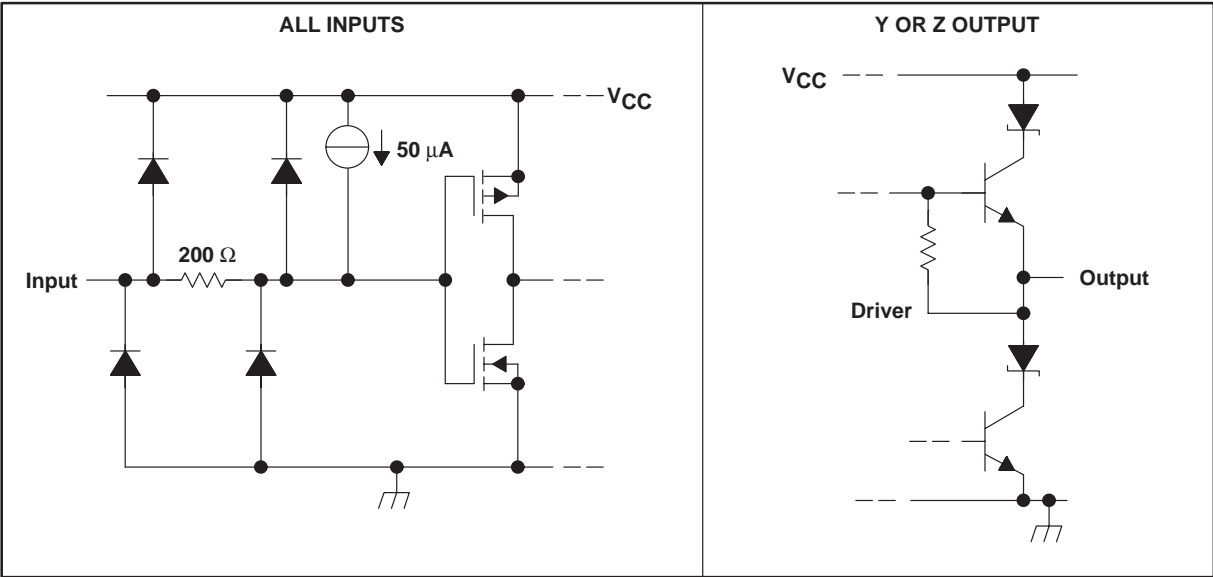


logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Terminal numbers shown are for the N package.

schematic of inputs and outputs



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absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 1)	–0.3 V to 7 V
Output voltage range, V_O	–10 V to 15 V
Input voltage range, V_I	–0.3 V to 7 V
Continuous total power dissipation	Internally limited [‡]
Operating free-air temperature range, T_A : SN65LBC174	–40°C to 85°C
SN75LBC174	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Voltage at any bus terminal (separately or common-mode), V_O	Y or Z			12	V
				–7	
High-level output current, I_{OH}	Y or Z			–60	mA
Low-level output current, I_{OL}	Y or Z			60	mA
Continuous total power dissipation		See Dissipation Rating Table			
Operating free-air temperature, T_A	SN65LBC174	–40		85	°C
	SN75LBC174	0		70	

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	585 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK} Input clamp voltage	$I_I = -18 \text{ mA}$			-1.5	V
$ V_{OD} $ Differential output voltage‡	$R_L = 54 \Omega$, See Figure 1	1.1	1.8	5	V
				5	
	$R_L = 60 \Omega$, See Figure 2	1.1	1.7	5	
				5	
$\Delta V_{OD} $ Change in magnitude of common-mode output voltage§				± 0.2	V
V_{OC} Common-mode output voltage	$R_L = 54 \Omega$, See Figure 1			3 -1	V
$\Delta V_{OC} $ Change in magnitude of common-mode output voltage§				± 0.2	V
I_O Output current with power off	$V_{CC} = 0$, $V_O = -7 \text{ V to } 12 \text{ V}$			± 100	μA
I_{OZ} High-impedance-state output current	$V_O = -7 \text{ V to } 12 \text{ V}$			± 100	μA
I_{IH} High-level input current	$V_I = 2.4 \text{ V}$			-100	μA
I_{IL} Low-level input current	$V_I = 0.4 \text{ V}$			-100	μA
I_{OS} Short-circuit output current	$V_O = -7 \text{ V to } 12 \text{ V}$			± 250	mA
I_{CC} Supply current (all drivers)	No load			7	mA
				1.5	

† All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$.

‡ The minimum V_{OD} specification does not fully comply with EIA-485 at operating temperatures below 0°C . The lower output signal should be used to determine the maximum signal transmission distance.

§ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from a high level to a low level.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(OD)}$ Differential output delay time	$R_L = 54 \Omega$, See Figure 3	2	11	20	ns
$t_{t(OD)}$ Differential output transition time		10	15	25	ns
t_{pZH} Output enable time to high level	$R_L = 110 \Omega$, See Figure 3			30	ns
t_{pZL} Output enable time to low level	$R_L = 110 \Omega$, See Figure 5			30	ns
t_{PHZ} Output disable time from high level	$R_L = 110 \Omega$, See Figure 4			50	ns
t_{PLZ} Output disable time from low level	$R_L = 110 \Omega$, See Figure 5			30	ns

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0 V or 3 V

A

EN at 5 V

V_{test}

$R1 = 375 \Omega$

$R_L = 60 \Omega$

$R2 = 375 \Omega$

V_{test}

V_{OD}

Y

Z

$-7 \text{ V} < V_{test} < 12 \text{ V}$

TEST CIRCUIT

Generator (see Note A) is connected to the Input of the inverter through a $50\ \Omega$ resistor. The inverter's output is connected to a load consisting of a resistor $R_L = 54\ \Omega$ and a capacitor $C_L = 50\ \text{pF}$ (see Note B) in parallel. The output voltage is measured across the load. A 3 V source is also connected to the inverter's input.

VOLTAGE WAVEFORMS

The Input waveform is a trapezoidal pulse with a peak value of 1.5 V and a baseline of 0 V. The Output waveform is an inverted trapezoidal pulse with a peak value of approximately 2.5 V and a baseline of approximately -2.5 V. The propagation delay $t_{d(OD)}$ is the time from the 50% input level to the 50% output level. The transition time $t_{t(OD)}$ is the time from the 10% to the 90% output level.

B. C_L includes probe and stray capacitance.

Figure 3. Time Waveforms for Driver Differential Output Test Circuit Delay and Transition

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PARAMETER MEASUREMENT INFORMATION

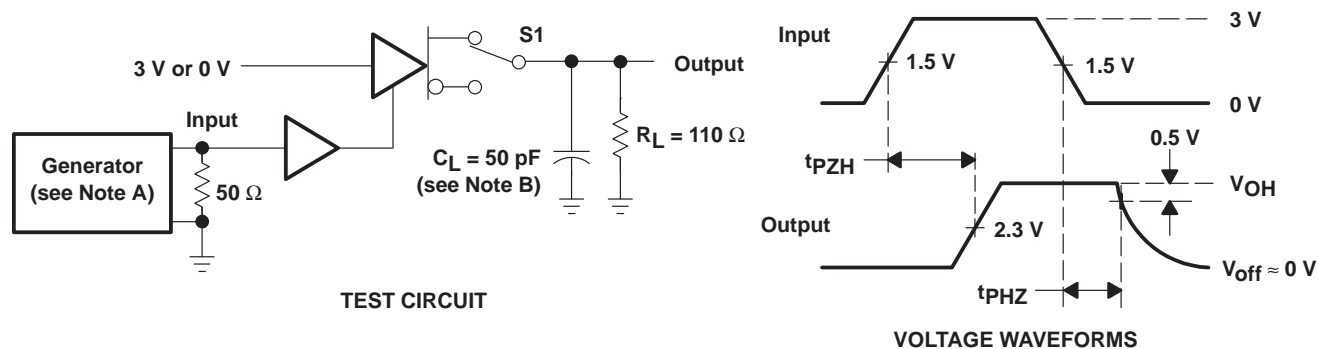
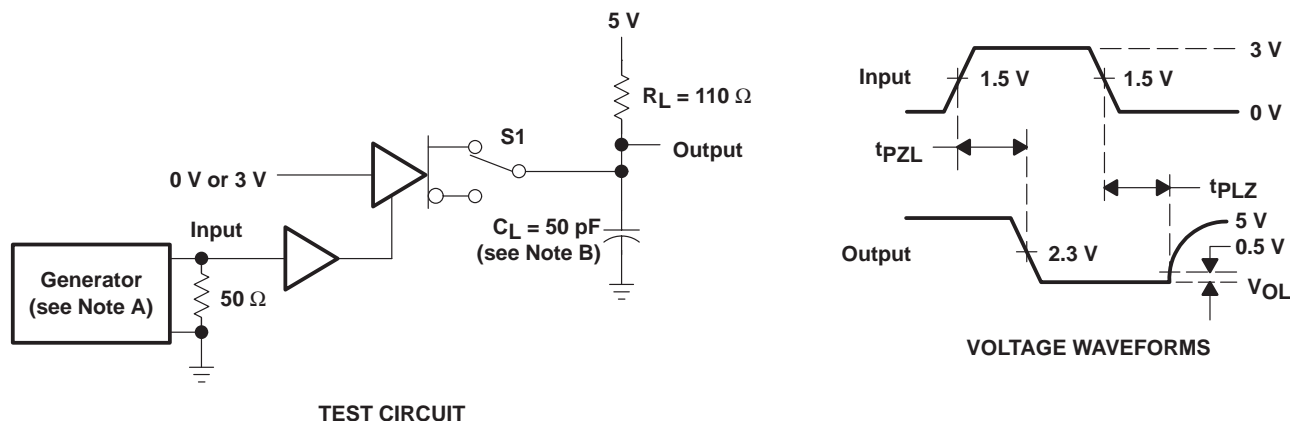


Figure 4. t_{pZH} and t_{pHZ} Test Circuit and Waveforms



TEST CIRCUIT

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, duty cycle = 50%, $t_r \leq 5$ ns, $t_f \leq 5$ ns, $Z_O = 50$ Ω .
- B. C_L includes probe and stray capacitance.

Figure 5. t_{pZL} and t_{pLZ} Test Circuit and Waveforms

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TYPICAL CHARACTERISTICS

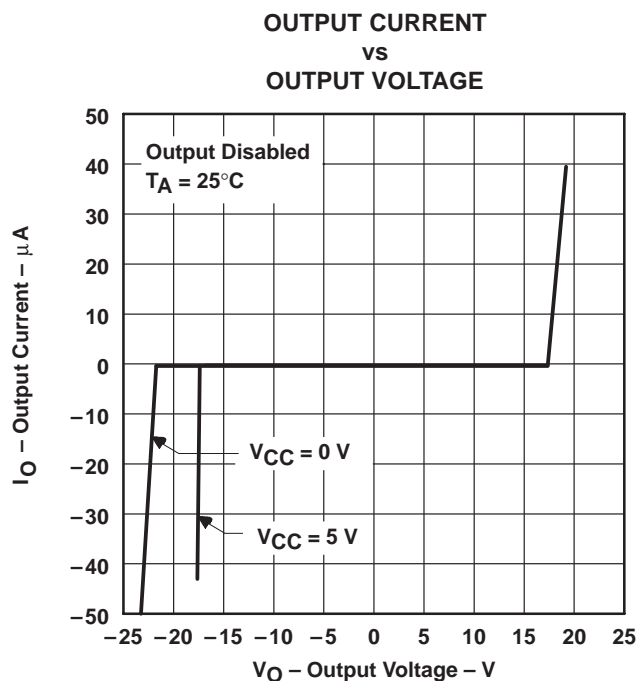


Figure 6

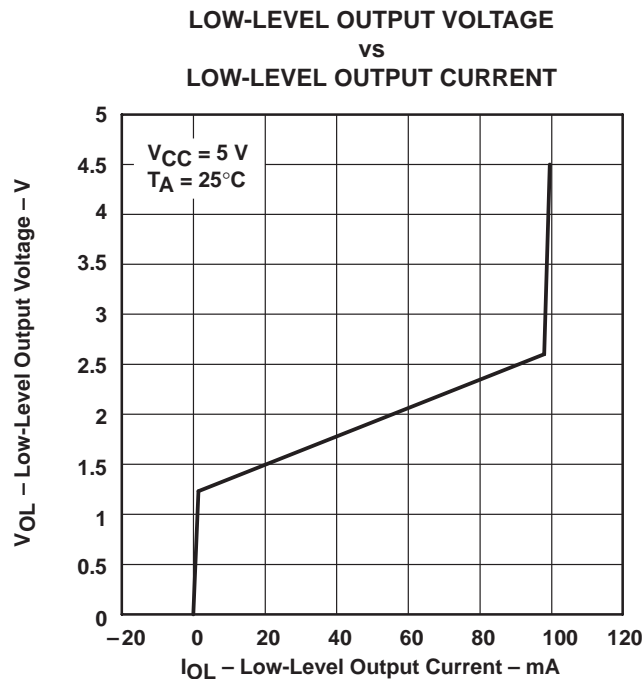


Figure 7

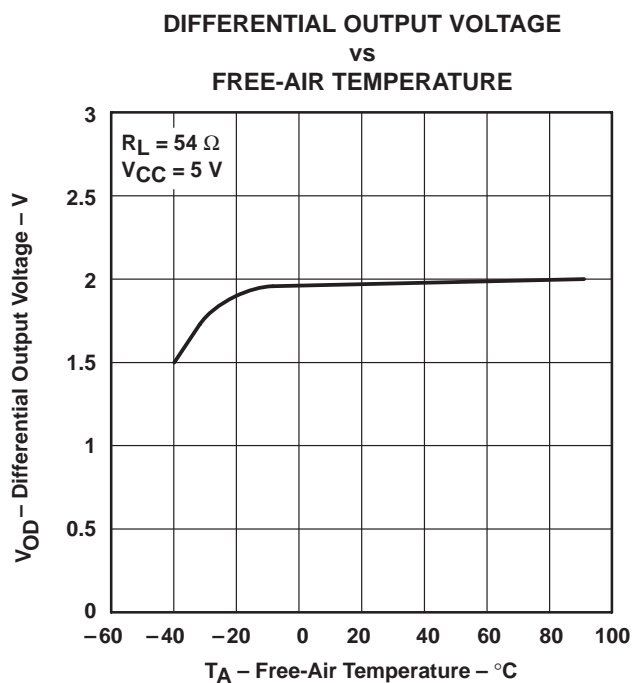


Figure 8

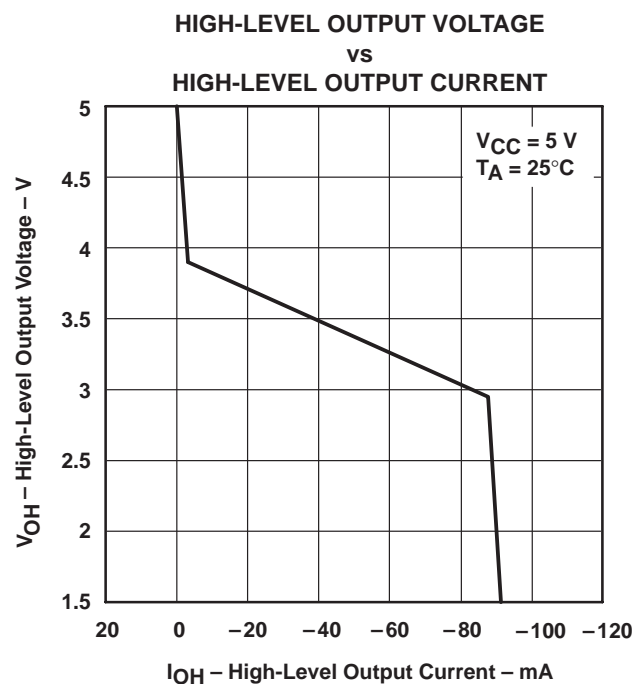


Figure 9

SN65LBC174, SN75LBC174
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TYPICAL CHARACTERISTICS

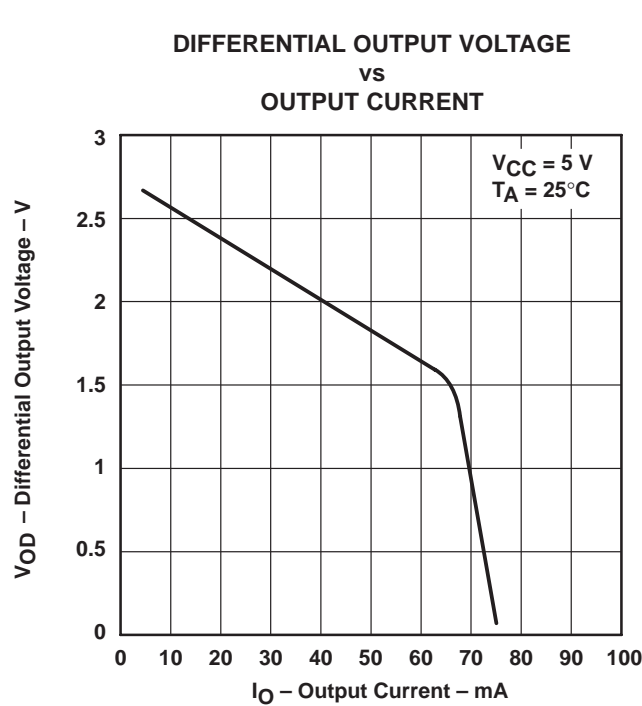


Figure 10

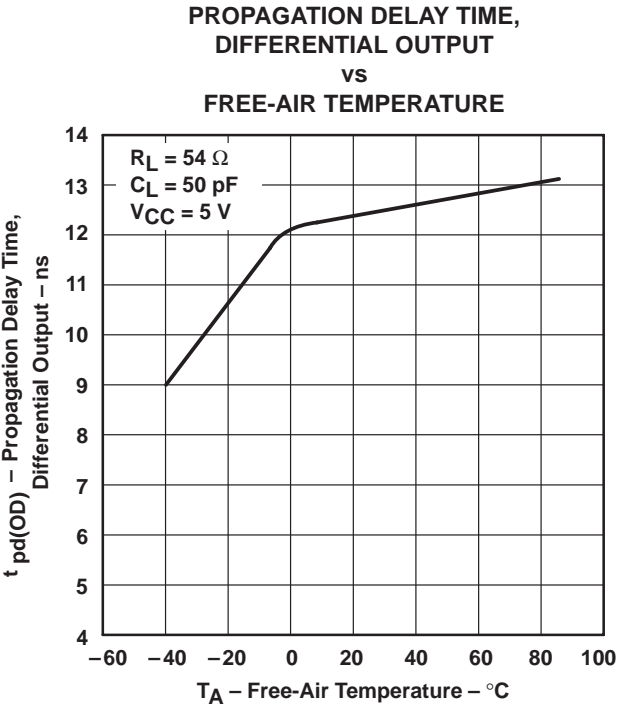


Figure 11

SN65LBC174, SN75LBC174 QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVERS

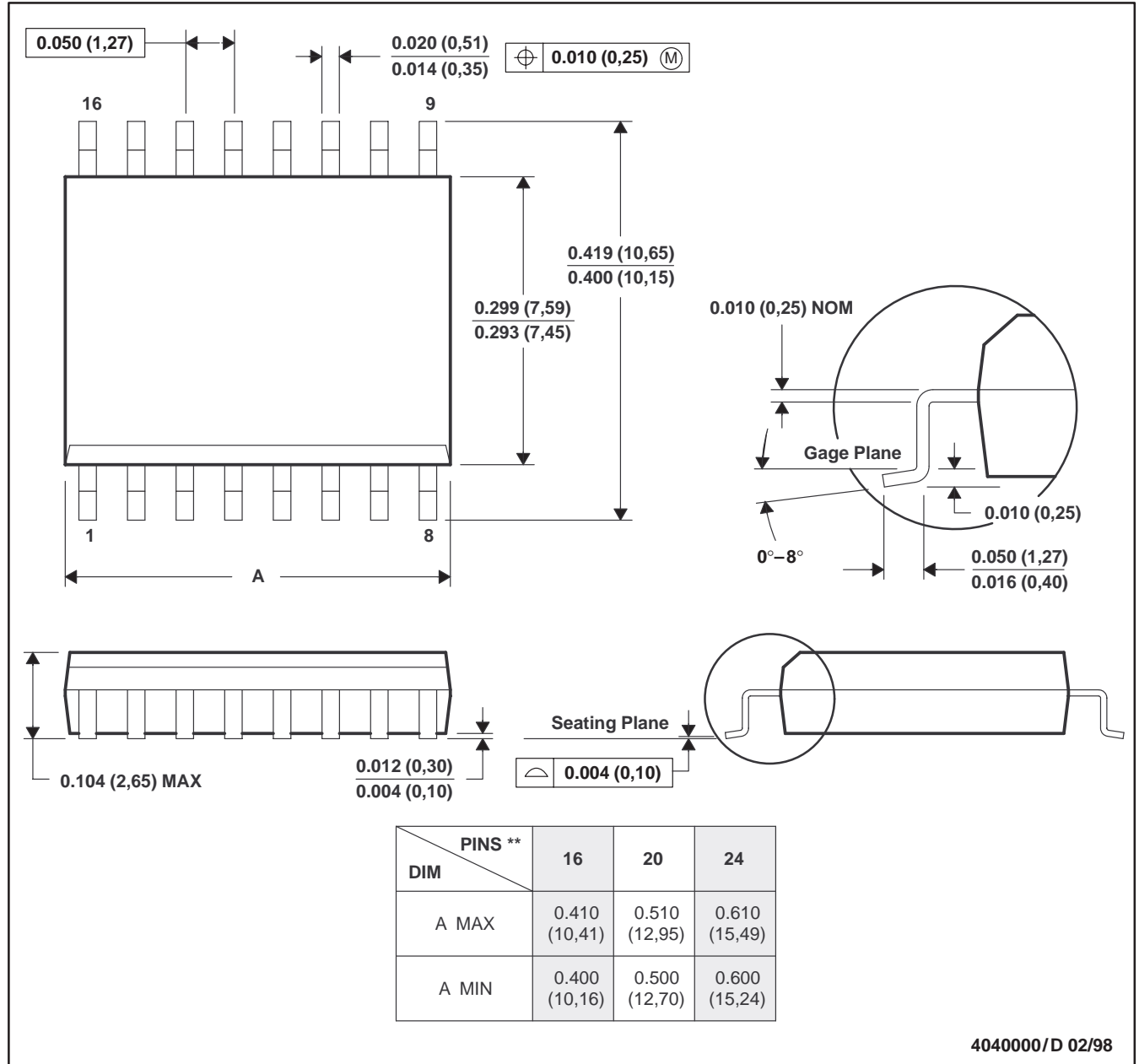
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MECHANICAL DATA

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-013

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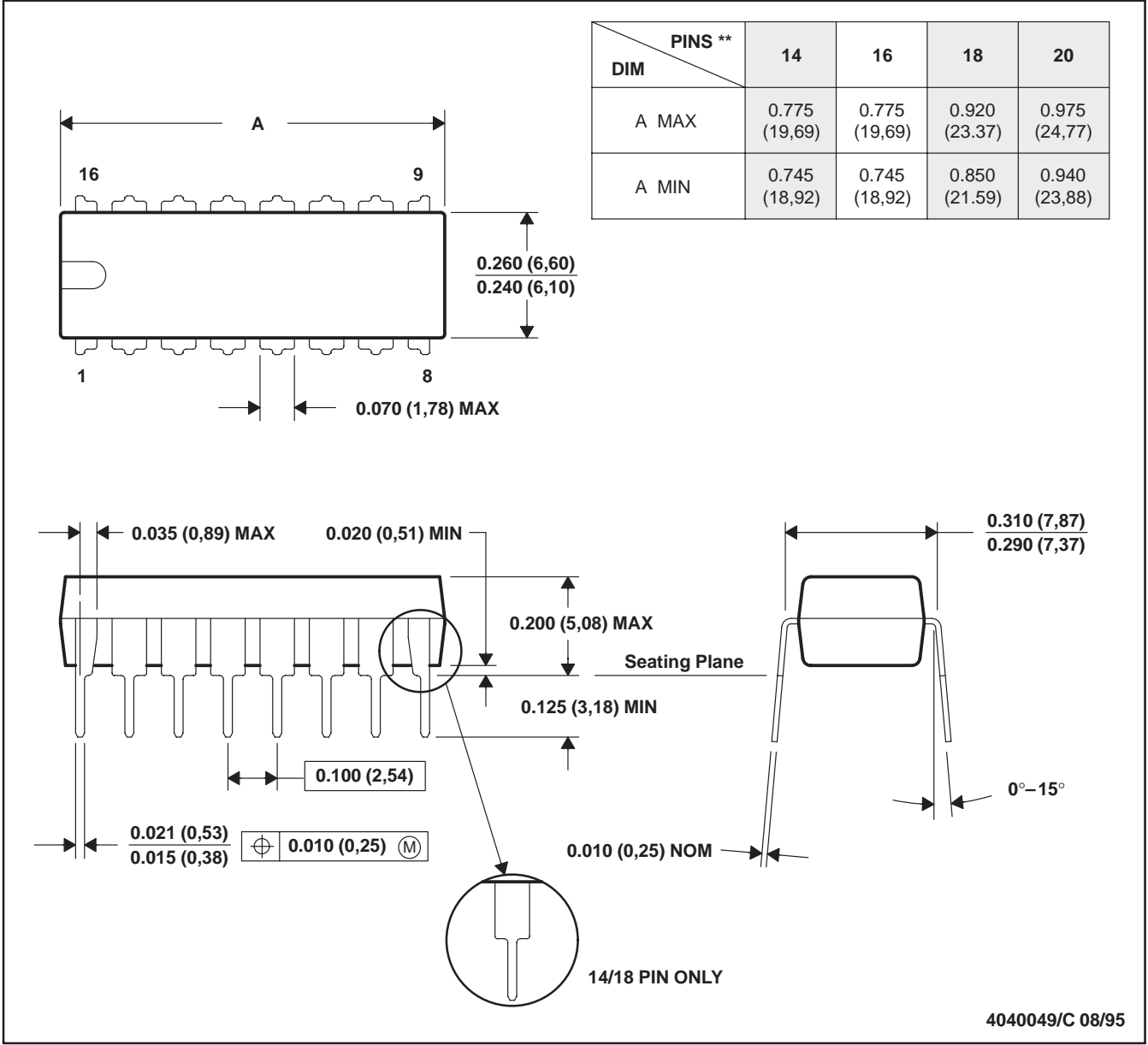
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MECHANICAL DATA

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PIN SHOWN



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