MICREL
The Infinite Bandwidth Company™

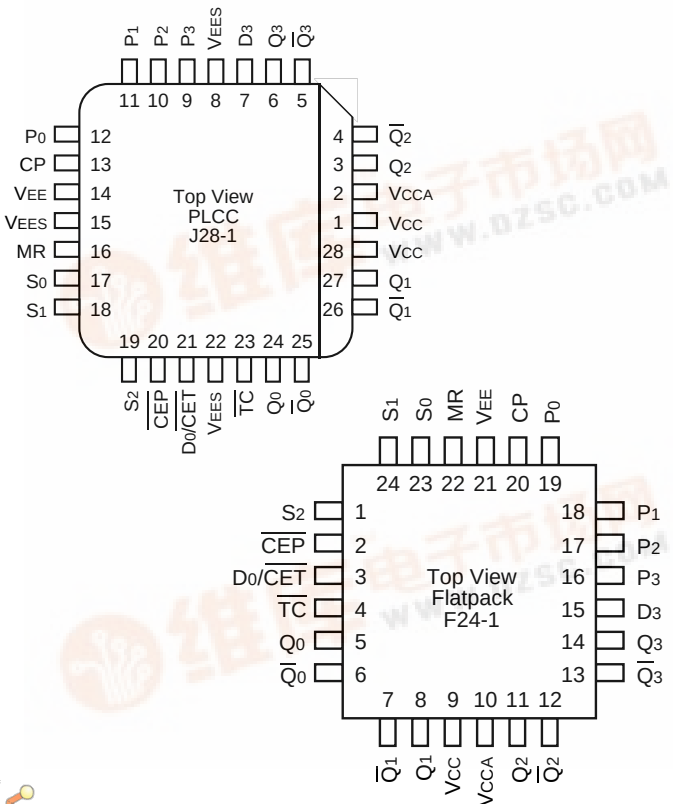
ENHANCED 4-STAGE COUNTER/SHIFT REGISTER

SY100S336A

FEATURES

- **Max. shift frequency of 700MHz**
- **Clock to Q delay max. of 1100ps**
- **Sn to $\overline{TC}$ speed improved by 50%**
- **Sn set-up and hold time reduced by more than 50%**
- **IEE min. of –170mA**
- **Industry standard 100K ECL levels**
- **Internal 75KΩ input pull-down resistors**
- **Extended supply voltage option: VEE = –4.2V to –5.5V**
- **Voltage and temperature compensation for improved noise immunity**
- **50% faster than Fairchild 300K at lower power**
- **Function and pinout compatible with Fairchild F100K**
- **Available in 24-pin CERPACK and 28-pin PLCC packages**

PIN CONFIGURATIONS



DESCRIPTION

The SY100S336A is functionally the same as the SY100S336, but has Sn to $\overline{TC}$ speed and Sn set-up and hold times significantly improved, allowing for higher clock frequency when used as a cascaded multi-stage counter.

The SY100S336A functions either as a modulo-16 up/down counter or as a 4-bit bidirectional shift register and is designed for use in high-performance ECL systems. Three Select inputs (Sn) are provided for determining the mode of operation. The Function Table lists the available modes of operation. In order to allow cascading for multistage counters, two Count Enable controls ($\overline{CEP}$, $\overline{CET}$) are provided. The $\overline{CET}$ input also functions as the Serial Data input (S_0) for a shift-up operation, while the D_3 input serves as the Serial Data input for the shift-down operation.

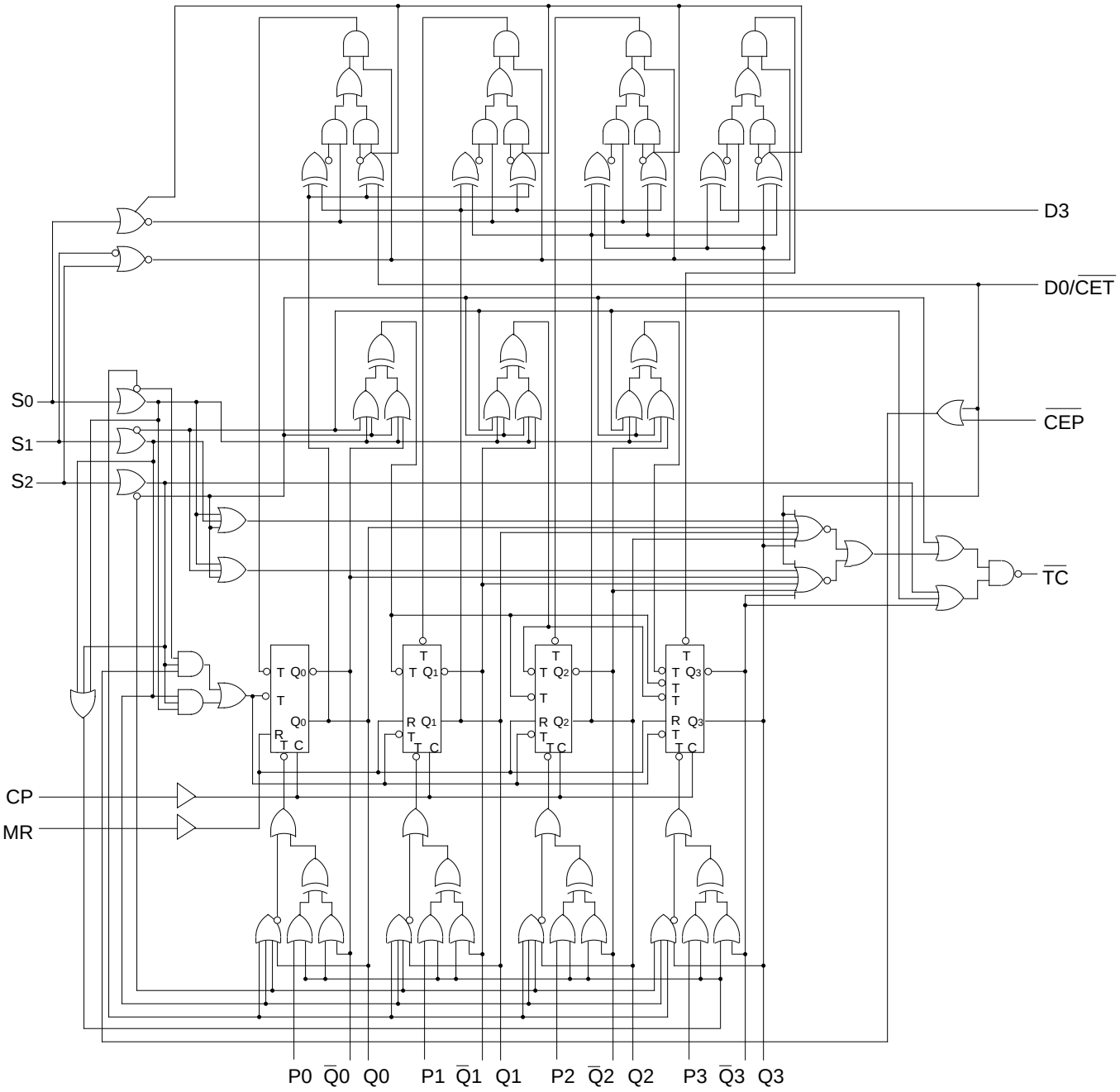
When the device is in the counting mode, the Terminal Count ($\overline{TC}$) goes to a logical LOW when the count reaches 15 for count-up or reaches 0 for count-down. When in the shift mode, the $\overline{TC}$ output simply repeats the Q_3 output.

The flexiblity provided by the $\overline{TC}/Q_3$ output and the $D_0/\overline{CET}$ input allows these signals to be interconnected from one stage to the next higher stage for multistage counting or shift-up operations. The individual Presets (P_n) allow initialization of the counter by entering data in parallel to preset the counter. A logic HIGH on the Master Reset (MR) overrides all other inputs and asynchronously clears the flip-flops. An additional synchronous Clear is provided, as well as a complement function which synchronously inverts the contents of the flip-flops. All inputs have 75KΩ pull-down resistors.

PIN NAMES

Pin	Function
CP	Clock Pulse Input
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)
$D_0/\overline{CET}$	Serial Data Input/Count Enable Trickle Input (Active LOW)
S_0 — S_2	Select Inputs
MR	Master Reset Input
VEES	VEE Substrate
VCCA	VCCO for ECL Outputs
P_0 – P_3	Preset Inputs
D_3	Serial Data Input
$\overline{TC}$	Terminal Count Output
Q_0 — Q_3	Data Outputs
$\overline{Q_0}$ — $\overline{Q_3}$	Complementary Data Outputs

BLOCK DIAGRAM



TRUTH TABLE[1]

Inputs								Outputs					
MR	**S_2**	**S_1**	**S_0**	**$\overline{CEP}$**	**$D_0/\overline{CET}$**	**D_3**	**CP**	**Q_0**	**Q_1**	**Q_2**	**Q_3**	**$\overline{TC}$**	**Mode**
L	L	L	L	X	X	X	u	P_0	P_1	P_2	P_3	L	Preset (Parallel Load)
L	L	L	H	X	X	X	u	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	L	Invert
L	L	H	L	X	X	X	u	Q_1	Q_2	Q_3	D_3	D_3	Shift Left
L	L	H	H	X	X	X	u	D_0	Q_0	Q_1	Q_2	Q_3*	Shift Right
L	H	L	L	L	L	X	u	(Q_{0-3}) minus 1				①	Count Down
L	H	L	L	H	L	X	X	Q_0	Q_1	Q_2	Q_3	①	Count Down with $\overline{CEP}$ Not Active
L	H	L	L	X	H	X	X	Q_0	Q_1	Q_2	Q_3	H	Count Down with $\overline{CET}$ Not Active
L	H	L	H	X	X	X	u	L	L	L	L	H	Clear
L	H	H	L	L	L	X	u	(Q_{0-3}) plus 1				≠	Count Up
L	H	H	L	H	L	X	X	Q_0	Q_1	Q_2	Q_3	≠	Count Up with $\overline{CEP}$ Not Active
L	H	H	L	X	H	X	X	Q_0	Q_1	Q_2	Q_3	H	Count Up with $\overline{CET}$ Not Active
L	H	H	H	X	X	X	X	Q_0	Q_1	Q_2	Q_3	H	Hold
H	L	L	L	X	X	X	X	L	L	L	L	L	Asynchronous Master Reset
H	L	L	H	X	X	X	X	L	L	L	L	L	
H	L	H	L	X	X	X	X	L	L	L	L	L	
H	L	H	H	X	X	X	X	L	L	L	L	L	
H	H	L	L	X	L	X	X	L	L	L	L	L	
H	H	L	L	X	H	X	X	L	L	L	L	H	
H	H	L	H	X	X	X	X	L	L	L	L	H	
H	H	H	L	X	X	X	X	L	L	L	L	H	
H	H	H	H	X	X	X	X	L	L	L	L	H	

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   u = LOW-to-HIGH Transition
   ① = L if $Q_0 – Q_3$ = LLLL
   H if $Q_0 – Q_3 \neq$ LLLL
   ≠ = L if $Q_0 – Q_3$ = HHHH
   H if $Q_0 – Q_3 \neq$ HHHH
   * Before the clock, $\overline{TC}$ is Q_3; after the clock, $\overline{TC}$ is Q_2

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current, All Inputs	—	—	200	µA	V_{IN} = V_{IH} (Max.)
I_{EE}	Power Supply Current	–170	–120	–60	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERPACK

V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{shift}	Shift Frequency	700	—	700	—	700	—	MHz	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q}_n$	450	1200	450	1200	450	1200	ps	
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	600	1900	600	1900	600	1900	ps	
t_{PLH} t_{PHL}	Propagation Delay MR to Q_n, $\overline{Q}_n$	500	1400	500	1400	500	1400	ps	
t_{PLH} t_{PHL}	Propagation Delay MR to $\overline{TC}$	600	1900	600	1900	600	1900	ps	
t_{PLH} t_{PHL}	Propagation Delay D_0/$\overline{CET}$ to $\overline{TC}$	400	1200	400	1200	400	1200	ps	
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{TC}$	400	1500	400	1500	400	1500	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t_S	Set-up Time							ps	
	D_3	800	—	800	—	800	—		
	P_n	800	—	800	—	800	—		
	D_0/$\overline{CET}$ to $\overline{CEP}$	700	—	700	—	700	—		
	S_n	1000	—	1000	—	1000	—		
	MR (Release Time)	900	—	900	—	900	—		
t_H	Hold Time							ps	
	D_3	200	—	200	—	200	—		
	P_n	200	—	200	—	200	—		
	D_0/$\overline{CET}$ to $\overline{CEP}$	200	—	200	—	200	—		
	S_n	-200	—	-200	—	-200	—		
t_{pw} (H)	Pulse Width HIGH, CP, MR	—	800	—	800	—	800	ps	

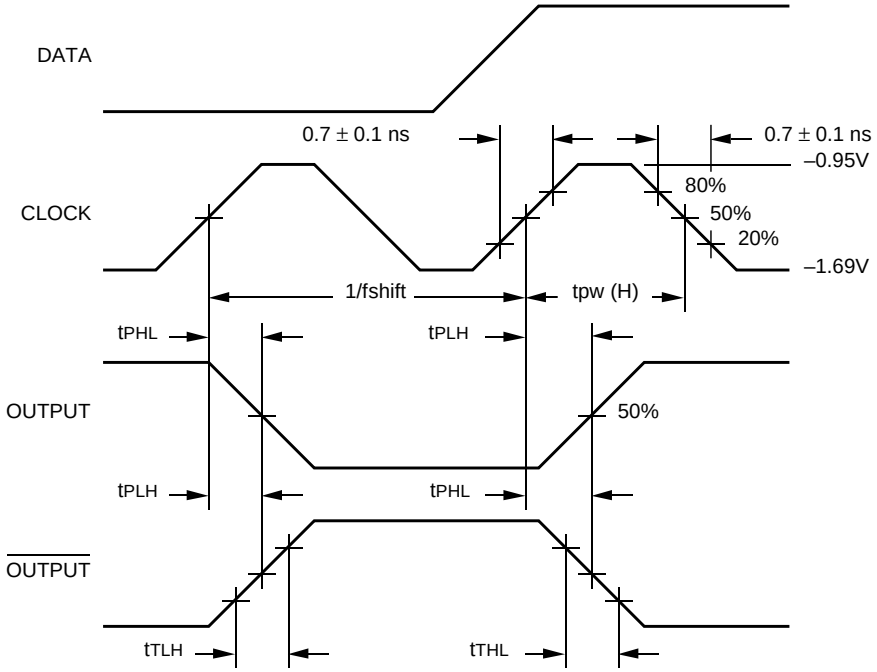
AC ELECTRICAL CHARACTERISTICS

PLCC

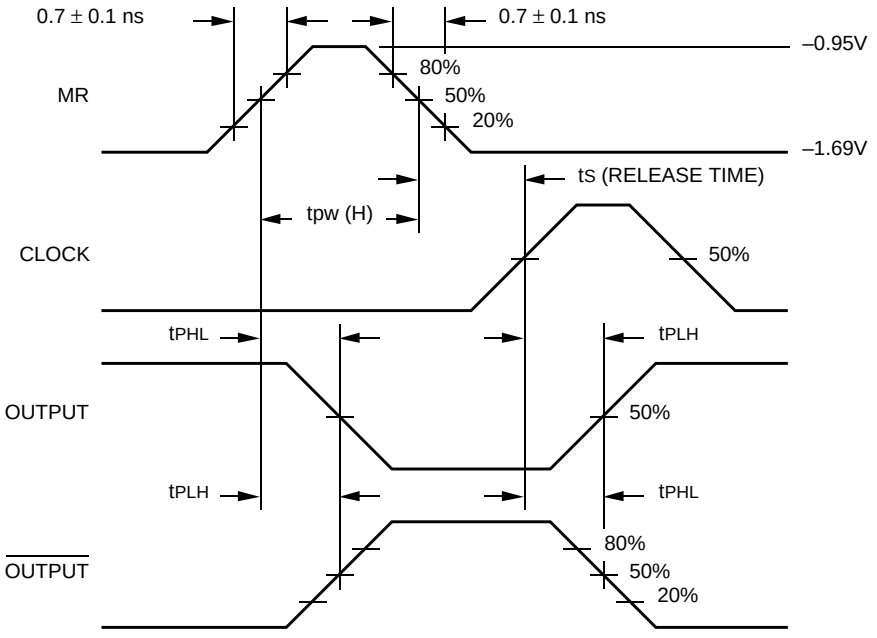
V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{shift}	Shift Frequency	700	—	700	—	700	—	MHz	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q}_n$	450	1100	450	1100	450	1100	ps	
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	600	1800	600	1800	600	1800	ps	
t_{PLH} t_{PHL}	Propagation Delay MR to Q_n, $\overline{Q}_n$	500	1300	500	1300	500	1300	ps	
t_{PLH} t_{PHL}	Propagation Delay MR to $\overline{TC}$	600	1800	600	1800	600	1800	ps	
t_{PLH} t_{PHL}	Propagation Delay D_0/$\overline{CET}$ to $\overline{TC}$	400	1100	400	1100	400	1100	ps	
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{TC}$	400	1500	400	1500	400	1500	ps	
t_{TLH} t_{THL}	Transition Time300 20% to 80%, 80% to 20%	900	300	900	300	900	ps		
t_S	Set-up Time							ps	
	D_3	800	—	800	—	800	—		
	P_n	800	—	800	—	800	—		
	D_0/$\overline{CET}$ to $\overline{CEP}$	700	—	700	—	700	—		
	S_n	1000	—	1000	—	1000	—		
	MR (Release Time)	900	—	900	—	900	—		
t_H	Hold Time							ps	
	D_3	200	—	200	—	200	—		
	P_n	200	—	200	—	200	—		
	D_0/$\overline{CET}$ to $\overline{CEP}$	200	—	200	—	200	—		
	S_n	-200	—	-200	—	-200	—		
t_{pw} (H)	Pulse Width HIGH, CP, MR	—	800	—	800	—	800	ps	

TIMING DIAGRAMS

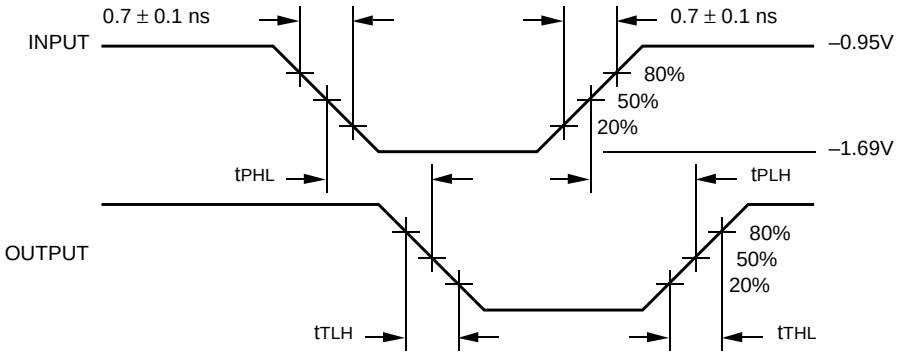


Propagation Delay (Clock) and Transition Times

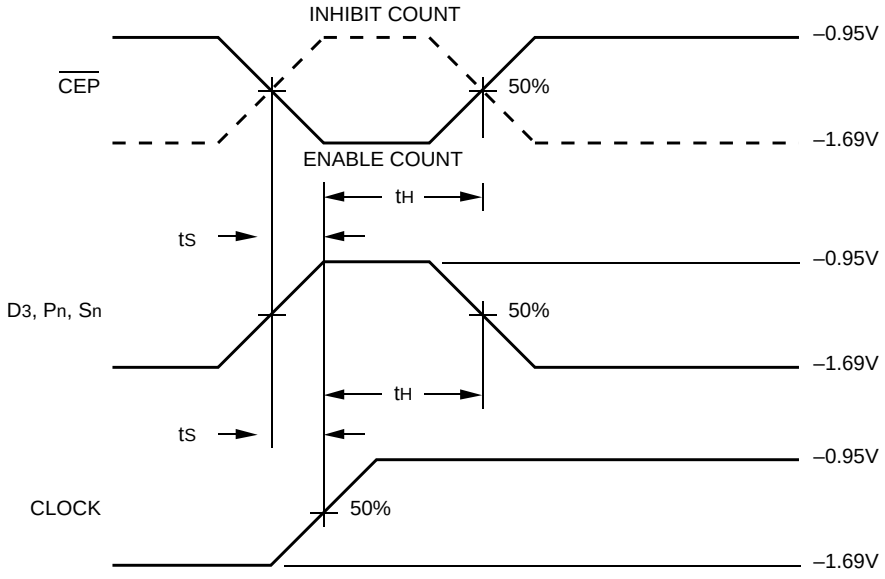


Propagation Delay (Reset)

TIMING DIAGRAMS



Propagation Delay (Serial Data, Selects)



Set-up and Hold Time

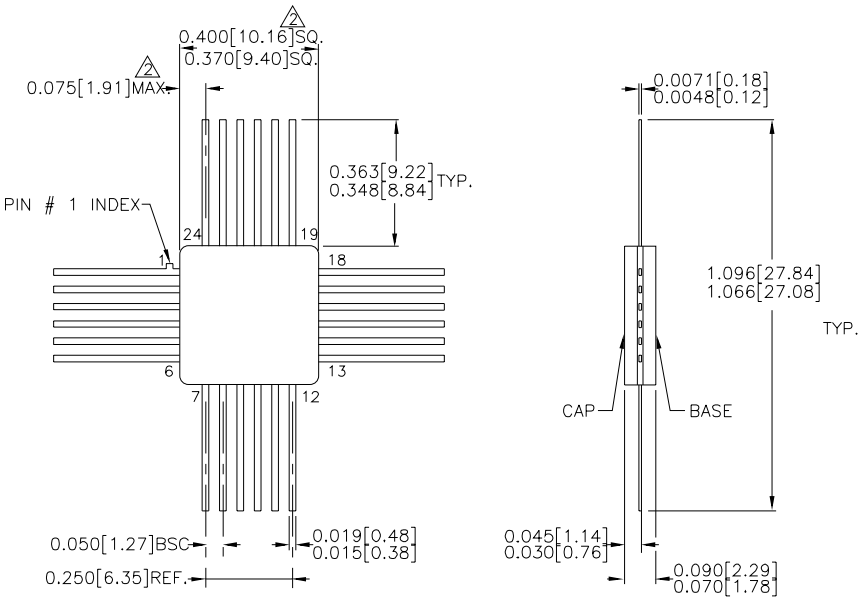
NOTES:

1. V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND.
2. t_S is the minimum time before the transition of the clock that information must be present at the data input.
3. t_H is the minimum time after the transition of the clock that information must remain unchanged at the data input.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S336AFC	F24-1	Commercial
SY100S336AJC	J28-1	Commercial
SY100S336AJCTR	J28-1	Commercial

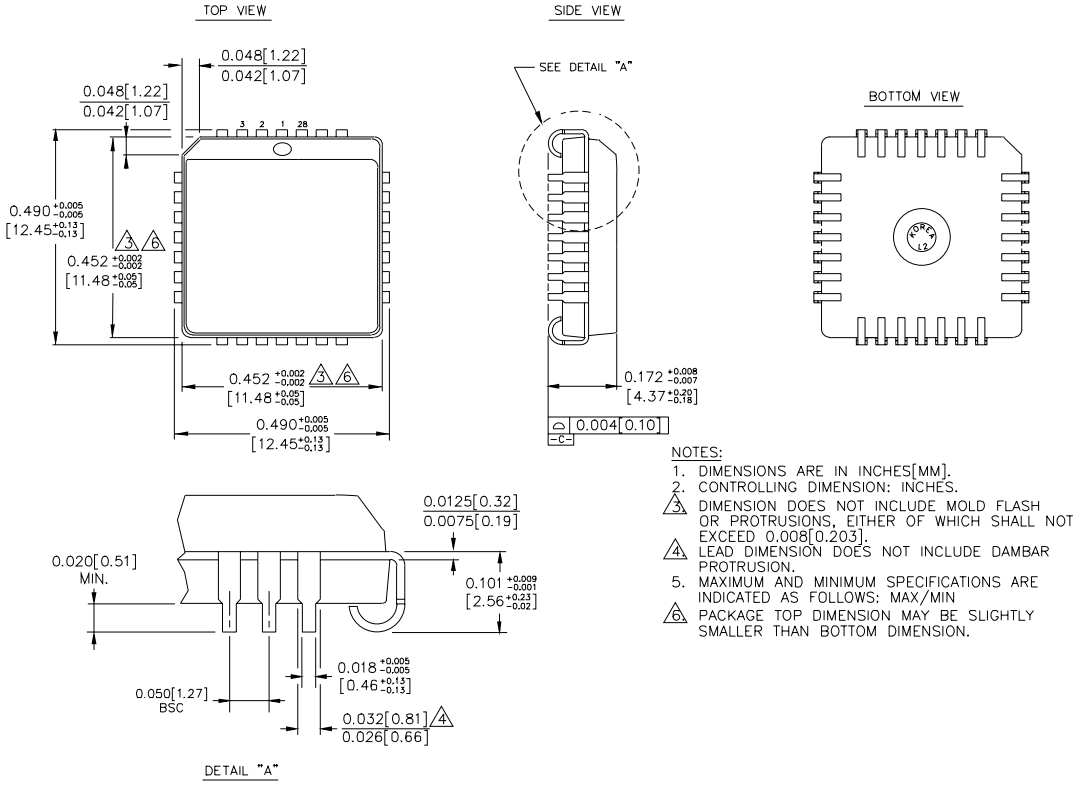
24 LEAD CERPACK (F24-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03

28 LEAD PLCC (J28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

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