Integrated Circuit Systems, Inc.

ICS85356I

2:1, Differential-to-3.3V Dual LVPECL / ECL Clock Multiplexer

General Description

ICS HiPerClockS™

The ICS85356I is a dual 2:1 Differential-to-LVPECL Multiplexer and is a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The device has both common select and individual select inputs. When COM_SEL is logic High, the CLKxx input pairs will be passed to the output. When COM_SEL is logic Low, the output is determined by the setting of the SEL0 pin for channel 0 and the SEL1 pin for Channel 1.

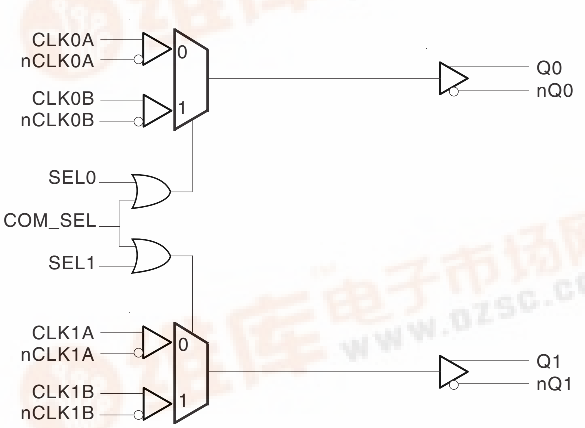
The differential input has a common mode range that can accept most differential input types such as LVPECL, LVDS, LVHSTL, SSTL, and HCSL. The ICS85356I can therefore be used as a differential translator to translate almost any differential input type to LVPECL. It can also be used in ECL mode by setting V_{CC}=0V and V_{EE} to -3.0V to - 3.8V.

The ICS85356I adds negligible jitter to the input clock and can operate at high frequencies in excess of 900MHz thus making it ideal for use in demanding applications such as SONET, Fibre Channel, 1 Gigabit/10 Gigabit Ethernet.

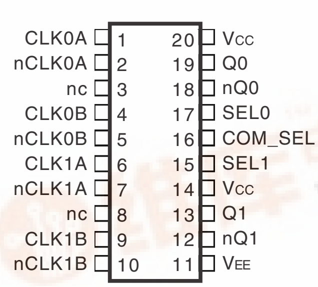
Features

- High speed differential multiplexer. The device can be configured as a 2:1 multiplexer
- Dual 3.3V LVPECL outputs
- Selectable differential CLKxx, nCLKxx inputs
- CLKxx, nCLKxx pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Output frequency: 900MHz (typical)
- Translates any single ended input signal to 3.3V LVPECL levels with resistor bias on nCLKxx input
- Output skew: 75ps (typical)
- Propagation delay: 1.15ns (typical)
- LVPECL mode operating voltage supply range: V_{CC} = 3V to 3.8V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -3V to -3.8V
- -40°C to 85°C ambient operating temperature
- Lead-Free package available
- Compatible with MC100LVEL56

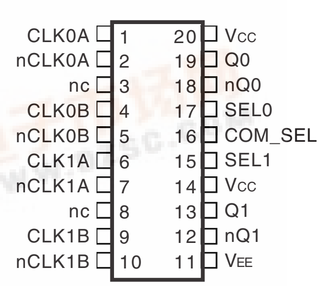
Block Diagram



Pin Assignment



ICS85356I
20-Lead SOIC
7.5mm x 12.8mm x 2.3mm
M Package
Top View



ICS85356I
20-Lead TSSOP
6.5mm x 4.4mm x 0.92mm
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
14, 20	V_{CC}	Power		Core supply pin.
1	CLK0A	Input	Pulldown	Non-inverting differential clock input.
2	nCLK0A	Input	Pullup	Inverting differential clock input.
3, 8	nc	Unused		No connect.
4	CLK0B	Input	Pulldown	Non-inverting differential clock input.
5	nCLK0B	Input	Pullup	Inverting differential clock input.
6	CLK1A	Input	Pulldown	Non-inverting differential clock input.
7	nCLK1A	Input	Pullup	Inverting differential clock input.
9	CLK1B	Input	Pulldown	Non-inverting differential clock input.
10	nCLK1B	Input	Pullup	Inverting differential clock input.
11	V_{EE}	Power		Negative supply pins.
12, 13	nQ1, Q1	Output		Differential output pairs. LVPECL interface levels.
15	SEL1	Input	Pullup	Clock select input. LVCMOS / LVTTL interface levels.
16	COM_SEL	Input	Pulldown	Common select input. LVCMOS / LVTTL interface levels.
17	SEL0	Input	Pullup	Clock select input. LVCMOS / LVTTL interface levels.
18, 19	nQ0, Q0	Output		Differential output pairs. LVPECL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ

TABLE 3. CONTROL INPUT FUNCTION TABLE

Inputs			Outputs			
COM_SEL	SEL1	SEL0	Q0	nQ0	Q1	nQ1
0	0	0	CLK0A	nCLK0A	CLK1A	nCLK1A
0	0	1	CLK0B	nCLK0B	CLK1A	nCLK1A
0	1	0	CLK0A	nCLK0A	CLK1B	nCLK1B
0	1	1	CLK0B	nCLK0B	CLK1B	nCLK1B
1	X	X	CLK0B	nCLK0B	CLK1B	nCLK1B

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	46.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 3.3V±0.3V, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.0	3.3	3.6	V
I_{EE}	Power Supply Current				40	mA

TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS, V_{CC} = 3.3V±0.3V, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	SEL0, SEL1, COM_SEL		2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	SEL0, SEL1, COM_SEL		-0.3		0.8	V
I_{IH}	Input High Current	SEL0, SEL1	$V_{CC} = V_{IN}$ = 3.6V			5	µA
		COM_SEL	$V_{CC} = V_{IN}$ = 3.6V			150	µA
I_{IL}	Input Low Current	SEL0, SEL1	V_{CC} = 3.6V, V_{IN} = 0V	-150			µA
		COM_SEL	V_{CC} = 3.6V, V_{IN} = 0V	-5			µA

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, V_{CC} = 3.3V±0.3V, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0A, CLK0B, CLK1A, CLK1B	$V_{CC} = V_{IN}$ = 3.6V			150	µA
		nCLK0A, nCLK0B, nCLK1A, nCLK1B	$V_{CC} = V_{IN}$ = 3.6V			5	µA
I_{IL}	Input Low Current	CLK0A, CLK0B, CLK1A, CLK1B	V_{CC} = 3.6V, V_{IN} = 0V	-5			µA
		nCLK0A, nCLK0B, nCLK1A, nCLK1B	V_{CC} = 3.6V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage			0.15		1.0	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 0.5		V_{CC} - 0.85	V

NOTE 1: Common mode input voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLKx, nCLKx is V_{CC} + 0.3V.

TABLE 4D. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V±0.3V, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.4		V_{CC} - 1.0	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 2.0		V_{CC} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing	$f \leq$ 700MHz	0.6		1.0	V

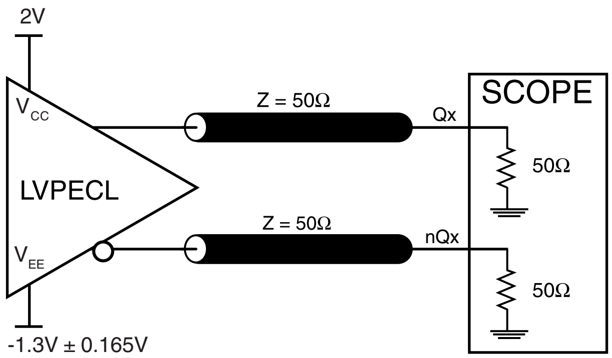
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 5. AC CHARACTERISTICS, V_{CC} = 3.3V±0.3V, TA = -40°C TO 85°C

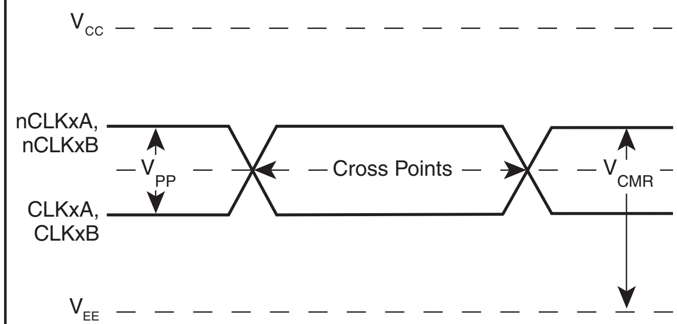
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency			900		MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq$ 900MHz	0.85	1.15	1.45	ns
*t*sk(o)	Output Skew; NOTE 2, 3			75	150	ps
t_R	Output Rise Time	20% to 80%	200		580	ps
t_F	Output Fall Time	20% to 80%	200		580	ps
t_{odc}	Duty Cycle Skew				100	ps

All parameters measured at $f \leq$ 622MHz unless noted otherwise.
This part does not add measurable jitter.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

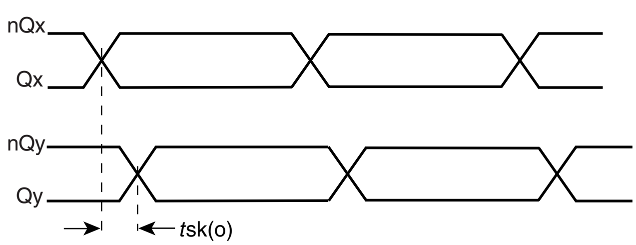
PARAMETER MEASUREMENT INFORMATION



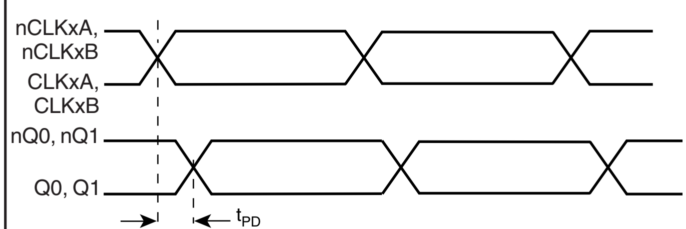
3.3V OUTPUT LOAD AC TEST CIRCUIT



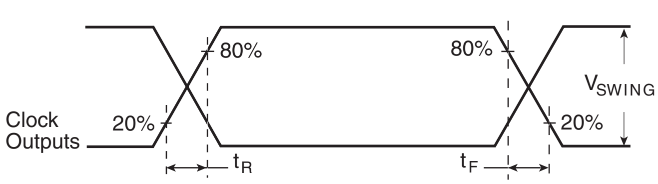
DIFFERENTIAL INPUT LEVEL



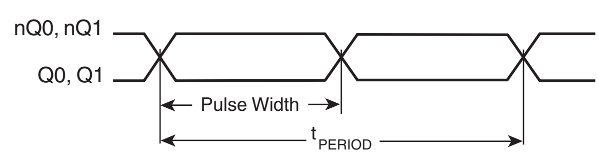
OUTPUT SKEW



PROPAGATION DELAY



OUTPUT RISE/FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = $V_{CC}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

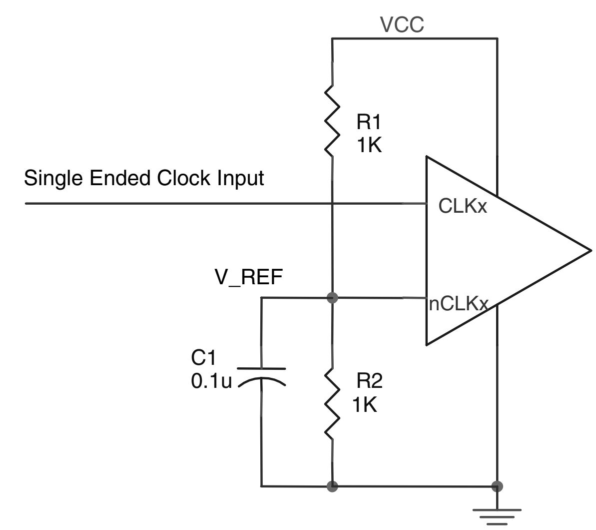


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

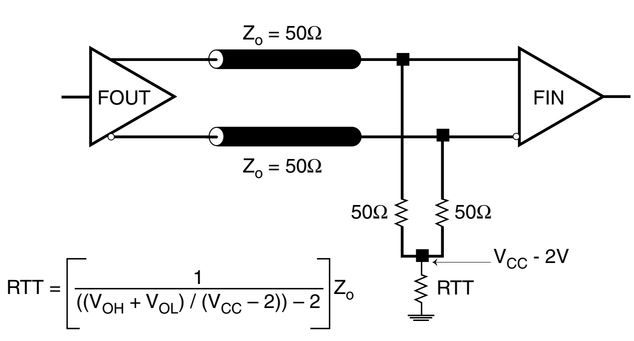


FIGURE 2A. LVPECL OUTPUT TERMINATION

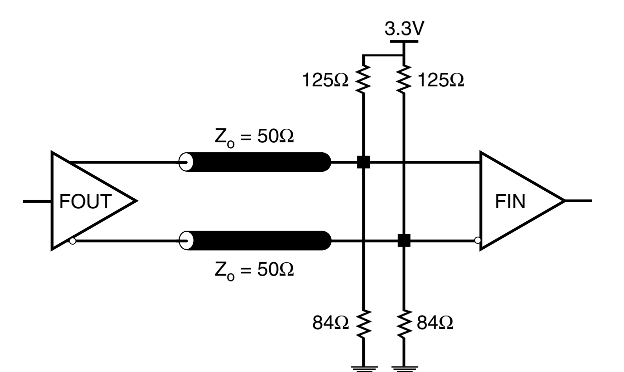


FIGURE 2B. LVPECL OUTPUT TERMINATION

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

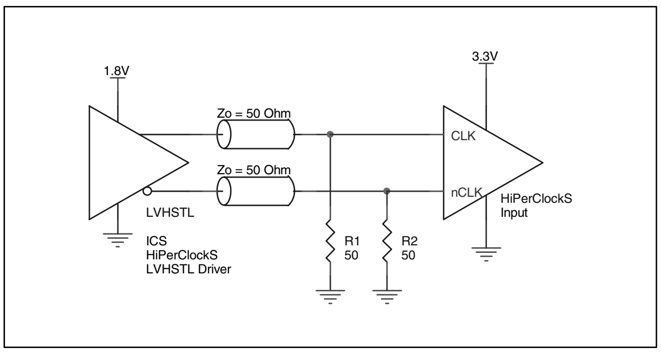


FIGURE 3A. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY ICS HIPERCLOCKS LVHSTL DRIVER

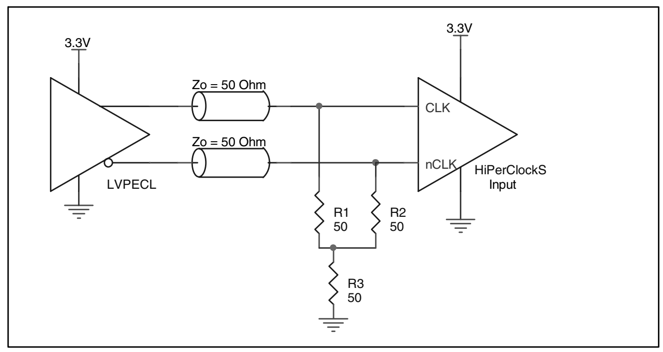


FIGURE 3B. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

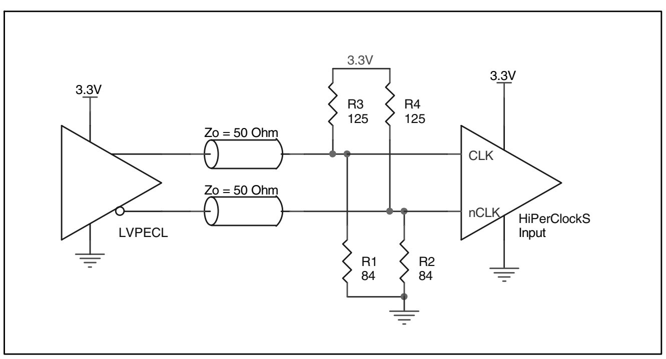


FIGURE 3C. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

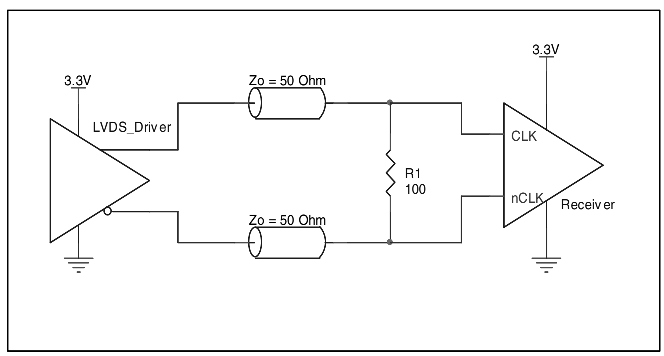


FIGURE 3D. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

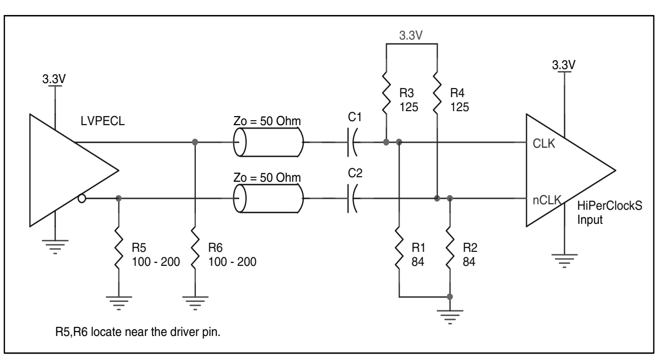


FIGURE 3E. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS85356I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS85356I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 0.3V = 3.6V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.6V * 40mA = **144mW**
- Power (outputs)$_{MAX}$ = **30.2mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 30.2mW = **60.4mW**

Total Power$_{\_MAX}$ (3.6V, with all outputs switching) = 144mW + 60.4mW = **204.4mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used . Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 39.7°C/W per Table 6A below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.204W * 39.7°C/W = 93.1°C. This is well below the limit of 125°C

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 6A. Thermal Resistance θ_{JA} for 20-pin SOIC, Forced Convection

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	83.2°C/W	65.7°C/W	57.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Table 6B. Thermal Resistance θ_{JA} for 20-pin TSSOP, Forced Convection

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 4.*

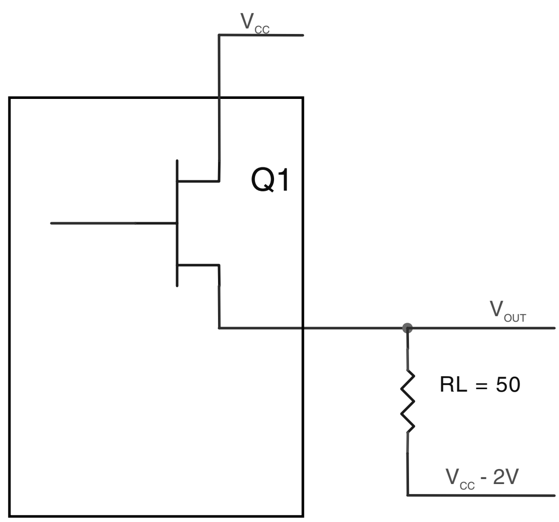


Figure 4. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 1.0V}$

  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{1.0V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.7V}$

  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 1V)/50\Omega] * 1V =$ **20.0mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.2mW**

RELIABILITY INFORMATION

TABLE 7A. θ_{JA} VS. AIR FLOW TABLE FOR 20 LEAD SOIC

θ_{JA} by Velocity (Linear Feet per Minute)

	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	83.2°C/W	65.7°C/W	57.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TABLE 7B. θ_{JA} VS. AIR FLOW TABLE FOR 20 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)

	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS85356I is: 446

PACKAGE OUTLINE - M SUFFIX FOR 20 LEAD SOIC

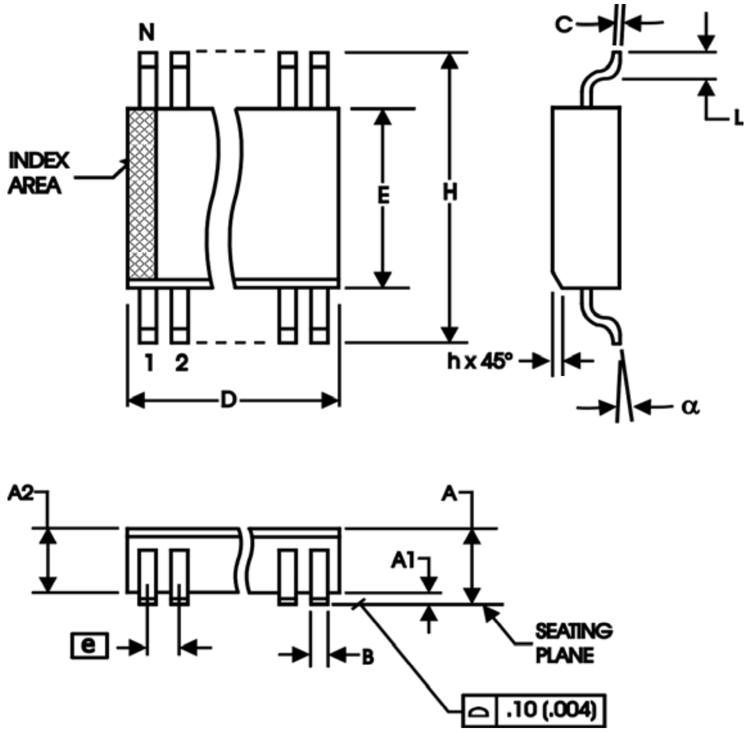


TABLE 8A. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	20	
A	--	2.65
A1	0.10	--
A2	2.05	2.55
B	0.33	0.51
C	0.18	0.32
D	12.60	13.00
E	7.40	7.60
e	1.27 BASIC	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS - 013, MO - 119

PACKAGE OUTLINE - G SUFFIX FOR 20 LEAD TSSOP

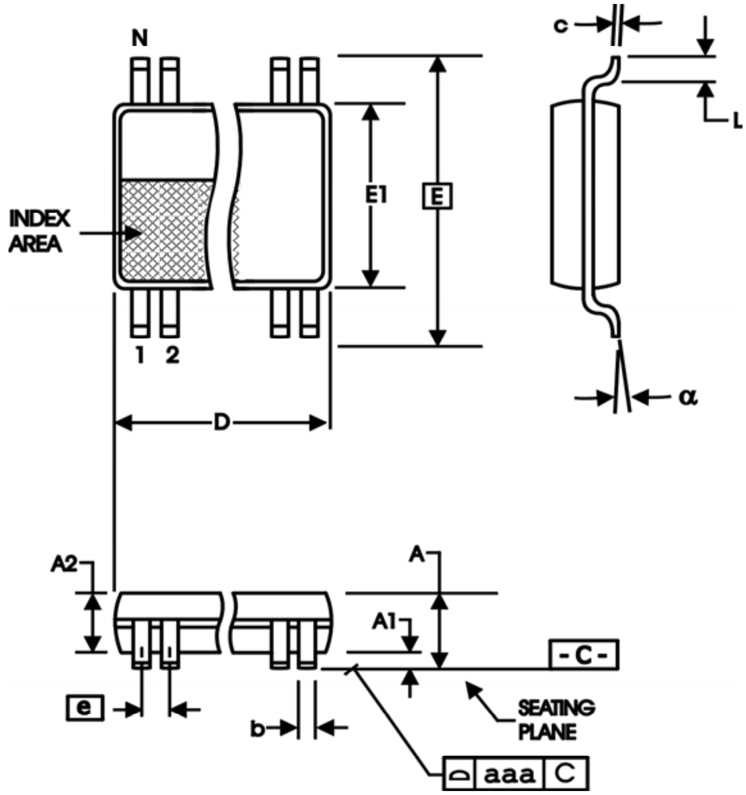


TABLE 8B. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

REFERENCE DOCUMENT: JEDEC PUBLICATION 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS85356AMI	ICS85356AMI	20 lead SOIC	38 per tube	-40°C to 85°C
ICS85356AMIT	ICS85356AMI	20 lead SOIC on Tape and Reel	1000	-40°C to 85°C
ICS85356AGI	ICS85356AGI	20 lead TSSOP	72 per tube	-40°C to 85°C
ICS85356AGIT	ICS85356AGI	20 lead TSSOP on Tape and Reel	2500	-40°C to 85°C
ICS85356AGILF	ICS85356AGIL	20 lead "Lead Free" TSSOP	72 per tube	-40°C to 85°C
ICS85356AGILFT	ICS85356AGIL	20 lead "Lead Free" TSSOP on Tape and Reel	2500	-40°C to 85°C

Integrated
Circuit
Systems, Inc.

ICS85356I

2:1, Differential-to-3.3V Dual LVPECL / ECL Clock Multiplexer

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A		7 13	Added Differential Clock Input Interface section. Ordering Information Table - added Lead Free part number. Updated data sheet format.	10/7/04