TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS043B – Revised July 2003

CD4046B Types

CMOS Micropower Phase-Locked Loop

■ CD4046B CMOS Micropower Phase-Locked Loop (PLL) consists of a low-power, linear voltage-controlled oscillator (VCO) and two different phase comparators having a common signal-input amplifier and a common comparator input. A 5.2-V zener diode is provided for supply regulation if necessary.

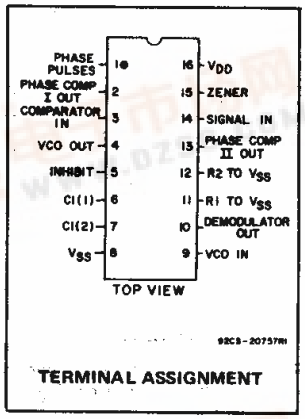
The CD4046B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

VCO Section

The VCO requires one external capacitor C1 and one or two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO and resistor R2 enables the VCO to have a frequency offset if required. The high input impedance ($10^{12}\Omega$) of the VCO simplifies the design of low-pass filters by permitting the designer a wide choice of resistor-to-capacitor ratios. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at terminal 10 (DEMODULATED OUTPUT). If this terminal is used, a load resistor (R_S) of 10 kΩ or more should be connected from this terminal to V_{SS}. If unused this terminal should be left open. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. A full CMOS logic swing is available at the output of the VCO and allows direct coupling to CMOS frequency dividers such as the RCA-CD4024, CD4018, CD4020, CD4022, CD4029, and CD4059. One or more CD4018 (Preset-table Divide-by-N Counter) or CD4029 (Pre-settable Up/Down Counter), or CD4059A (Programmable Divide-by-"N" Counter), together with the CD4046B (Phase-Locked Loop) can be used to build a micropower low-frequency synthesizer. A logic 0 on the INHIBIT input "enables" the VCO and the source follower, while a logic 1 "turns off" both to minimize stand-by power consumption.

Features:

- Very low power consumption: 70 μW (typ.) at VCO f_o = 10 kHz, V_{DD} = 5 V
- Operating frequency range up to 1.4 MHz (typ.) at V_{DD} = 10 V, RI = 5 kΩ
- Low frequency drift: 0.04%/°C (typ.) at V_{DD} = 10 V
- Choice of two phase comparators:
  Exclusive-OR network (I)
  Edge-controlled memory network with phase-pulse output for lock indication (II)
- High VCO linearity: <1% (typ.) at V_{DD} = 10 V
- VCO inhibit control for ON-OFF keying and ultra-low standby power consumption
- Source-follower output of VCO control input (Demod. output)
- Zener diode to assist supply regulation
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



TERMINAL ASSIGNMENT

Applications:

- FM demodulator and modulator
- Frequency synthesis and multiplication
- Frequency discriminator
- Data synchronization
- Voltage-to-frequency conversion
- Tone decoding
- FSK – Modems
- Signal conditioning
- (See ICAN-6101) "RCA COS/MOS Phase-Locked Loop – A Versatile Building Block for Micropower Digital and Analog Applications"

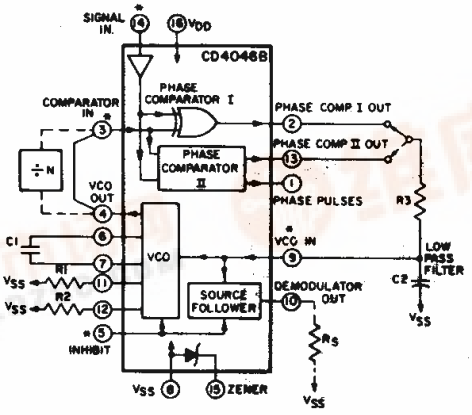
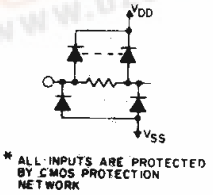


Fig.1 – CMOS phase-locked loop block diagram.



92CS-29172

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

Phase Comparators

The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within CMOS logic levels [logic "0" ≤30% (V_{DD}–V_{SS}), logic "1" ≥ 70% (V_{DD}–V_{SS})]. For smaller swings the signal must be capacitively coupled to the self-biasing amplifier at the signal input.

Phase comparator I is an exclusive-OR network; it operates analagously to an over-driven balanced mixer. To maximize the lock range, the signal- and comparator-input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to $V_{DD}/2$. The low-pass filter connected to the output of phase comparator

RECOMMENDED OPERATING CONDITIONS at T_A = Full Package-Temperature Range

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range VCO Section:			
As Fixed Oscillator	3	18	V
Phased-Lock-Loop Operation	5	18	
Supply-Voltage Range Phase Comparator Section:			
Comparators	3	18	
VCO Operation	5	18	

DESIGN INFORMATION

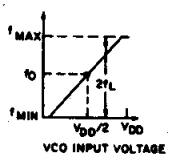
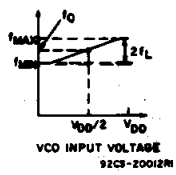
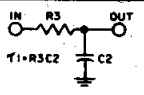
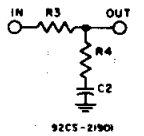
This information is a guide for approximating the values of external components for the CD4046B in a Phase-Locked-Loop system.

The selected external components must be within the following ranges:

$5\ k\Omega \leq R1, R2, R_S \leq 1\ M\Omega$

$C1 \geq 100\ pF$ at $V_{DD} \geq 5\ V$;

$C1 \geq 50\ pF$ at $V_{DD} \geq 10\ V$

Characteristics	Phase Comparator Used	Design Information	
		VCO WITHOUT OFFSET $R_2 = \infty$	VCO WITH OFFSET
VCO Frequency	1		
	2	Same as for No.1	
For No Signal Input	1	VCO will adjust to center frequency, f_o	
	2	VCO will adjust to lowest operating frequency, f_{min}	
Frequency Lock Range, $2f_L$	1	$2f_L$ = full VCO frequency range	
		$2f_L = f_{max} - f_{min}$	
	2	Same as for No.1	
Frequency Capture Range, $2f_C$	1	 (1), (2) $2f_C \approx \frac{1}{\pi}\sqrt{\frac{2\pi f_L}{\tau 1}}$	
Loop Filter Component Selection		 For $2f_C$, see Ref. (2)	
	2	$f_C = f_L$	
Phase Angle Between Signal and Comparator	1	90° at center frequency (f_o) approximating 0° and 180° at ends of lock range ($2f_L$)	
	2	Always 0° in lock	
Locks On Harmonic of Center Frequency	1	Yes	
	2	No	
Signal Input Noise Rejection	1	High	
	2	Low	

For further information, see

(1) F. Gardner, "Phase-Lock Techniques" John Wiley and Sons, New York, 1966

(2) G. S. Moschytz, "Miniaturized RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.

I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency (f_o).

The frequency range of input signals on which the PLL will lock if it was initially out of lock is defined as the frequency capture range ($2f_C$).

The frequency range of input signals on which the loop will stay locked if it was initially in lock is defined as the frequency lock range ($2f_L$). The capture range is $\leq$ the lock range.

With phase comparator I the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal.

One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0° and 180°, and is 90° at the center frequency. Fig. 2 shows the typical, triangular, phase-to-output response characteristic of phase-comparator I. Typical waveforms for a CMOS phase-locked-loop employing phase comparator I in locked condition of f_o is shown in Fig. 3.

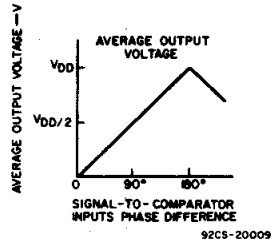


Fig.2 – Phase-comparator I characteristics at low-pass filter output.

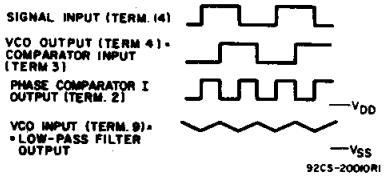


Fig. 3—Typical waveforms for CMOS phase-locked loop employing phase comparator in locked condition of f_o.

Phase-comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-state output circuit comprising p- and n-type drivers having a common output node. When the p-MOS or n-MOS drivers are ON they pull the output up to V_{DD} or down to V_{SS}, respectively. This type of phase comparator acts only on the positive edges of the signal and comparator inputs. The duty cycles of the signal and comparator inputs are not important since positive transitions

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
VCO Section											
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0.15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	Term. 4 driving CMOS e.g. Term.3	0,5	5	0.05				–	0	0.05	V
		0,10	10	0.05				–	0	0.05	
		0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.		0,5	5	4.95				4.95	5	–	
		0,10	10	9.95				9.95	10	–	
		0,15	15	14.95				14.95	15	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA
Phase Comparator Section											
Total Device Current, I_{DD} Max. Term. 14 open, Term. 5 = V_{DD}	–	0,5	5	0.2				–	0.1	0.2	mA
	–	0,10	10	1				–	0.5	1	
	–	0,15	15	1.5				–	0.75	1.5	
	–	0,20	20	4				–	2	4	
Term. 14 = V_{SS} or V_{DD}, Term. 5 = V_{DD}	–	0,5	5	20				–	10	20	μA
	–	0,10	10	40				–	20	40	
	–	0,15	15	80				–	40	80	
	–	0,20	20	160				–	80	160	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
DC-Coupled Signal Input and Comparator Input Voltage Sensitivity Low Level V_{IL} Max.	0.5,4.5	–	5			1.5		–	–	1.5	V
	1,9	–	10			3		–	–	3	
	1.5,13.5	–	15			4		–	–	4	
High Level V_{IH} Min.	0.5,4.5	–	5			3.5		3.5	–	–	
	1,9	–	10			7		7	–	–	
	1.5,13.5	–	15			11		11	–	–	

control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-type output driver is maintained ON most of the time, and both the n and p drivers OFF (3 state) the remainder of the time. If the signal-input frequency is lower than the comparator-input frequency, the n-type output driver is maintained ON most of the time, and both the n and p drivers OFF (3 state) the remainder of the time. If the signal- and comparator-input frequencies are the same, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the signal- and comparator-input frequencies are the same, but

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Phase Comparator Section (cont'd)											
Input Current I_{IN} Max. (except Term.14)	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA
3-State Leakage Current, I_{OUT} Max.	0,18	0,18	18	±0.1	±0.1	±0.2	±0.2	–	$\pm 10^{-5}$	±0.1*	μA

*Limit determined by minimum feasible leakage current measurement for automatic testing.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	TEST CONDITIONS		V_{DD} (V)	LIMITS ALL TYPES Min.	Typ.	Max.	UNITS
VCO Section							
Operating Power Dissipation, P_D	f_o = 10 kHz, R_2 = ∞	R_1 = 1 MΩ, $VCO_{IN} = \frac{V_{DD}}{2}$	5	–	70	140	μW
			10	–	800	1600	
			15	–	3000	6000	
Maximum Operating Frequency f_{max}	C_1=50 pF, R_2 = ∞, $VCO_{IN}=V_{DD}$	R_1 = 10 kΩ	5	0.3	0.6	–	MHz
			10	0.6	1.2	–	
			15	0.8	1.6	–	
	C_1 = 50 pF, R_2 = ∞, $VCO_{IN}=V_{DD}$	R_1 = 5 kΩ	5	0.5	0.8	–	
			10	1	1.4	–	
			15	1.4	2.4	–	
Center Frequency (f_o) and Frequency Range ($f_{max}-f_{min}$)	Programmable with external components R1, R2, and C1 *See Design Information*						
Linearity	VCO_{IN} = 2.5 V ± 0.3V, R_1=10 kΩ		5	–	1.7	–	%
	=5 V ± 1 V, = 100 kΩ		10	–	0.5	–	
	=5 V ± 2.5 V, =400 kΩ		10	–	4	–	
	=7.5 V ± 1.5 V, = 100 kΩ		15	–	0.5	–	
	= 7.5 V ± 5 V, = 1 MΩ		15	–	7	–	
Temperature-Frequency Stability: No Frequency Offset f_{MIN} = 0			5	–	±0.12	–	%/°C
			10	–	±0.04	–	
			15	–	±0.015	–	
Frequency Offset $f_{MIN} \neq 0$			5	–	±0.09	–	
			10	–	±0.07	–	
			15	–	±0.03	–	
Output Duty Cycle			5,10,15	–	50	–	%
Output Transition Times, t_{THL}, t_{TLH}			5	–	100	200	ns
			10	–	50	100	
			15	–	40	80	

the comparator input lags the signal in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point both p- and n-type output drivers remain OFF and thus the phase comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant. Moreover the signal at the "phase pulses" output is a high level which can be used for indicating a locked condition. Thus, for phase comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p- and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Fig. 10 shows typical waveforms for a CMOS PLL employing phase comparator II in a locked condition.

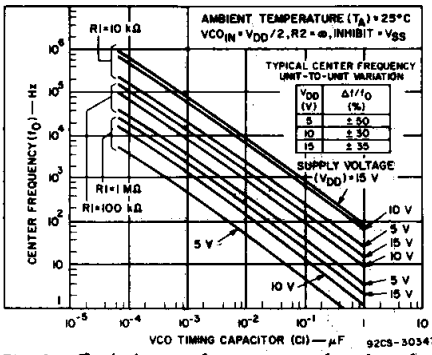


Fig. 4 – Typical center frequency as a function of C1 and R1 at V_{DD} = 5 V, 10 V, and 15 V.

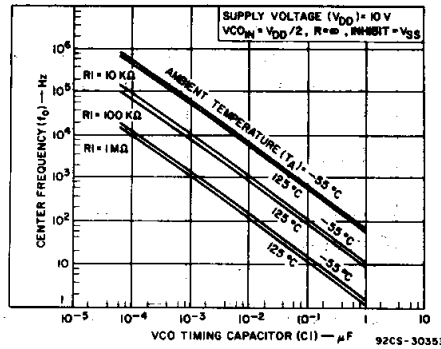


Fig. 5 – Center frequency as a function of C1 and R1 for ambient temperatures of −55°C to 125°C.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	TEST CONDITIONS		V_{DD} (V)	LIMITS ALL TYPES Min.	Typ.	Max.	UNITS
VCO Section (cont'd)							
Source-Follower Output (Demodulated Output): Offset Voltage $\lvert VCO_{IN}-V_{DEM}\rvert$	RS > 10 kΩ		5 10 15	– – –	1.8 1.8 1.8	2.5 2.5 2.5	V
Linearity	R_S=100 kΩ =300 kΩ =500 kΩ	VCO_{IN} = 2.5±0.3 V =5±2.5 V =7.5± 5 V	5 10 15	– – –	0.3 0.7 0.9	– – –	%
Zener Diode Voltage (V_z)	I_Z = 50 μA			4.45	5.5	6.15	V
Zener Dynamic Resistance, R_z	I_Z = 1 mA			–	40	–	Ω
Phase Comparator Section							
Term. 14 (SIGNAL IN) Input Resistance R_{14}			5 10 15	1 0.2 0.1	2 0.4 0.2	– – –	MΩ
AC Coupled Signal Input Voltage Sensitivity* (peak-to-peak)	f_{IN} = 100 kHz, sine wave		5 10 15	– – –	180 330 900	360 660 1800	mV
Propagation Delay Times, Terms. 14 to 1: High to Low Level, t_{PHL}			5 10 15	– – –	225 100 65	450 200 130	ns
Low to High Level, t_{PLH}			5 10 15	– – –	350 150 100	700 300 200	ns
3-State Propagation Delay Times, Terms. 3 to 13: High Level to High Impedance, t_{PHZ}			5 10 15	– – –	225 100 95	450 200 190	ns
Terms. 14 to 13: Low Level to High Impedance, t_{PLZ}			5 10 15	– – –	285 130 95	570 260 190	ns
Input Rise or Fall Times, t_r, t_f Comparator Input, Term. 3	See Fig. 5 for Phase Comp. II output loading		5 10 15	– – –	– – –	50 1 0.3	μs
Signal Input, Term. 14			5 10 15	– – –	– – –	500 20 2.5	μs
Output Transition Times, t_{THL}, t_{TLH}			5 10 15	– – –	100 50 40	200 100 80	ns

* For sine wave, the frequency must be greater than 10 kHz for Phase Comparator II.

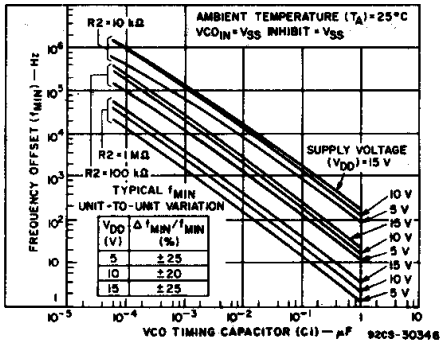


Fig. 6 – Typical frequency offset as a function of C1 and R2 for V_{DD} = 5 V, 10 V, and 15 V.

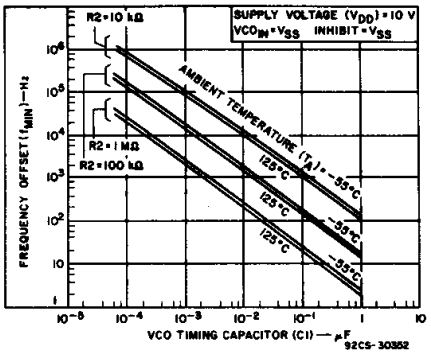


Fig. 7 – Frequency offset as a function of C1 and R2 for ambient temperatures of −55°C to 125°C.

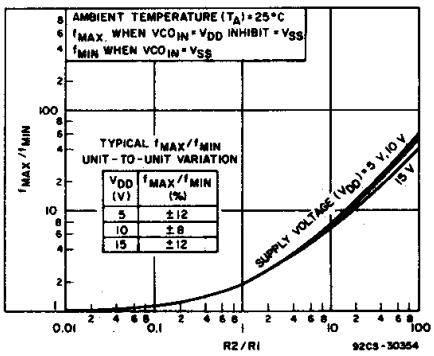


Fig. 8 – Typical f_{MAX}/f_{MIN} as a function of R2/R1.

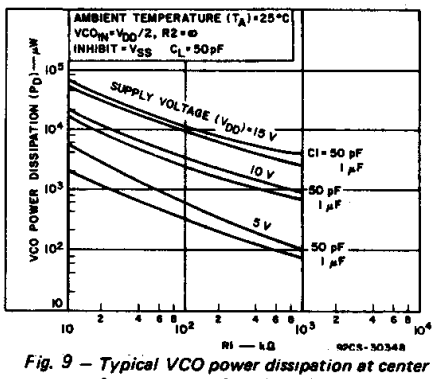


Fig. 9 – Typical VCO power dissipation at center frequency as a function of R1.

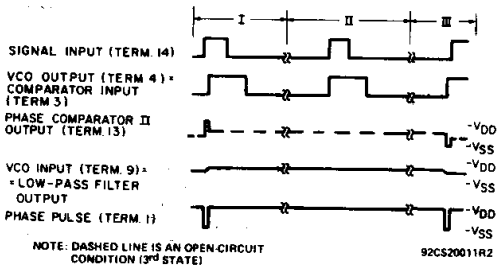


Fig. 10 - Typical waveforms for COS/MOS phase-locked loop employing phase comparator II in locked condition.

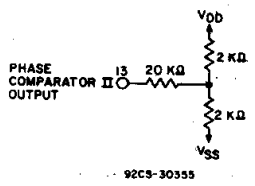


Fig. 11 – Phase comparator II output loading circuit.

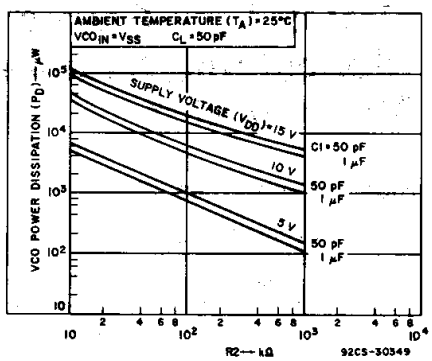


Fig. 12 – Typical VCO power dissipation at f_{MIN} as a function of R2.

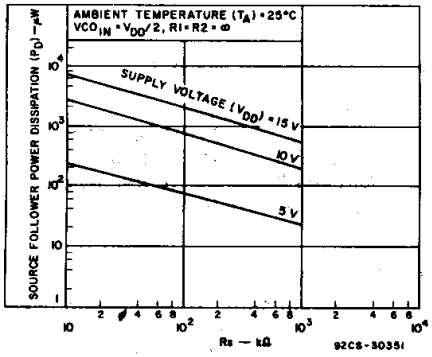


Fig. 13 – Typical source follower power dissipation as a function of Rs.

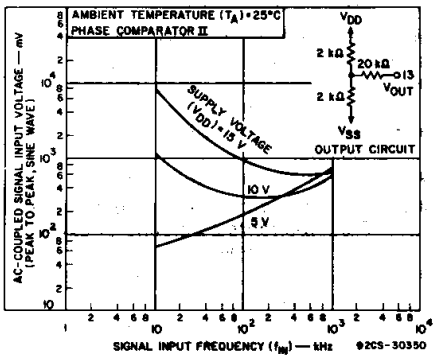


Fig. 14 – AC-coupled signal input voltage as a function of signal input frequency.

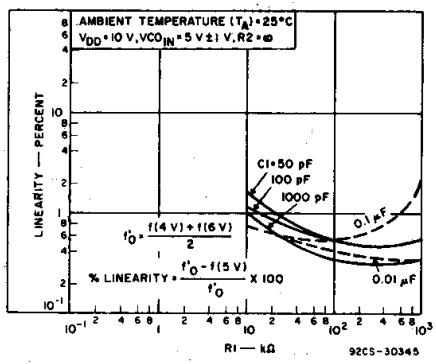


Fig. 15 – Typical VCO linearity as a function of R1 and C1 at V_{DD} = 10 V.

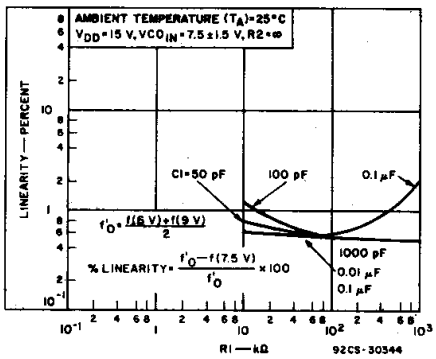
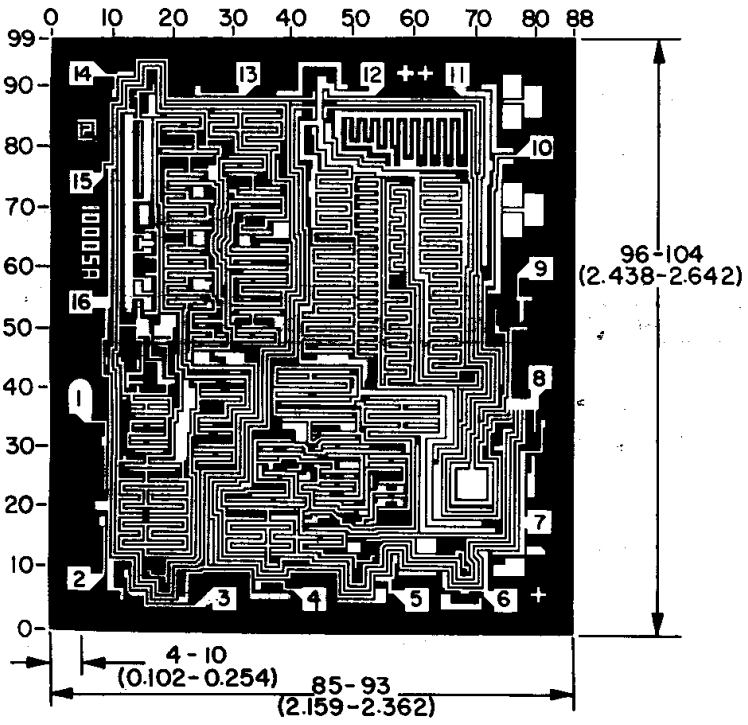


Fig. 16 – Typical VCO linearity as a function of R1 and C1 at V_{DD} = 15 V.



Dimensions and pad layout for CD4046BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

PACKAGE OPTION ADDENDUM

28-Feb-2005

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-9466401MEA	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4046BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD4046BF	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4046BF3A	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4046BNSR	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4046BPW	ACTIVE	TSSOP	PW	16	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CD4046BPWR	ACTIVE	TSSOP	PW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

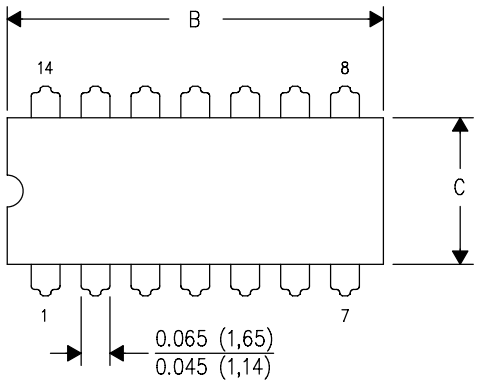
(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

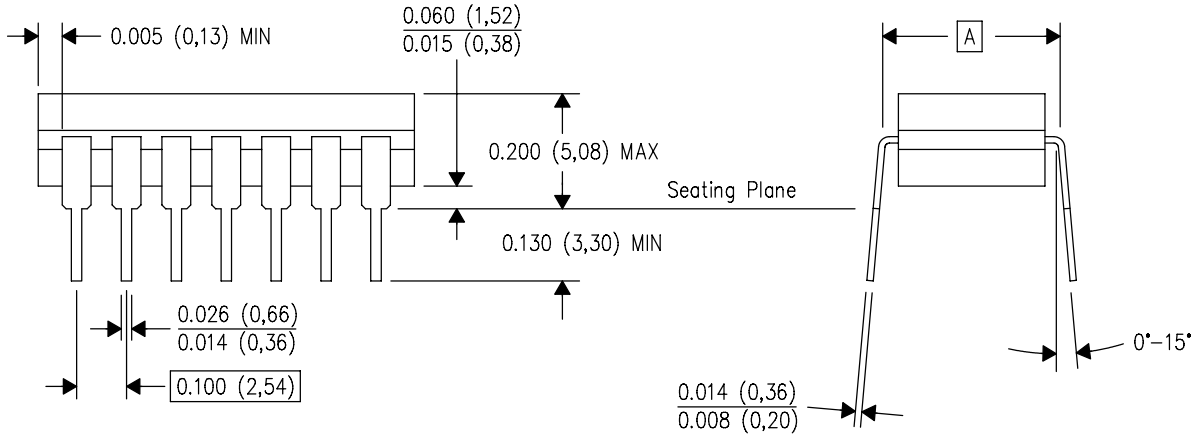
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



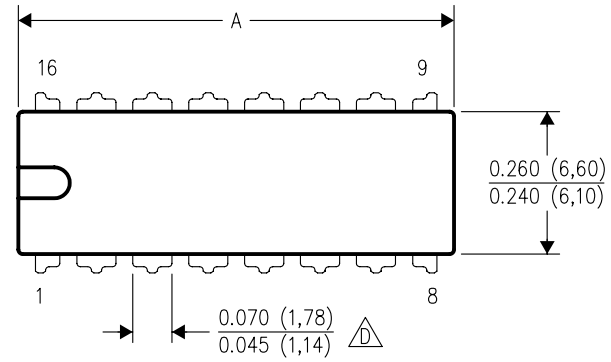
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

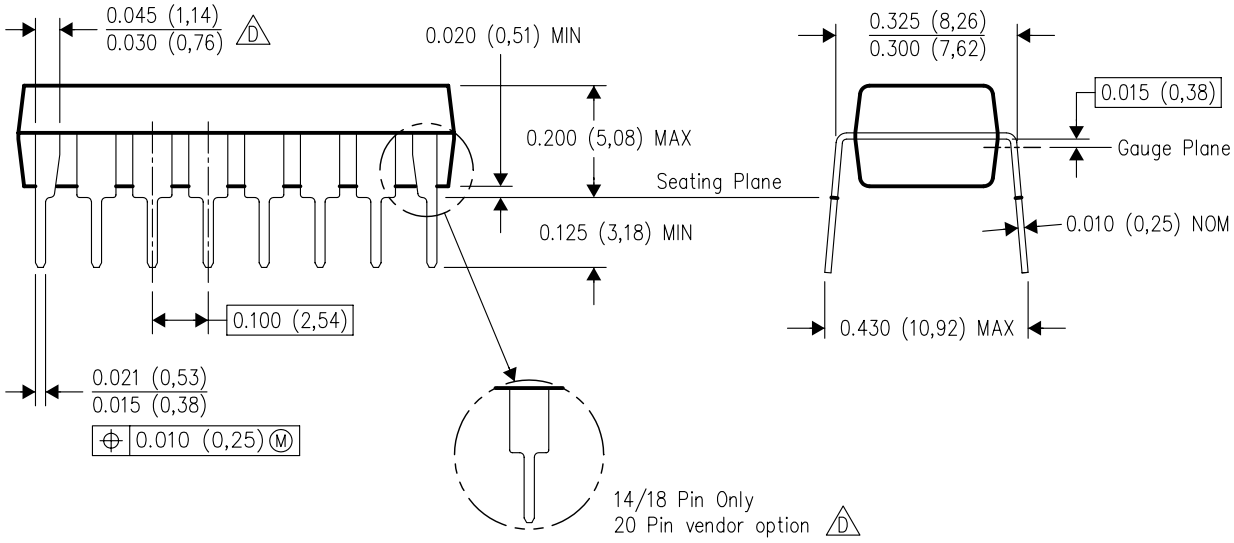
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



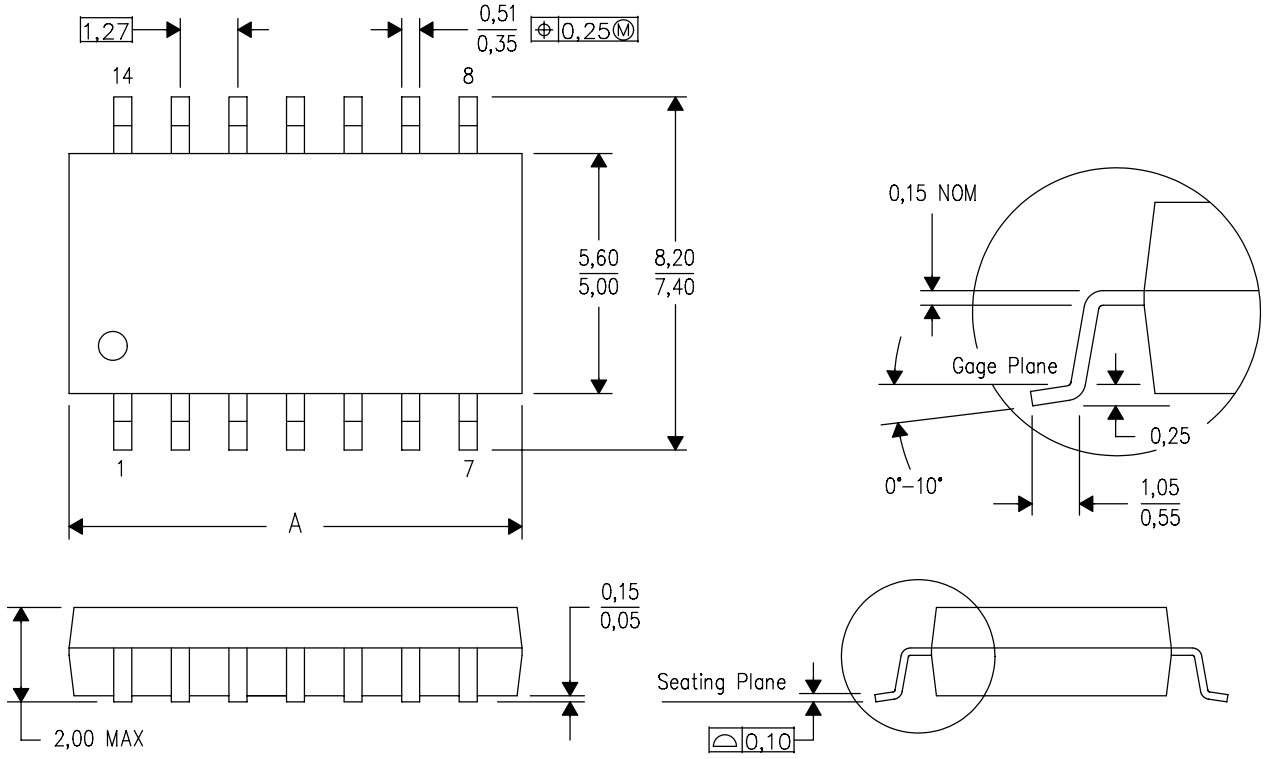
4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



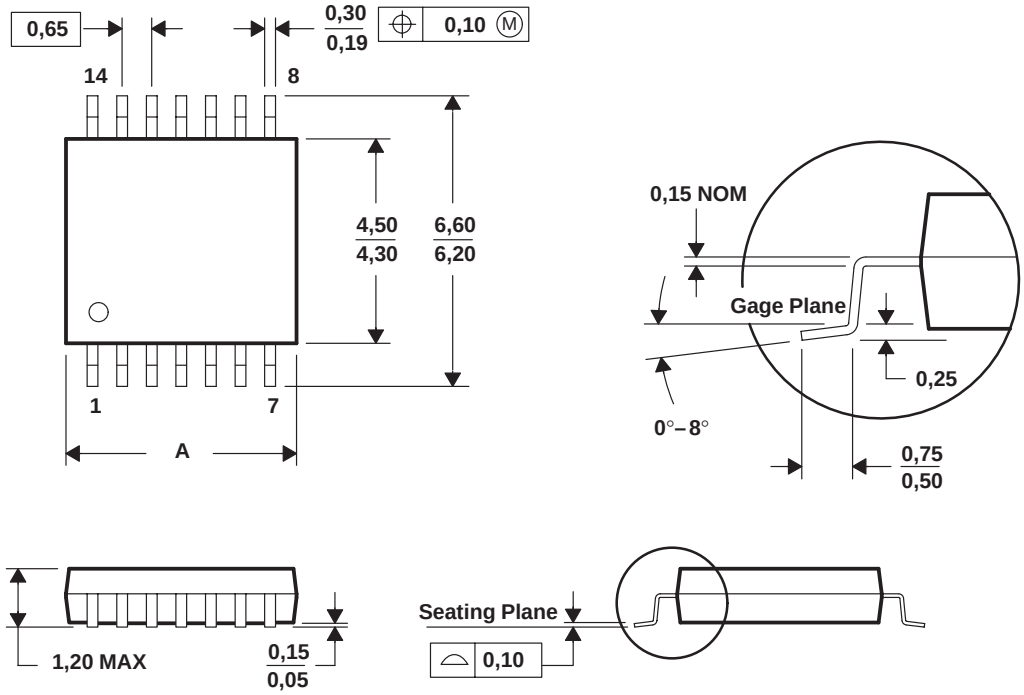
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265