intersil

CD4066BMS

CMOS Quad Bilateral Switch

December 1992

Features

- For Transmission or Multiplexing of Analog or Digital Signals
- High Voltage Types (20V Rating)
- 15V Digital or ±7.5V Peak-to-Peak Switching
- 125Ω Typical On-State Resistance for 15V Operation
- Switch On-State Resistance Matched to Within 5Ω Over 15V Signal Input Range
- On-State Resistance Flat Over Full Peak-to-Peak Signal Range
- High On/Off Output Voltage Ratio
  - 80dB Typ. at FIS = 10kHz, RL = 1kΩ
- High Degree of Linearity: <0.5% Distortion Typ. at FIS = 1kHz, VIS = 5Vp-p, VDD - VSS ≥ 10V, RL = 10kΩ
- Extremely Low Off-State Switch Leakage Resulting in Very Low Offset Current and High Effective Off-State Resistance: 10pA Typ. at VDD - VSS = 10V, T_A = +25°C
- Extremely High Control Input Impedance (Control Circuit Isolated from Signal Circuit): $10^{12}\Omega$ Typ.
- Low Crosstalk Between Switches: -50dB Typ. at FIS = 8MHz, RL = 1kΩ
- Matched Control Input to Signal Output Capacitance: Reduces Output Signal Transients
- Frequency Response, Switch on = 40MHz (Typ.)
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of "B" Series CMOS Devices"

Applications

- Analog Signal Switching/Multiplexing
  - Signal Gating
  - Squelch Control
  - Chopper
  - Modulator
  - Demodulator
  - Commutating Switch
- Digital Signal Switching/Multiplexing
- Transmission Gate Logic Implementation
- Analog to Digital & Digital to Analog Conversion
- Digital Control of Frequency, Impedance, Phase, and Analog Signal Gain

Description

CD4066BMS is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin for pin compatible with CD4016B, but exhibits a much lower on state resistance. In addition, the on-state resistance is relatively constant over the full input signal range.

The CD4066BMS consists of four independent bilateral switches. A single control signal is required per switch. Both the p and the n device in a given switch are biased on or off simultaneously by the control signal. As shown in Figure 1, the well of the n channel device on each switch is either tied to the input when the switch is on or to VSS when the switch is off. This configuration eliminates the variation of the switch transistor threshold voltage with input signal, and thus keeps the on-state resistance low over the full operating signal range.

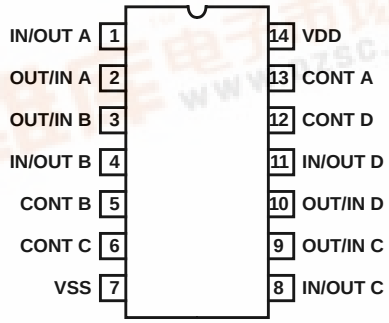
The advantages over single channel switches include peak input signal voltage swings equal to the full supply voltage, and more constant on-state impedance over the input signal range. For sample and hold applications, however, the CD4016B is recommended.

The CD4066BMS is supplied in these 14-lead outline packages:

Braze Seal DIP	H4Q
Frit Seal DIP	H1B
Ceramic Flatpack	H3W

Pinout

CD4066BMS
TOP VIEW



Specifications CD4066BMS

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . . -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . . . -0.5V to VDD +0.5V
DC Input Current, Any One Input . . . . . ±10mA
Operating Temperature Range . . . . . -55^{o}C to +125^{o}C
Package Types D, F, K, H
Storage Temperature Range (TSTG) . . . . . -65^{o}C to +150^{o}C
Lead Temperature (During Soldering) . . . . . +265^{o}C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80^{o}C/W	20^{o}C/W
Flatpack Package	70^{o}C/W	20^{o}C/W

Maximum Package Power Dissipation (PD) at +125^{o}C
For TA = -55^{o}C to +100^{o}C (Package Type D, F, K) 500mW
For TA = +100^{o}C to +125^{o}C (Package Type D, F, K) . . . . . Derate Linearity at 12mW/^{o}C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature . . . . . +175^{o}C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25^{o}C	-	0.5	µA
				2	+125^{o}C	-	50	µA
		VDD = 18V, VIN = VDD or GND		3	-55^{o}C	-	0.5	µA
Input Leakage Current	IIL	VC = VDD or GND		1	+25^{o}C	-100	-	nA
				2	+125^{o}C	-1000	-	nA
				3	-55^{o}C	-100	-	nA
Input Leakage Current	IIH	VC = VDD or GND		1	+25^{o}C	-	100	nA
				2	+125^{o}C	-	1000	nA
				3	-55^{o}C	-	100	nA
Input/Output Leakage Current (Switch OFF)	IOZL	VC = 0V, VIS = 18V, VOS = 0V, VIS = 0V, VOS = 18V	VDD = 20	1	+25^{o}C	-100	-	nA
				2	+125^{o}C	-1000	-	nA
			VDD = 18V	3	-55^{o}C	-100	-	nA
	IOZH		VDD = 20	1	+25^{o}C	-	100	nA
				2	+125^{o}C	-	1000	nA
			VDD = 18V	3	-55^{o}C	-	100	nA
On Resistance	RON5	VC = VDD, RL = 10kW returned to VDD - VSS/2 VIS = VSS to VDD	VDD = 5V	1	+25^{o}C	1050	-	Ω
	RON10		VDD = 10V	1	+25^{o}C	400	-	Ω
	RON15		VDD = 15V	1	+25^{o}C	240	-	Ω
On Resistance	RON5	VDD = 5V		1, 2	+125^{o}C	-	1300	Ω
					-55^{o}C	-	800	Ω
On Resistance	RON10	VDD = 10V		1, 2	+125^{o}C	-	550	Ω
					-55^{o}C	-	310	Ω
On Resistance	RON15	VDD = 15V		1, 2	+125^{o}C	-	320	Ω
					-55^{o}C	-	220	Ω
Functional (Note 3)	F	VDD = 2.8V, VIN = VDD or GND		7	+25^{o}C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25^{o}C			
		VDD = 18V, VIN = VDD or GND		8A	+125^{o}C			
		VDD = 3V, VIN = VDD or GND		8B	-55^{o}C			
Switch Threshold RL = 100k to VDD	SWTHRH5	VDD = 5V, VC = 1.5V, VIS = GND		1, 2, 3	+25^{o}C, +125^{o}C, -55^{o}C	4.1	-	V
	SWTHRH15	VDD = 15V, VC = 2V, VIS = GND		1, 2, 3	+25^{o}C, +125^{o}C, -55^{o}C	14.1	-	V
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25^{o}C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25^{o}C	0.7	2.8	V

Specifications CD4066BMS

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Control Input Low Voltage (Note 2) |IIS| < 10µa, VIS = VSS, VOS = VDD and VIS = VDD, VOS = VSS	VILC5	VDD = 5V	1, 2, 3	+25°C, +125°C, -55°C	-	1	V
	VILC15	VDD = 15V	1, 2, 3	+25°C, +125°C, -55°C	-	2	V
Control Input High Voltage (Note 2, Figure 2) VIS = VSS and VIS = VDD	VIHC	VDD = 5V, |IIS| = .51mA, 4.6V < VOS < 0.4V	1	+25°C	3.5	-	V
		VDD = 5V, |IIS| = .36mA, 4.6V < VOS < 0.4V	2	+125°C	3.5	-	V
		VDD = 5V, |IIS| = .64mA, 4.6V < VOS < 0.4V	3	-55°C	3.5	-	V
	VIHC	VDD = 15V, |IIS| = 3.4mA, 13.5V < VOS <1.5V	1	+25°C	11	-	V
		VDD = 15V, |IIS| = 2.4mA, 13.5V < VOS < 1.5V	2	+125°C	11	-	V
		VDD = 15V, |IIS| = 4.2mA, 13.5V < VOS <1.5V	3	-55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. VDD = 2.8V/3.0V, RL = 100K to VDD
VDD = 20V/18V, RL = 10K to VDD

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Signal Input to Signal Output	TPLH TPHL	VC = VDD = 5V, VSS = GND (Notes 2, 3)	9	+25°C	-	40	ns
			10, 11	+125°C, -55°C	-	54	ns
Propagation Delay Turn-On, Turn-Off	TPHZ/ZH TPLZ/ZL	VIS = VDD = 5V (Notes 1, 2)	9	+25°C	-	70	ns
			10, 11	+125°C, -55°C	-	95	ns

NOTES:

1. CL = 50pF, RL = 1K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.25	µA
				+125°C	-	7.5	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.5	µA
				+125°C	-	15	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.5	µA
				+125°C	-	30	µA
Control Input Low Voltage |IIS| < 10µa, VIS = VSS, VOS = VDD and VIS = VDD, VOS = VSS	VILC10	VDD = 10V	1, 2	+25°C, +125°C, -55°C	-	2	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Control Input High Voltage (See Figure 2)	VIHC10	VDD = 10V, VIS = VDD or GND	2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay Signal Input to Signal Output	TPLH TPHL	VDD = 10V	1, 2, 3	+25°C	-	20	ns
		VDD = 15V	1, 2, 3	+25°C	-	15	ns
Propagation Delay Turn-On, Turn-Off	TPHZ/ZH TPLZ/ZL	VDD = 10V	1, 2, 3	+25°C	-	40	ns
		VDD = 15V	1, 2, 3	+25°C	-	30	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - SSI	IDD	±0.1µA
ON Resistance	RONDEL10	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
Interim Test 2 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

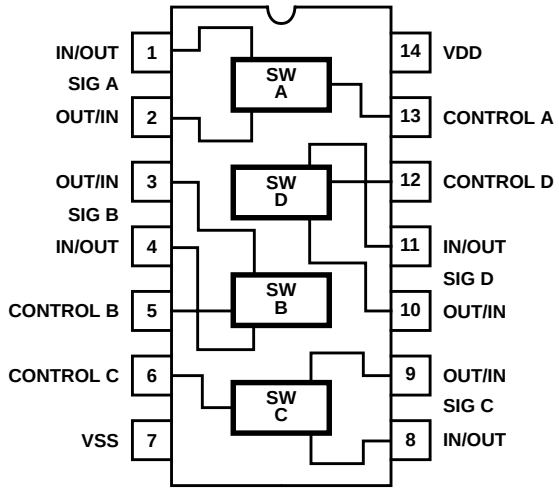
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	2, 3, 9, 10	1, 4-8, 11-13	14			
Static Burn-In 2 (Note 1)	2, 3, 9, 10	7	1, 4-6, 8, 11-14			
Dynamic Burn-In (Note 1)	-	7	14	2, 3, 9, 10	5, 6, 12, 13	1, 4, 8, 11
Irradiation (Note 2)	2, 3, 9, 10	7	1, 4-6, 8, 11-14			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Functional Diagram



TRUTH TABLE EACH SWITCH		
INPUT		OUTPUT
VC	VIS	VOS
1	0	0
1	1	1
0	0	Open
0	1	Open

Positive Logic: Switch ON VC = “1”
Switch OFF VC = “0”

Schematic

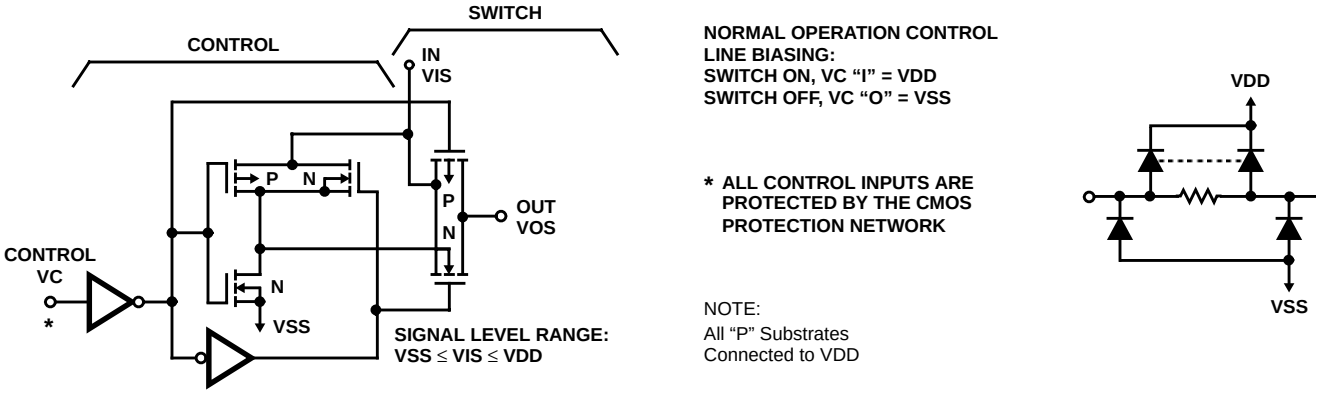


FIGURE 1. SCHEMATIC DIAGRAM OF 1 OF 4 IDENTICAL SWITCHES AND ITS ASSOCIATED CONTROL CIRCUITRY

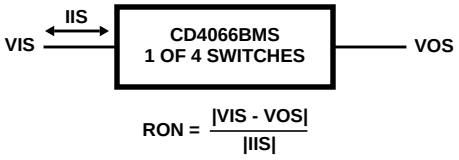


FIGURE 2. DETERMINATION OF RON AS A TEST CONDITION FOR CONTROL INPUT HIGH VOLTAGE (VIHC) SPECIFICATION

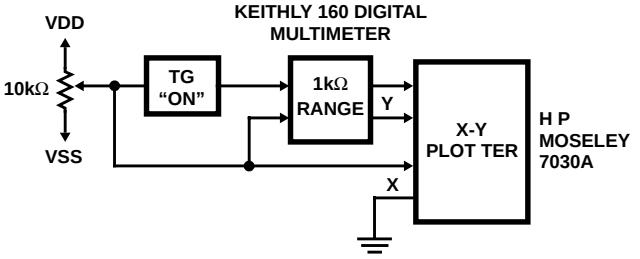


FIGURE 3. CHANNEL ON-STATE RESISTANCE MEASUREMENT CIRCUIT

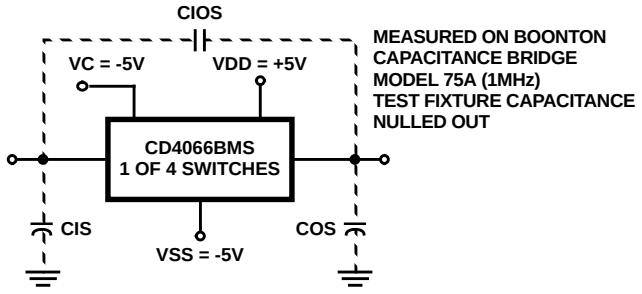


FIGURE 4. CAPACITANCE TEST CIRCUIT

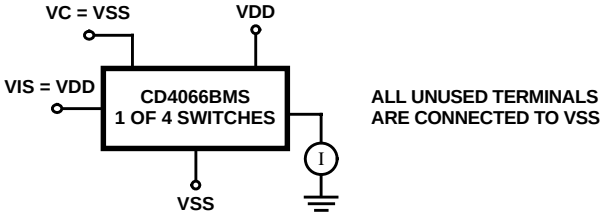


FIGURE 5. OFF SWITCH INPUT OR OUTPUT LEAKAGE

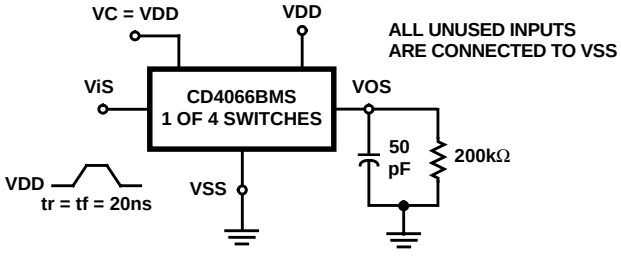


FIGURE 6. PROPAGATION DELAY TIME SIGNAL INPUT (VIS) TO SIGNAL OUTPUT (VOS)

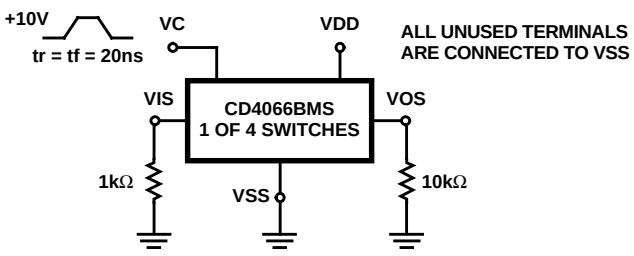


FIGURE 7. CROSSTALK CONTROL INPUT TO SIGNAL OUTPUT

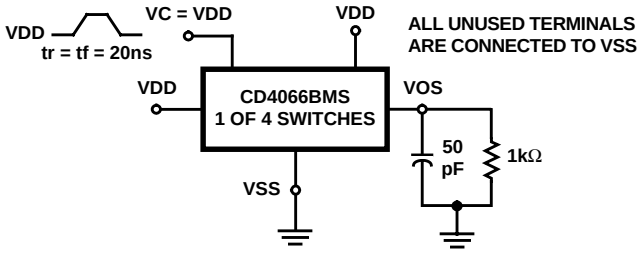
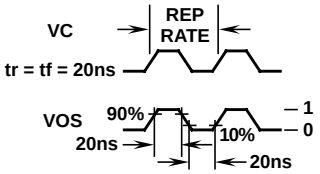


FIGURE 8. PROPAGATION DELAY TPLH, TPHL CONTROL SIGNAL OUTPUT. DELAY IS MEASURED AT VOS LEVEL OF +10% FROM GROUND (TURN ON) OR ON-STATE OUTPUT LEVEL (TURN OFF).



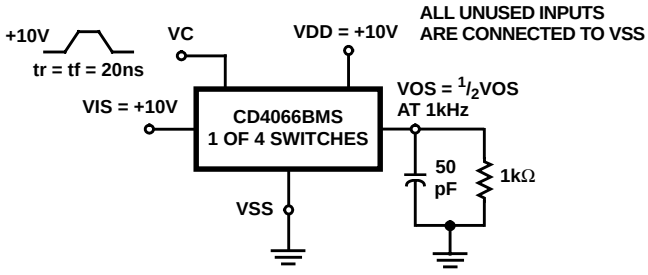


FIGURE 9. MAXIMUM ALLOWABLE CONTROL INPUT REPETITION RATE

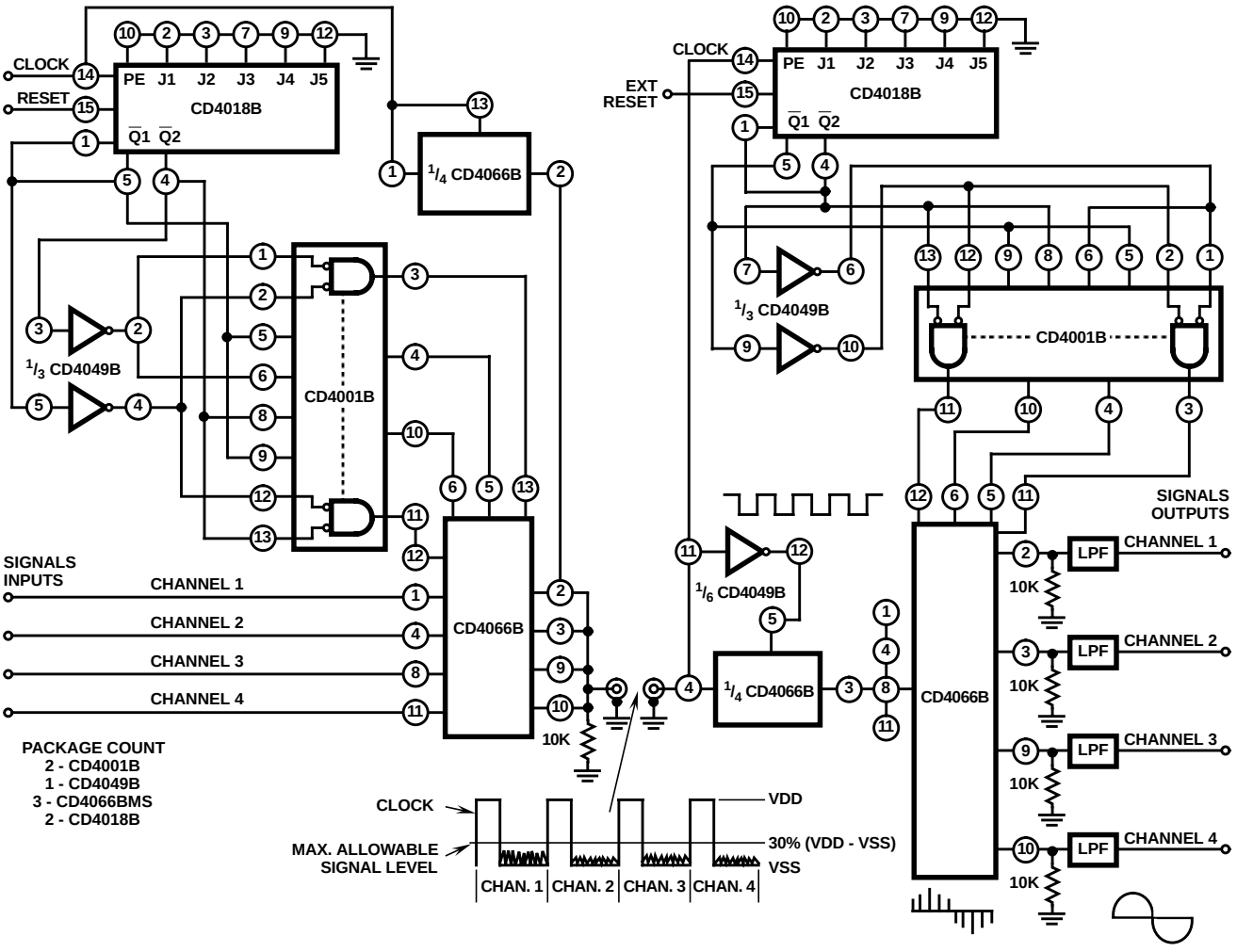


FIGURE 10. 4 CHANNEL PAM MULTIPLEX SYSTEM DIAGRAM

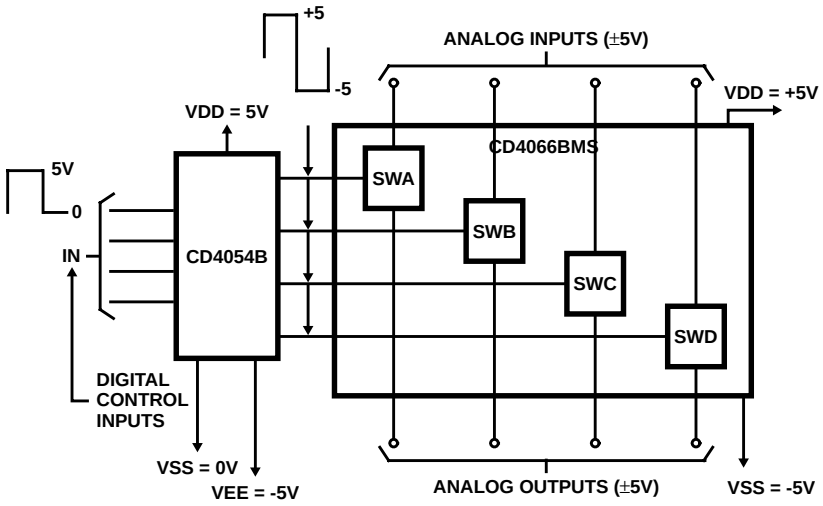


FIGURE 11. BIDIRECTIONAL SIGNAL TRANSMISSION VIA DIGITAL CONTROL LOGIC

Typical Performance Characteristics

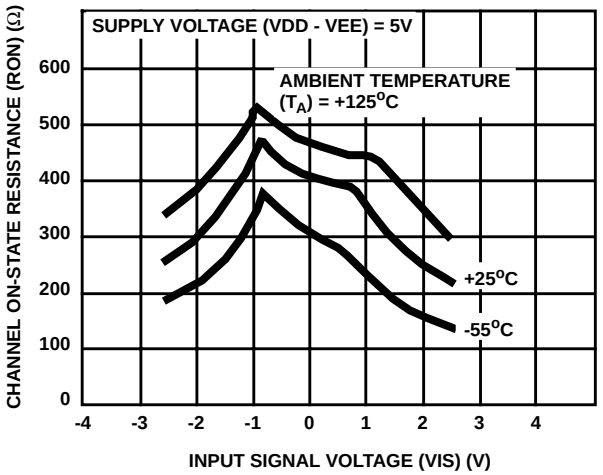


FIGURE 12. TYPICAL ON-STATE RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

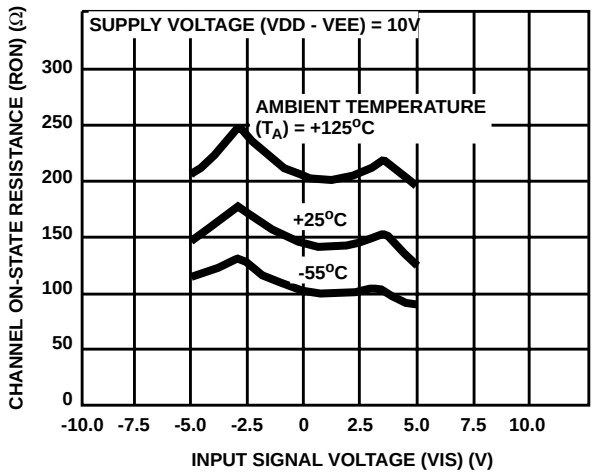


FIGURE 13. TYPICAL ON-STATE vs INPUT SIGNAL VOLTAGE (ALL TYPES).

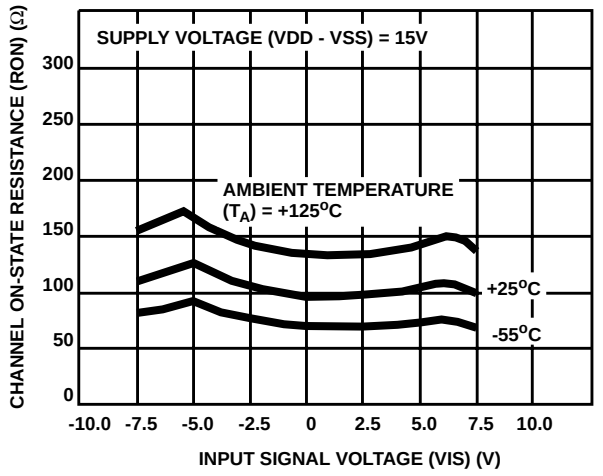


FIGURE 14. TYPICAL ON-STATE RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

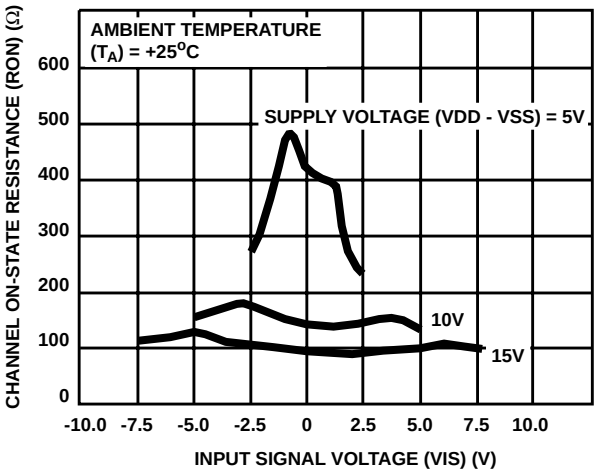


FIGURE 15. ON-STATE RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

Typical Performance Characteristics (Continued)

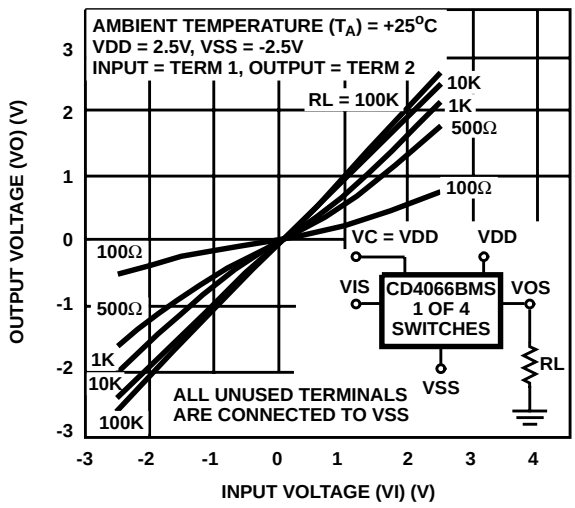


FIGURE 16. TYPICAL ON CHARACTERISTICS FOR 1 OF 4 CHANNELS

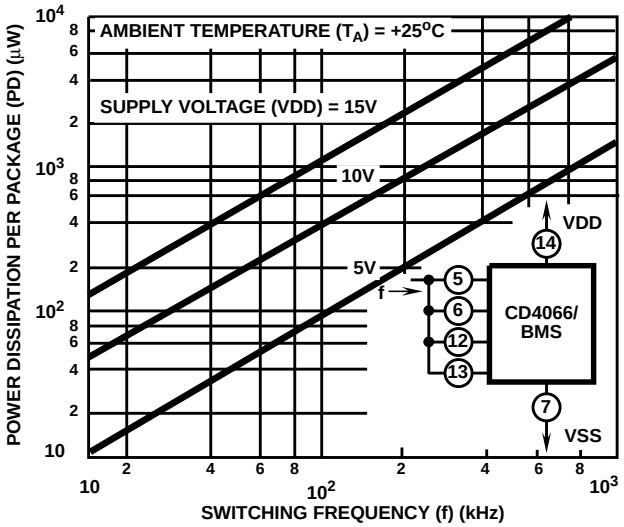
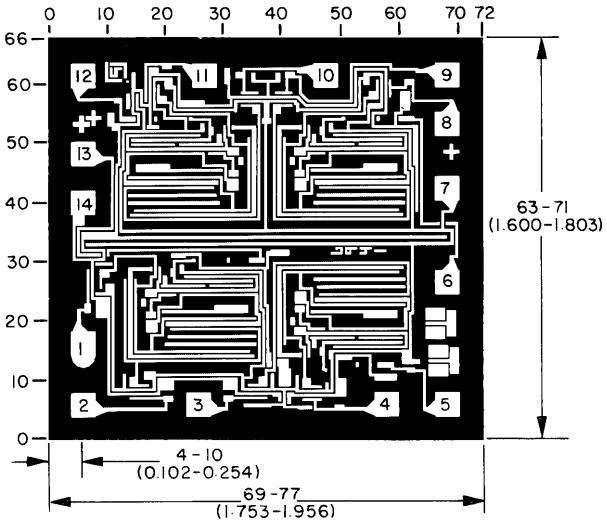


FIGURE 17. POWER DISSIPATION PER PACKAGE vs SWITCHING FREQUENCY

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Special Considerations

In applications that employ separate power sources to drive VDD and the signal inputs, the VDD current capability should exceed VDD/RL (RL = effective external load of the four CD4066B bilateral switches). This provision avoids any permanent current flow or clamp action on the VDD supply when power is applied or removed from the CD4066B.

In certain applications, the external load-resistor current may include both VDD and signal line components. To avoid drawing VDD current when switch current flows into terminals 1, 4, 8 or 11 the voltage drop across the bidirectional switch must not exceed 0.8 volts (calculated from RON values shown).

No VDD current will flow through RL if the switch current flows into terminals 2, 3, 9, or 10.

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches